

# **Baseline for CGMII Extender, CGMII Extender Sublayer (100GXS)**

Gary Nicholl, Cisco

Shawn Nicholl, Xilinx

IEEE P802.3cn and P802.3ck Task Force Interim Meetings

Long Beach, CA

January 2019

# Supporters

- **Mark Gustlin – Cisco**
- **Ilya Lyubomirsky – Inphi**
- **Jeff Slavick – Broadcom**

# Relevant P802.3cn Objectives

- **Proposed Objectives**

- Support full-duplex operation only
- Preserve the Ethernet frame format utilizing the Ethernet MAC
- Preserve minimum and maximum FrameSize of current Ethernet standard
- Provide appropriate support for OTN

- **100 Gb/s Ethernet**

- Support a MAC data rate of 100 Gb/s
- Support a BER of better than or equal to  $10^{-12}$  at the MAC/PLS service interface (or the frame loss ratio equivalent) for 100 Gb/s
- Provide a physical layer specification supporting 100 Gb/s operation on a single wavelength capable of at least 80 km over a DWDM system.

- **400 Gb/s Ethernet**

- Support a MAC data rate of 400 Gb/s
- Support a BER of better than or equal to  $10^{-13}$  at the MAC/PLS service interface (or the frame loss ratio equivalent) for 400 Gb/s
- Provide a physical layer specification supporting 400 Gb/s operation on a single wavelength capable of at least 80 km over a DWDM system.

# Relevant P802.3ck Objectives

- Support a MAC data rate of 100 Gb/s, 200 Gb/s and 400 Gb/s
- Support full-duplex operation only
- Preserve the Ethernet frame format utilizing the Ethernet MAC
- Preserve minimum and maximum FrameSize of current IEEE 802.3 standard
- Support the existing bit error ratios (BERs) at the MAC/PLS service interface (or the frame loss ratio equivalent) for 100 Gb/s, 200 Gb/s and 400 Gb/s Ethernet

- Define a single-lane 100 Gb/s Attachment Unit interface (AUI) for chip-to-module applications, compatible with PMDs based on 100 Gb/s per lane optical signaling
- Define a single-lane 100 Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications
- Define a single-lane 100 Gb/s PHY for operation over electrical backplanes supporting an insertion loss  $\approx 28$  dB at 26.56 GHz.
- Define a single-lane 100 Gb/s PHY for operation over twin-axial copper cables with lengths up to at least 2 m.

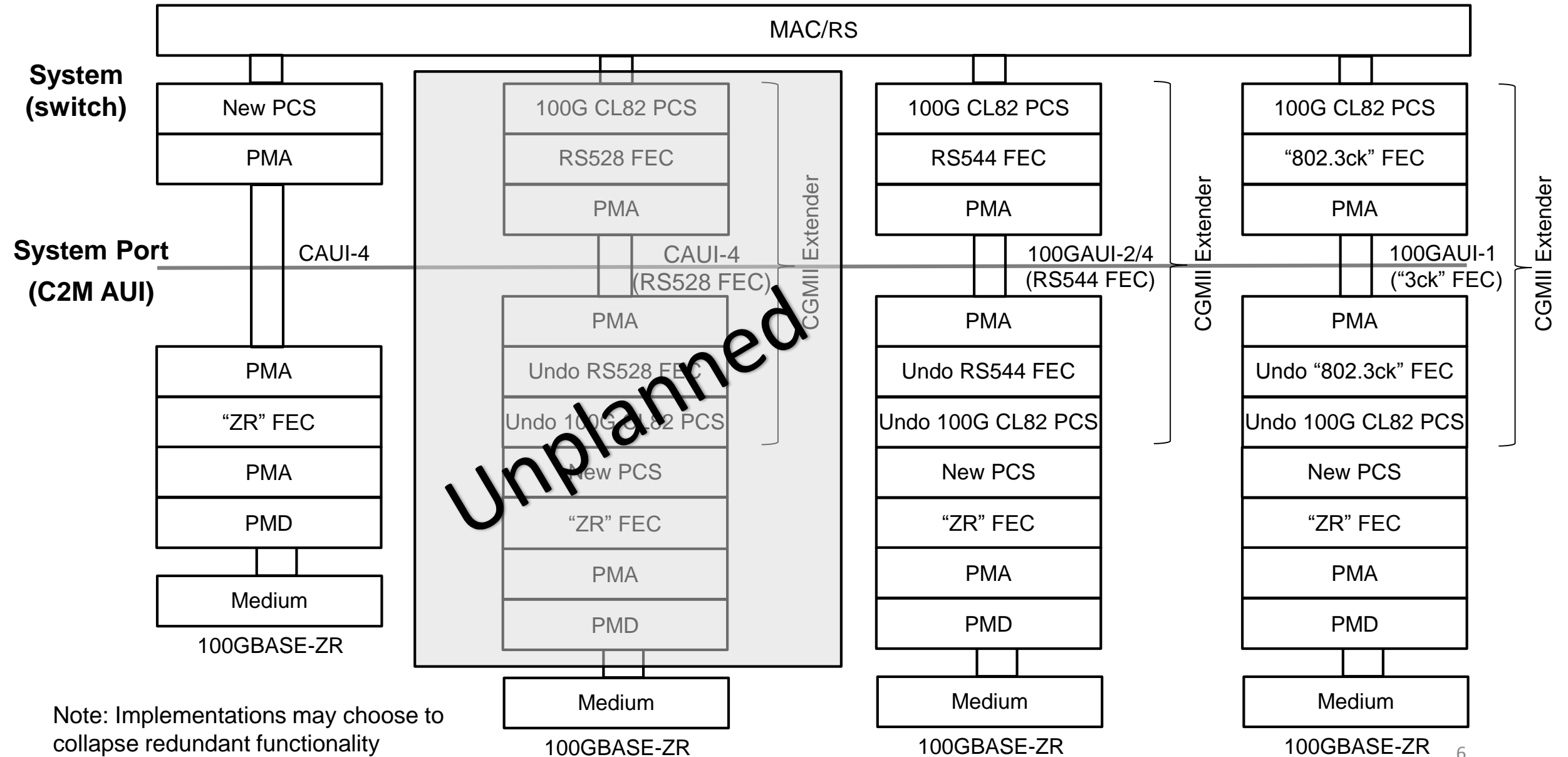
- Define a two-lane 200 Gb/s Attachment Unit interface (AUI) for chip-to-module applications, compatible with PMDs based on 100 Gb/s per lane optical signaling.
- Define a two-lane 200 Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications.
- Define a two-lane 200 Gb/s PHY for operation over electrical backplanes supporting an insertion loss = 28 dB at 26.56 GHz.
- Define a two-lane 200 Gb/s PHY for operation over twin-axial copper cables with lengths up to at least 2 m.

- Define a four-lane 400 Gb/s Attachment Unit interface (AUI) for chip-to-module applications, compatible with PMDs based on 100 Gb/s per lane optical signaling.
- Define a four-lane 400 Gb/s Attachment Unit Interface (AUI) for chip-to-chip applications.
- Define a four-lane 400 Gb/s PHY for operation over electrical backplanes supporting an insertion loss  $\approx 28$  dB at 26.56 GHz.
- Define a four-lane 400 Gb/s PHY for operation over twin-axial copper cables with lengths up to at least 2 m.

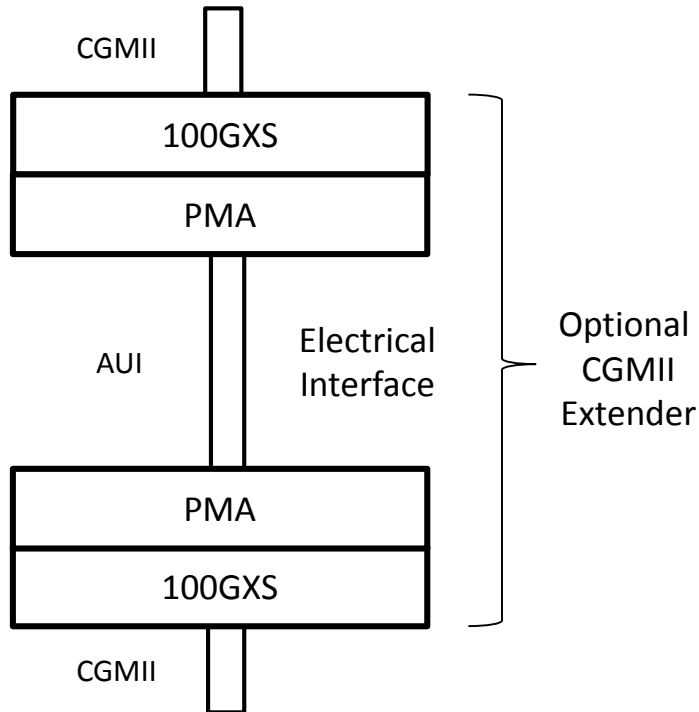
# Background

- **Previous work on this topic includes the following:**
  - [nicholl b10k 01a 0518](#) proposed using the Clause 118 existing 400GMII Extender and 400GMII Extender Sublayer (400GXS) to enable a new 400GBASE-ZR PHY to interface to a 400GAUI-n and address the 400G 80km DWDM PHY objective.
  - [nicholl b10k 01a 0518](#) also highlighted that there is no existing 100 Gb/s Extender Sublayer
  - [nicholl 3cn 01 1118](#) described the motivation for a CGMII Extender Sublayer (100GXS) to enable a new 100GBASE-ZR PHY to interface to one of several possible 100 Gigabit Ethernet AUIs and address the 100G 80km DWDM PHY objective:
    - CAUI-4/10 without FEC
    - CAUI-4 with RS(528,514) FEC
    - 100GAUI-2/4 with RS(544,514) FEC
    - 100GAUI-1 which is under development in P802.3ck
- **The new CGMII Extender and CGMII Extender Sublayer (100GXS) will take an approach that is similar to the existing 400GMII Extender and 400GMII Extender Sublayer (400GXS)**
  - While other approaches have been considered (for example, “upside side down FEC”), the CGMII Extender provides a means to capture the required functionality in a manner like previously used
- **This presentation proposes a baseline for the CGMII Extender Sublayer (100GXS) and CGMII Extender, to support extension of the CGMII across a physically instantiated 100GAUI-4 or 100GAUI-2 interface**
  - The 100GXS is likely to be used in all 100GBASE-ZR PHYs

# 100GBASE-ZR Use Cases – Functional Stack up

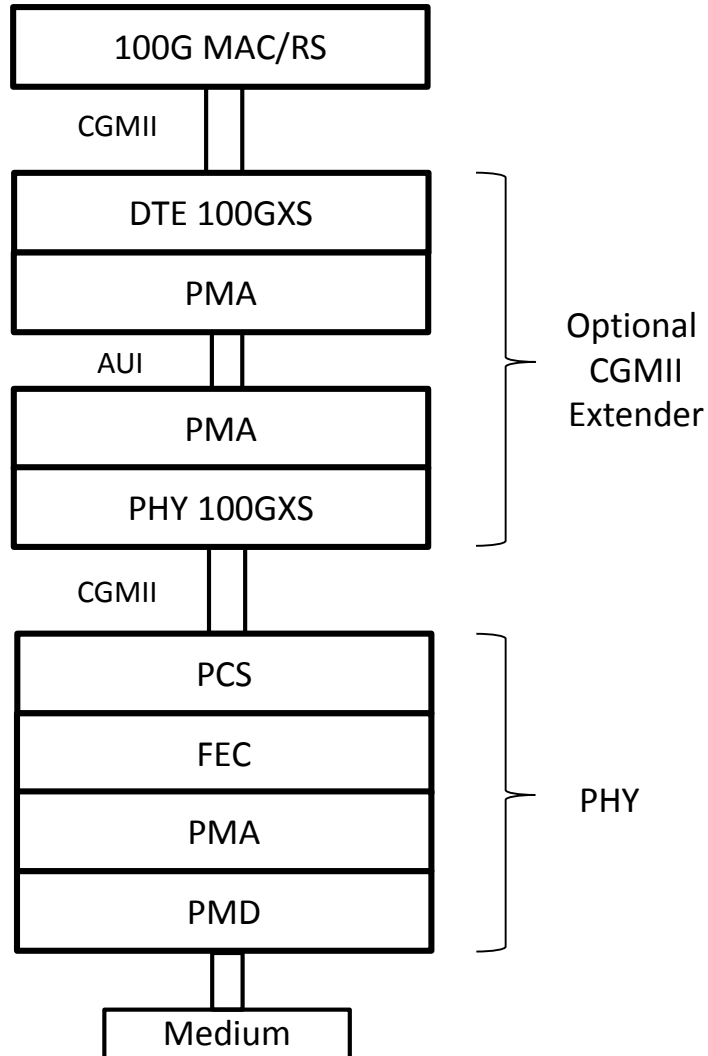


# CGMII Extender Concept



- The **CGMII Extender** is used to extend the **CGMII** across a physically instantiated **AUI**
- The **CGMII Extender Sublayer (100GXS)** is the proposed extender sublayer to extend the **CGMII**
  - A pair of 100GXS instances along with AUI is used to extend the CGMII
  - A typical instantiation is a high speed parallel SerDes interface
- The **100GXS** is optional for **100 Gb/s Ethernet**, only used if the **PCS/FEC** does not cover both the electrical and optical interface needs
- The **100GXS** contains **PCS** and **FEC** functionality related to the extender sublayer

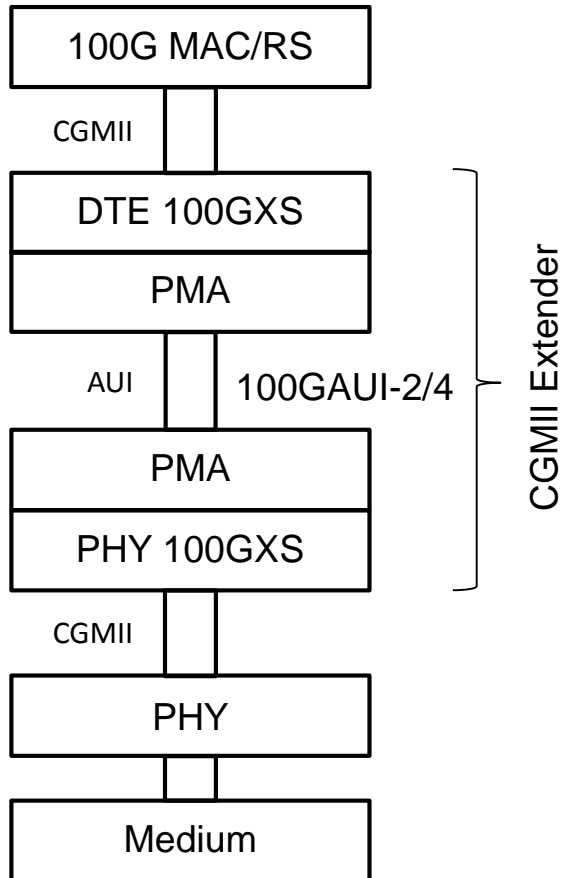
# CGMII Extender Details



- **The CGMII Extender is composed of the following:**
  - DTE 100GXS at the RS end
  - PHY 100GXS at the PHY end
  - Physical instantiation of 100 Gb/s AUI between the adjacent PMA sublayers
- **This allows support for new PCS/FEC/PMA functionality (different implementations, alternate FEC coding, or future PHYs) below the extended CGMII, if needed.**
  - The 100GXS is a combination of the functionality of the 100G PCS sublayer and the FEC sublayer associated with a specific AUI interface
  - The 100GXS provides the coding / FEC of the electrical interface, not the coding / FEC of the PHY



# CGMII Extender and CGMII Extender Sublayer (100GXS) Baseline Proposal



- **DTE 100GXS based on:**
  - CL82 100G PCS
  - CL91 RS(544,514)
- **PHY 100GXS based on:**
  - CL82 100G PCS
  - CL91 RS(544,514)
- **Supports extension of the CGMII across a physically instantiated 100GAUI-2/4 interface**
  - CL135 100G PMA
  - Annex 135D, 135E, 135F, 135G
- Note: Support for extension of the CGMII across a single-lane 100 Gb/s (AUI) is anticipated future work of P802.3ck task force

# Editorial Guidance – Table of Contents

- **Add new Clause TBD – CGMII Extender, CGMII Extender Sublayer (100GXS)**
  - The new clause can take an approach similar to 802.3-2018 Clause 118

✓	🔖	118. 200GMII Extender, 400GMII Extender, 200GMII Extender Sublayer (200GXS), and 400GMII Extender Sublayer (400GXS)
✓	🔖	118.1 Overview
	🔖	118.1.1 Summary of major concepts
	🔖	118.1.2 200GXS/400GXS Sublayer
	🔖	118.1.3 200GAUI-n/400GAUI-n
<del>✓</del>	<del>🔖</del>	<del>118.2 FEC Degrade</del>
	<del>🔖</del>	<del>118.2.1 DTE XS FEC Degrade signaling</del>
	<del>🔖</del>	<del>118.2.2 PHY XS FEC Degrade signaling</del>
	🔖	118.3 200GXS and 400GXS partitioning example
	🔖	118.4 200GXS and 400GXS MDIO function mapping
>	🔖	118.5 Protocol implementation conformance statement (PICS) proforma for Clause 118, 200GMII Extender, 400GMII Extender, 200GMII Extender Sublayer (200GXS), and 400GMII Extender Sublayer (400GXS)

- **Note that FEC Degrade capability is not present at 100 Gb/s**

# Editorial Guidance – Supported AUI instantiations

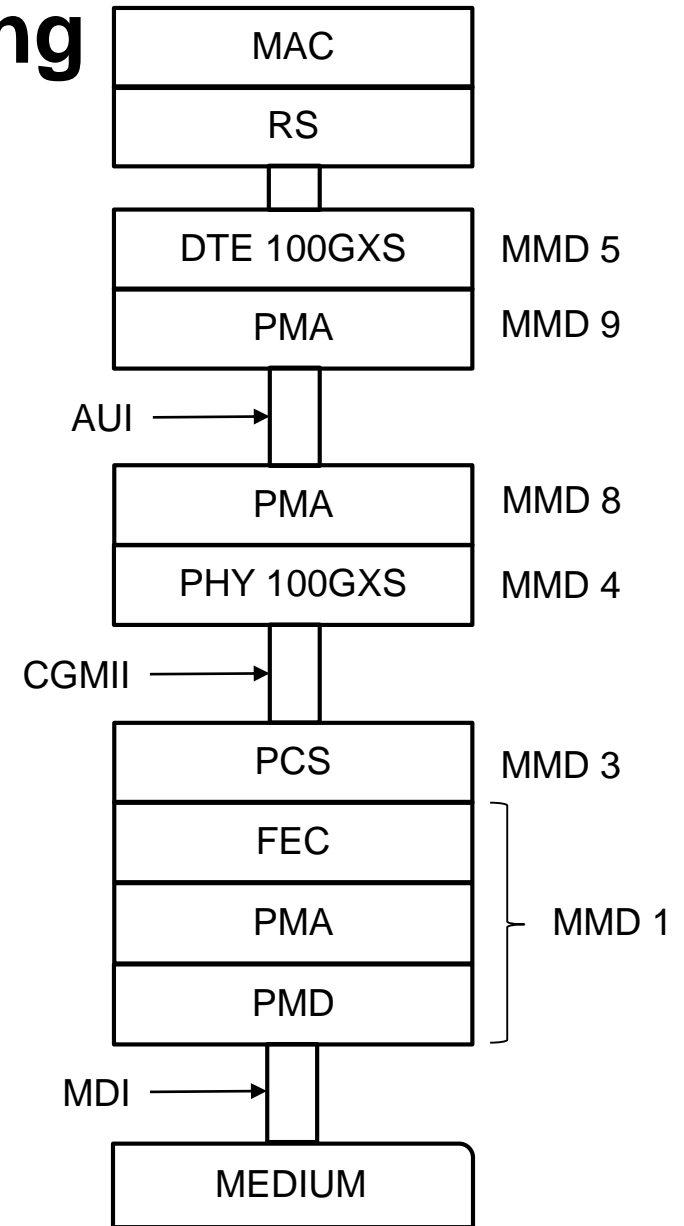
- **Like Clause 118, the new Clause TBD should indicate that a CGMII Extender may use the following 100G AUI instantiation:**
  - 100GAUI-2/4 (Annex 135D, 135E, 135F, 135G)
    - With RS(544,514) FEC
- **The following AUI instantiation is anticipated to be added as part of P802.3ck:**
  - 100GAUI-1 (Annex TBD)
- **Intentionally omitted from the above list are:**
  - ~~CAUI-10 (Annex 83A)~~
    - ~~Without RS-FEC~~
  - ~~CAUI-4 (Annex 83E)~~
    - ~~Without RS-FEC~~
    - ~~With RS(528,514) FEC~~

# Editorial Guidance – MMD Numbering

- Like Clause 118, the new Clause TBD should contain the 100GXS MDIO function mapping for MDIO PHY XS and DTE XS registers
- MMD addresses as per Clause 45
  - Note: FEC registers are included under PMA/PMD MMD

Table 45-1—MDIO Manageable Device addresses

Device address	MMD name
0	Reserved
1	PMA/PMD
2	WIS
3	PCS
4	PHY XS
5	DTE XS
6	TC
7	Auto-Negotiation
8	Separated PMA (1)
9	Separated PMA (2)
10	Separated PMA (3)
	Separated PMA (4)



**Thank You!**

# Backups

## **P802.3cn – Proposed Motion**

**Move to adopt the CGMII Extender baseline as proposed in nicholl\_3cn\_01\_0119.pdf, page 9**