Options for C2M Reference Equalizer

Ali Ghiasi

Ghiasi Quantum LLC

IEEE 802.3ck Taskforce Meeting

Salt Lake City

May 21, 2019

Overview

- Channel investigated are Lim 3/19 802.3ck channels
- COM analysis at TP1a and CDR Slicer with Lim channels
- COM analysis at TP5 and ASIC Slicer with Lim channels
- COM analysis of Yamaichi mated board at TP4/TP5
- Best choice for reference equalizer
- Summary

Lim QSFP-dd Channels

- **30 layers 150 mils thick Megtron 7 board with 10 mils via stub the channel also include ASIC or CDR BGA foot print effects, for detail channel description see**
  - http://www.ieee802.org/3/ck/public/19_03/lim_3ck_01a_0319.pdf
  - http://www.ieee802.org/3/ck/public/tools/c2m/lim_3ck_01_0319_c2m.zip
  - Lim COM results at TP1a are shown in the table to the right for Cd increased to 130 ff
- **Lim more challenging channels 3 and 4 with CDR BGA foot prints and channel 5 and 6 with ASIC BGA foot prints are analyzed in this contribution at following test points:**
  - TP1a, CDR Slicer, TP5, and ASIC Slicer.

DUT	COM case 1	COM case 2	ERL11 (dB)	ERL22 (dB)	ICN (mV)	IL@26G (15mm)*	ILD
Channel 1 FFE4post	4.27	4.47	13.57	9.63	0.77	14.4/18.0	0.19
Channel 2 FFE4post	3.15	4.01	11.49	9.53	0.81	14.6/18.3	0.19
Channel 1 FFE4postDFE1	5.10	5.23	13.64	9.63	0.77	14.4/18.1	0.19
Channel 2 FFE4postDFE1	4.54	4.83	11.49	9.53	0.81	14.6/18.4	0.19
Channel 3 FFE4post	3.87	4.52	13.51	10.22	0.77	14.7/18.4	0.19
Channel 4 FFE4post	2.55	4.07	11.66	10.13	0.85	14.9/18.6	0.18
Channel 3 FFE4postDFE1	5.06	5.20	13.54	10.22	0.77	14.7/18.4	0.19
Channel 4 FFE4postDFE1	4.41	4.70	11.66	10.13	0.85	14.9/18.6	0.18
Channel 5 FFE4post	2.45	3.83	10.44	9.58	1.41	14.7/18.5	0.16
Channel 6 FFE4post	1.36	3.51	10.62	10.23	1.55	15.0/18.8	0.17
Channel 5 FFE4postDFE1	4.33	4.75	10.44	9.58	1.41	14.7/18.5	0.16
Channel 6 FFE4postDFE1	3.94	4.44	10.62	10.23	1.55	15.0/18.8	0.17

COM Code 2.6.0 Host-Module TP1a

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.1e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
z_p select	[1 2]		[test cases to run]		Port Order	[1 3 2 4]			Table 92–12 parameters		
z_p (TX)	[15 30; 1.8 1.8]	mm	[test cases]		RUNTAG	C2M_1218			Parameter	Setting	
z_p (NEXT)	[15 30; 1.8 1.8]	mm	[test cases]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (FEXT)	[15 30; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]		COM Pass threshold	-3	dB		board_Z_c	90	Ohm
C_p	[0.87e-4 0]	nF	[TX RX]		ERL Pass threshold	0	dB		z_bp (TX)	50	mm
R_0	50	Ohm			DER_0	1.00E-05			z_bp (NEXT)	50	mm
R_d	[45 50]	Ohm	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	50	mm
A_v	0.41	V			FORCE_TR	1	logical		z_bp (RX)	0	mm
A_fe	0.41	V			Include PCB	0	logical				
A_ne	0.6	V			TDR and ERL options						
L	4				TDR	1	logical				
M	32				ERL	1	logical				
filter and Eq					ERL_ONLY	0	logical				
f_r	0.75	*fb			TR_TDR	0.01	ns				
c(0)	0.65		min		N	300					
c(-1)	[-0.2:0.02:0]		[min:step:max]	0.7	TDR_Butterworth	1	logical				
c(-2)	[0:.02:0.1]		[min:step:max]		beta_x	1.70E+09					
c(1)	[-0.1:0.02:0]		[min:step:max]		rho_x	0.18					
N_b	1	UI			fixture delay time	0					
b_max(1)	0.5				TDR_W_TXPKG	1					
b_max(2..N_b)	0.2				N_bx	4	UI				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Receiver testing						
f_z	18.55345912	GHz			RX_CALIBRATION	0	logical				
f_p1	53.1	GHz			Sigma BBN step	5.00E-03	V				
f_p2	28.2	GHz									
g_DC_HP	[-3:0.5:-1]		[min:step:max]		Noise, jitter						
f_HP_PZ	1.3275	GHz			sigma_RJ	0.01	UI				
ffe_pre_tap_len	0	UI			A_DD	0.02	UI				
ffe_post_tap_len	4	UI			eta_0	8.20E-09	V^2/GHz				
ffe_tap_step_size	0				SNR_TX	33	dB				
ffe_main_cursor_min	0.7				R_LM	0.95					
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.125										
ffe_backoff	1										

COM Code 2.6.0 Host-Module Slicer Input

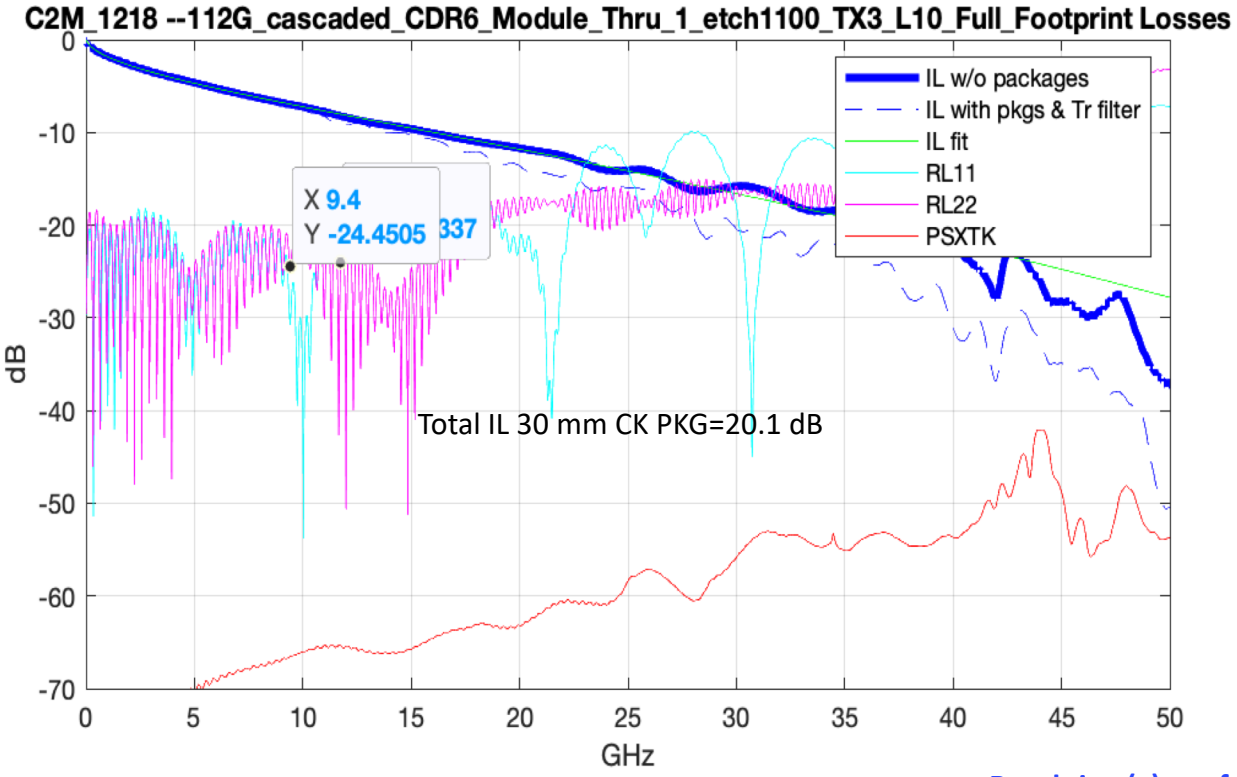
Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.1e-4 0.85e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
z_p select	[1 2]		[test cases to run]		Port Order	[1 3 2 4]			Table 92–12 parameters		
z_p (TX)	[15 30; 1.8 1.8]	mm	[test cases]		RUNTAG	C2M_1218			Parameter	Setting	
z_p (NEXT)	[15 30; 1.8 1.8]	mm	[test cases]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (FEXT)	[15 30; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (RX)	[2 8 ; 0 0]	mm	[test cases]		COM Pass threshold	-3	dB		board_Z_c	90	Ohm
C_p	[0.87e-4 0.65e-4]	nF	[TX RX]		ERL Pass threshold	0	dB		z_bp (TX)	50	mm
R_0	50	Ohm			DER_0	1.00E-05			z_bp (NEXT)	50	mm
R_d	[45 45]	Ohm	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	50	mm
A_v	0.41	V			FORCE_TR	1	logical		z_bp (RX)	0	mm
A_fe	0.41	V			Include PCB	0	logical				
A_ne	0.6	V			TDR and ERL options						
L	4				TDR	1	logical				
M	32				ERL	1	logical				
filter and Eq					ERL_ONLY	0	logical				
f_r	0.75	*fb			TR_TDR	0.01	ns				
c(0)	0.55		min		N	300					
c(-1)	[-0.2:0.02:0]		[min:step:max]	0.9	TDR_Butterworth	1	logical				
c(-2)	[0:.02:0.1]		[min:step:max]		beta_x	1.70E+09					
c(1)	[-0.1:0.02:0]		[min:step:max]		rho_x	0.18					
N_b	0	UI			fixture delay time	0					
b_max(1)	0.5				TDR_W_TXPKG	1					
b_max(2..N_b)	0.2				N_bx	4	UI				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Receiver testing						
f_z	18.55345912	GHz			RX_CALIBRATION	0	logical				
f_p1	53.1	GHz			Sigma BBN step	5.00E-03	V				
f_p2	28.2	GHz									
g_DC_HP	[-3:0.5:-1]		[min:step:max]		Noise, jitter						
f_HP_PZ	1.3275	GHz			sigma_RJ	0.01	UI				
ffe_pre_tap_len	0	UI			A_DD	0.02	UI				
ffe_post_tap_len	4	UI			eta_0	8.20E-09	V^2/GHz				
ffe_tap_step_size	0				SNR_TX	33	dB				
ffe_main_cursor_min	0.7				R_LM	0.95					
ffe_pre_tap1_max	0.35										
ffe_post_tap1_max	0.35										
ffe_tapn_max	0.2										
ffe_backoff	1										

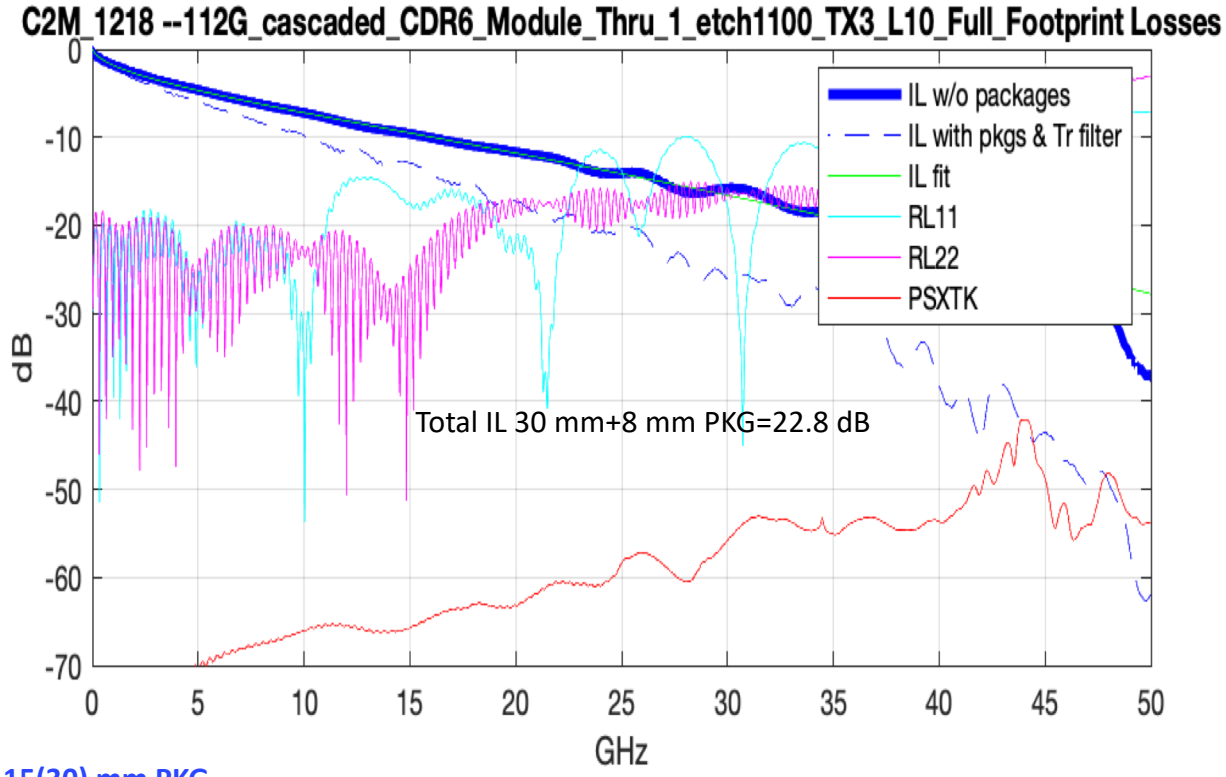
COM Analysis on Lim Channel 3 – ASIC to Module

- **Lim channel 3 (short via) Legacy QSFP-dd contacts includes retimer foot print at TP1a and slicer input**

TP1a FOM_ILD=0.11, ICN=0.77 mV, ICR=43, ERL11=16.1, ERL22=10.4
5T FFE: COM=4.1 (5.1) dB, EH=14.2 (13.5) mV, VEC=8.5 (7.1) dB
TX FIR [0.02, -0.12, 0.86, 0] Optimum
5T FFE(4 post)+1DFE: COM=5.3 (5.5) dB, EH=22.3 (20) mV, VEC=6.8 (6.5) dB
TX FIR [0.02, -0.12, 0.86, 0] Optimum
4DFE: COM=5.0 (5.3) dB, EH=20.9 (15.9) mV, VEC=7.2 (6.9) dB
TX FIR [0.04, -0.18, 0.78, 0] Optimum

Slicer Input FOM_ILD=0.11, ICN=0.77 mV, ICR=43, ERL11=16.1, ERL22=10.4
5T FFE: COM=3.7 (4.1) dB, EH=10.0 (10.3) mV, VEC=9.2 (8.6) dB
TX FIR [0.04, -0.18, 0.74, -0.04] Optimum
5T FFE(4 post)+1DFE: COM=4.2 (5.1) dB, EH=13.8 (15.5) mV, VEC=7.8 (7.0) dB
TX FIR [0.04, -0.2, 0.76, 0] Optimum
4DFE: COM=4.2 (4.8) dB, EH=16.3 (15.3) mV, VEC=8.3 (7.4) dB
TX FIR [0.04, -0.2, 0.76, 0] Optimum





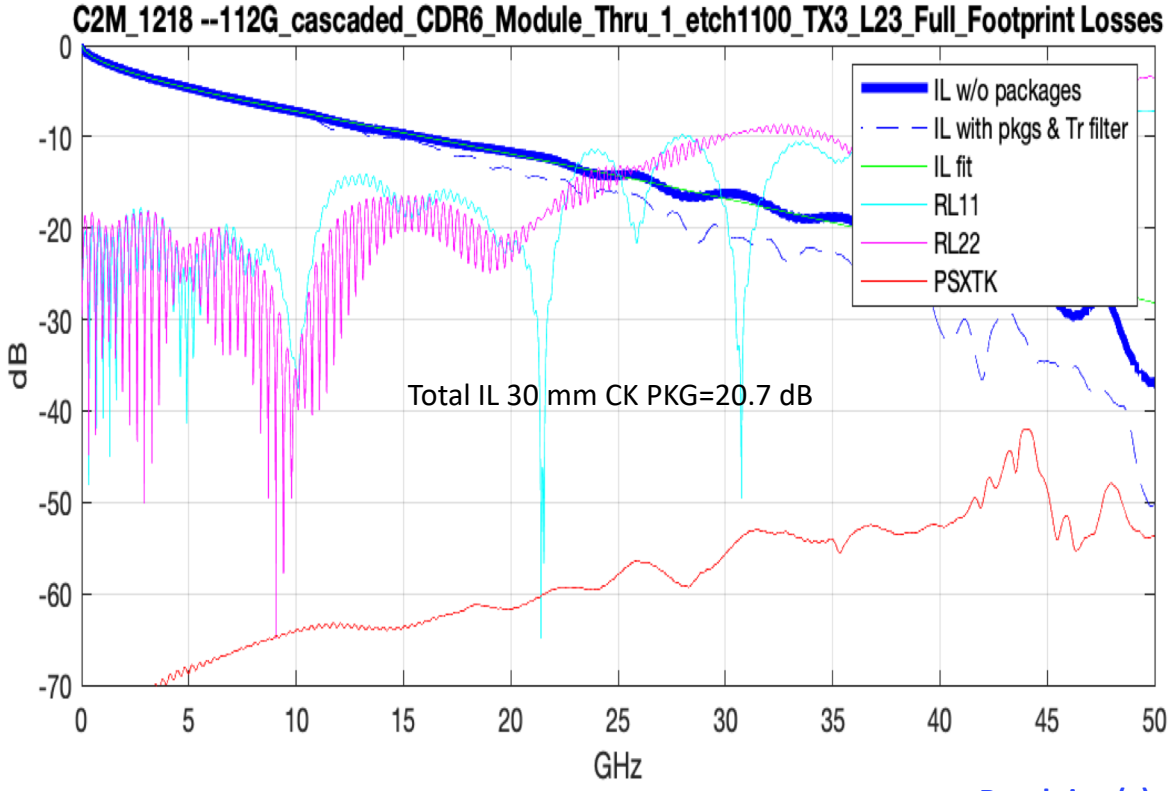
Result in x(y) are for 15(30) mm PKG.

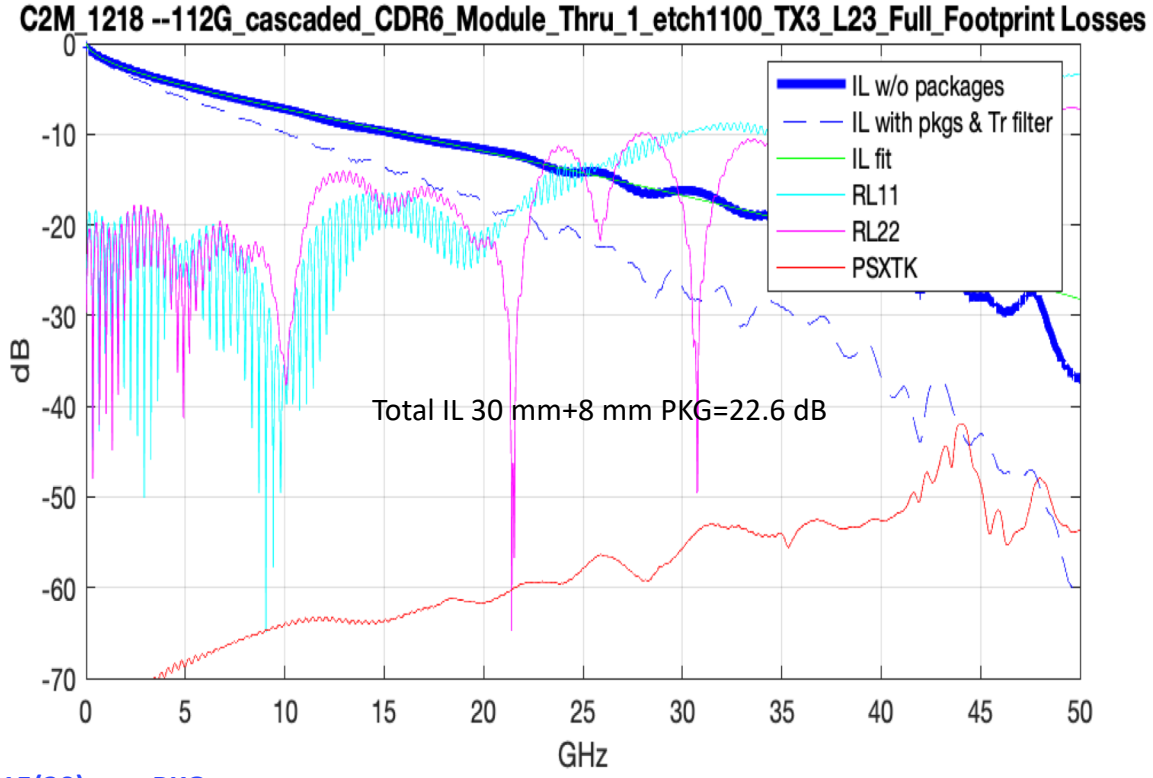
COM Analysis on Lim Channel 4 – ASIC to Module

- **Lim channel 4 (long via) Legacy QSFP-dd contact includes retimer foot print at TP1a and slicer input**

TP1a, FOM_ILD=0.18, ICN=0.85 mV, ICR=42 dB, , ERL11=15.9, ERL22=10.3
5T FFE(4 post): COM=2.8 (4.7) dB, EH=9.3 (11.7) mV, VEC=11.1 (7.5) dB
TX FIR[-0.04, -0.18, 0.78, 0.04] Optimum
5T FFE(4 post)+1DFE: COM=4.6 (5.1) dB, EH=19.7 (18.7) mV, VEC=7.7 (7.0) dB
TX FIR[-0.04, -0.2, 0.78, 0] Optimum
4DFE: COM=4.5 (5.0) dB, EH=16.6 (14.5) mV, VEC=7.6 (7.2) dB
TX FIR[-0.04, -0.18, 0.78, 0] Optimum

Slicer Input, FOM_ILD=0.18, ICN=0.85 mV, ICR=42 dB, , ERL11=15.9, ERL22=10.3
5T FFE(4 post): COM=2.2 (4.4) dB, EH=6.9 (8.9) mV, VEC=13.2 (8.6) dB
TX FIR[-0.04, -0.18, 0.72, -0.06] Optimum
5T FFE(4 post)+1DFE: COM=4.0 (4.6) dB, EH=13.9 (13.8) mV, VEC=8.9 (7.7) dB
TX FIR[-0.04, -0.2, 0.76, 0] Optimum
4DFE: COM=3.8 (5.0) dB, EH=16.6 (14.5) mV, VEC=7.6 (7.2) dB
TX FIR[-0.04, -0.2, 0.76, 0] Optimum



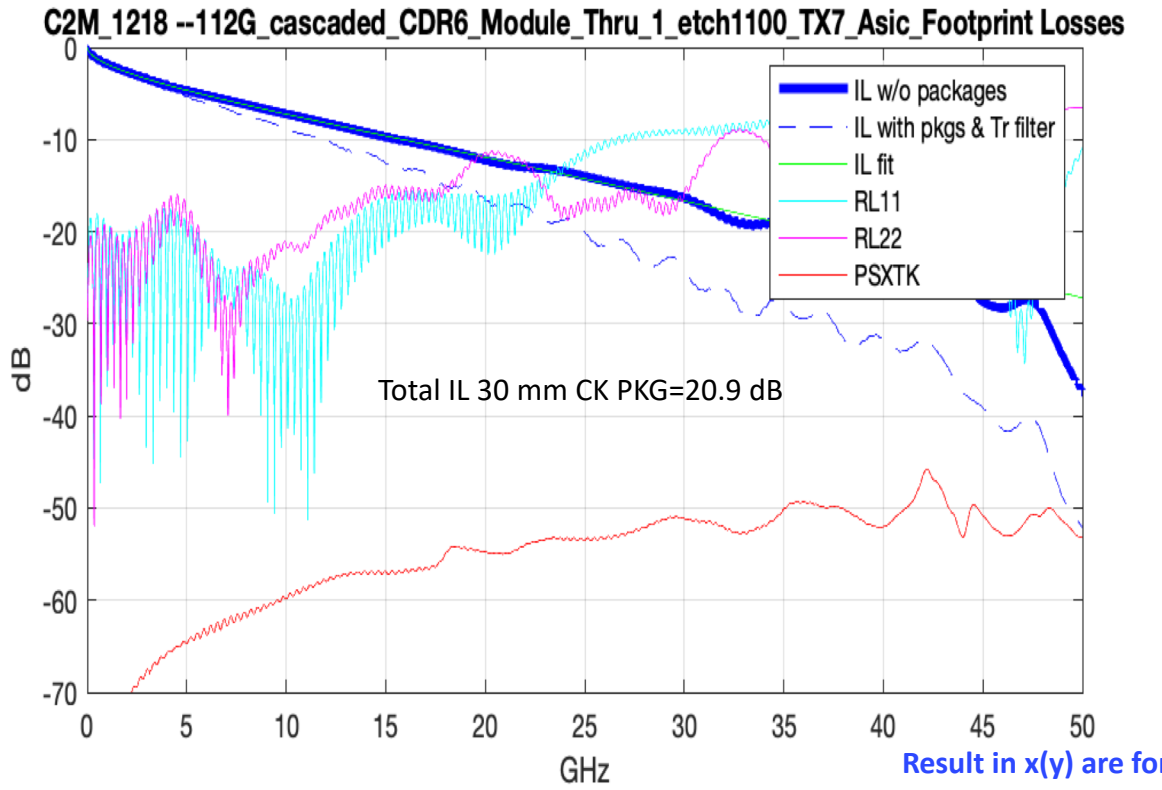


Result in x(y) are for 15(30) mm PKG.

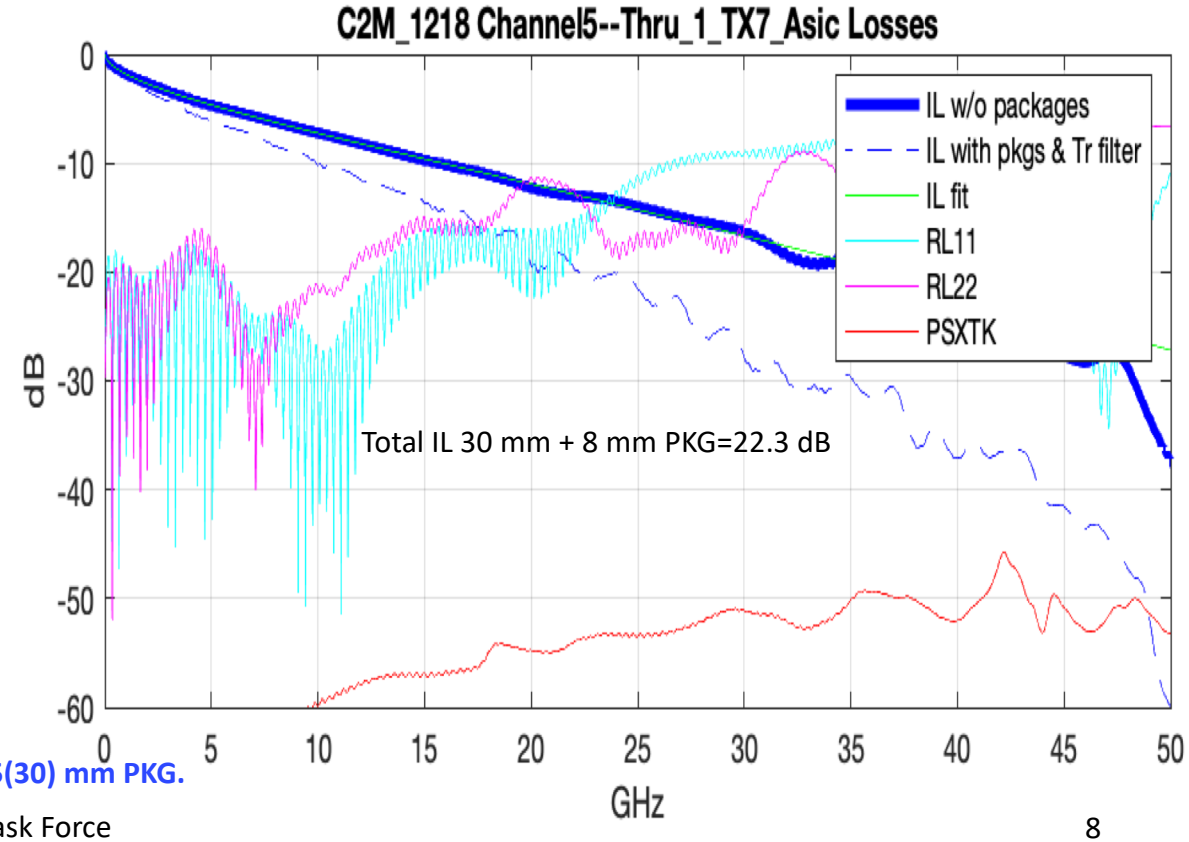
COM Analysis on Lim Channel 5 - ASIC-Module

- **Lim channel 5 QSFP-dd new contact with Legacy QSFP-dd contacts includes ASIC foot print at TP1a and slicer input.**

TP1a, FOM_ILD=0.17, ICN=1.6 mV, ICR=36.8 dB, , ERL11=16.6, ERL22=10.4
5T FFE(4 post): COM=2.7 (4.4) dB, EH=10.4 (11.3) mV, VEC=11.2 (8.0) dB
TX FIR[0.04, -0.18, 0.72, -0.06] Optimum
5T FFE(4 post)+1DFE: COM=4.5 (5.2) dB, EH=19.7 (18.7) mV, VEC=7.8 (6.9) dB
TX FIR[0.04, -0.2, 0.76, 0] Optimum
4DFE: COM=4.2 (4.9) dB, EH=14.1 (14.8) mV, VEC=7.9 (8.4) dB
TX FIR[0.04, -0.2, 0.76, 0] Optimum



Slicer Input, FOM_ILD=0.16, ICN=1.4 mV, ICR=38.2 dB, , ERL11=16.2, ERL22=9.8
5T FFE(4 post): COM=2.1 (1.9) dB, EH=7.0 (4.9) mV, VEC=13.2 (14.1) dB
TX FIR [0.04, -0.18, 0.7, -0.08] Optimum
5T FFE(4 post)+1DFE: COM=4.0 (3.4) dB, EH=16.4 (11.4) mV, VEC=8.9 (9.8) dB
TX FIR[0.02, -0.16, 0.82, 0] Optimum
4DFE: COM=3.7 (3.5) dB, EH=14.1 (11.3) mV, VEC=7.9 (9.6) dB
TX FIR[0.04, -0.2, 0.76, 0] Optimum

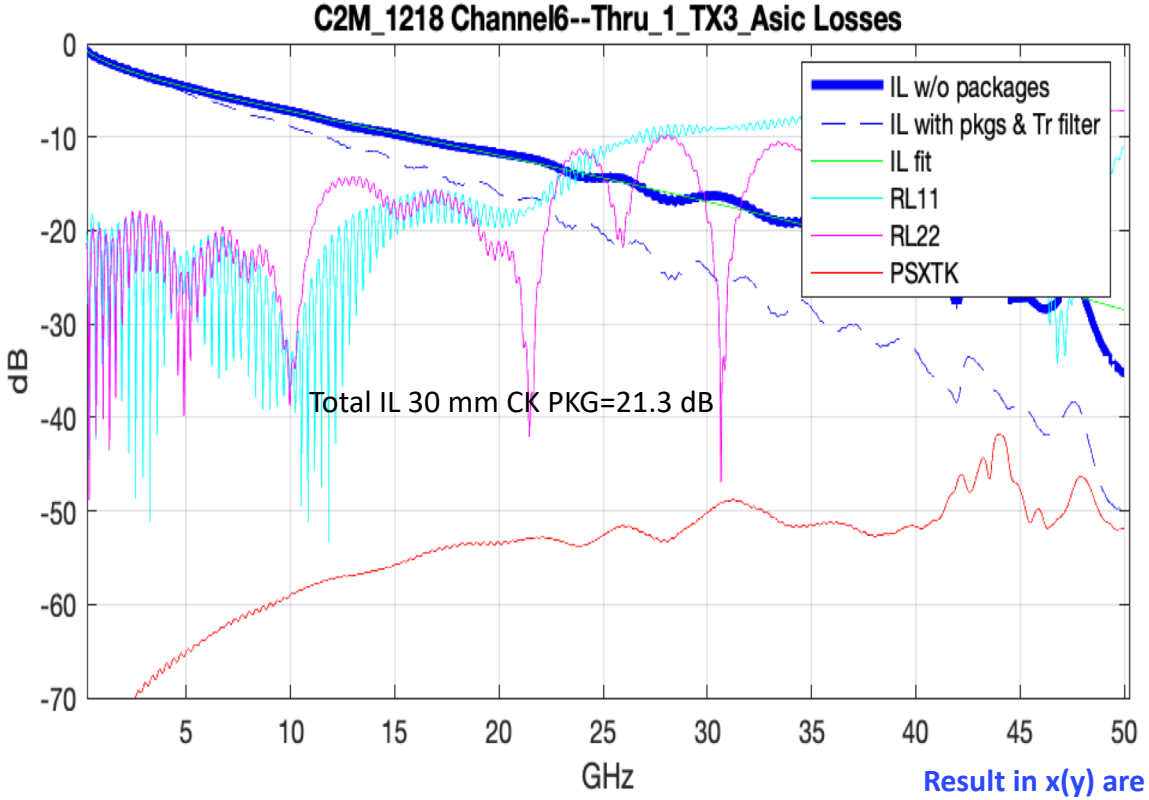


Result in x(y) are for 15(30) mm PKG.

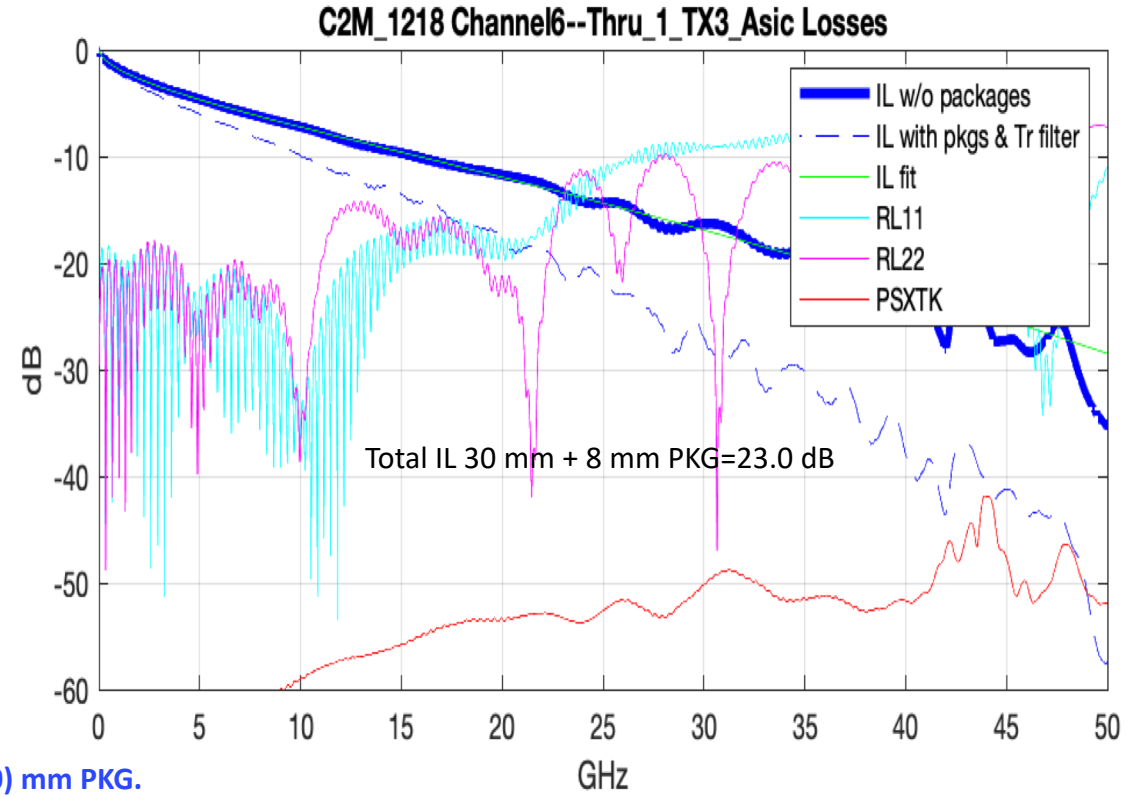
COM Analysis on Lim Channel 6 - ASIC-Module

- **Lim channel 6 both with Legacy QSFP-dd contacts includes ASIC foot print at TP1a and slicer input.**

TP1a, FOM_ILD=0.17, ICN=1.6 mV, ICR=36.8 dB, , ERL11=16.6, ERL22=10.4
5T FFE(4 post): COM=1.7 (4.1) dB, EH=6.2 (9.8) mV, VEC=15.1 (8.5) dB
Optimum TX FIR[0.04, -0.18, 0.7, -0.08]
7T FFE(6 post): COM=4.1 (4.9) dB, EH=18.4 (17.9) mV, VEC=8.4 (7.4) dB
Optimum TX FIR[0.04, -0.2, 0.76, 0]
5T FFE(4 post)+1DFE: COM=4.3 (4.5) dB, EH=14.1 (14.2) mV, VEC=7.9 (8.2) dB
Optimum TX FIR[0.04, -0.18, 0.7, -0.08]



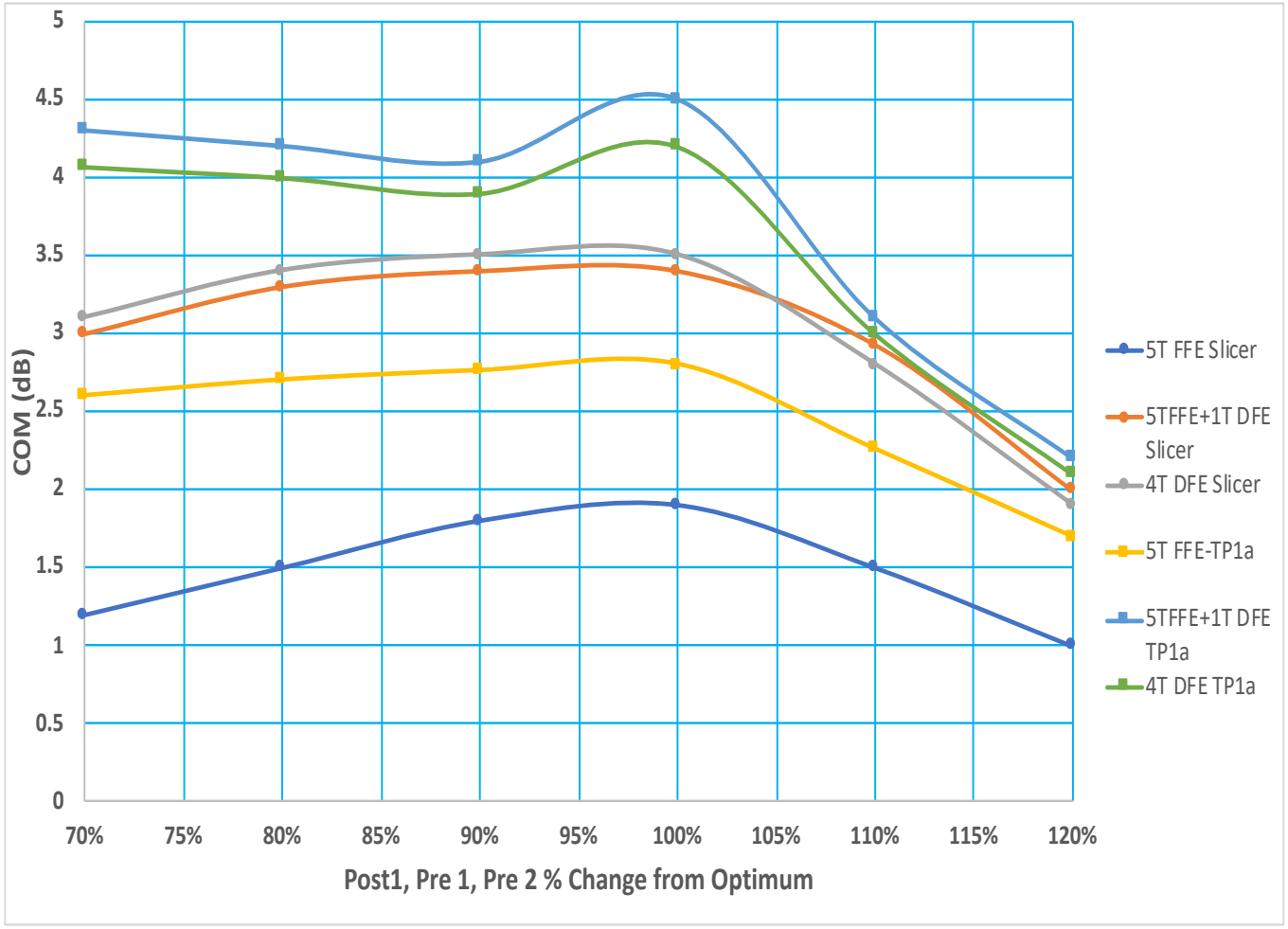
Slicer input, FOM_ILD=0.17, ICN=1.6 mV, ICR=36.8 dB, , ERL11=16.6, ERL22=10.4
5T FFE(4 post): COM=1.4 (3.8) dB, EH=4.3 (8.4) mV, VEC=16.5 (9.0) dB
Optimum TX FIR[0.04, 0.18, 0.7, -0.08]
5T FFE(4 post)+1DFE: COM=3.7 (4.8) dB, EH=19.7 (14.4) mV, VEC=7.8 (7.5) dB
Optimum TX FIR[0.04, -0.2, 0.76, 0]
4DFE: COM=3.5 (4.5) dB, EH=12.0 (13.4) mV, VEC=9.5 (7.9) dB
Optimum TX FIR[0.04, -0.2, 0.76, 0]



Result in x(y) are for 15(30) mm PKG.

COM Sensitivity Analysis as Function of TX FIR @ Module CDR Slicer Input

- **Lim channel 5 with ASIC package foot print**
  - COM results are for worst package combinations
- **Optimum TX FFE at TP1a**
  - 5T TX FFE [0.04, -0.18, 0.72, -0.06]
  - 5T FFE+1T DFE [0.04, -0.2, 0.76, 0]
  - 4T DFE [0.04, -0.2, 0.76, 0]
- **Optimum TX FFE at slicer**
  - 5T TX FFE FIR [0.04, -0.18, 0.7, -0.08]
  - 5T FFE+1T DFE [0.02, -0.16, 0.82, 0]
  - 4T DFE [0.04, -0.2, 0.76, 0]



COM 2.5.8 Module to Host TP5 (CDR PKG 2-8 mm)

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5]	Ohm
C_d	[0.85e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
z_p select	[1 2]		[test cases to run]		Port Order	[2 4 1 3]			Table 92–12 parameters		
z_p (TX)	[2 8]	mm	[test cases]		RUNTAG	C2M_1218			Parameter	Setting	
z_p (NEXT)	[2 8]	mm	[test cases]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (FEXT)	[2 8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (RX)	[0 0]	mm	[test cases]		COM Pass threshold	1	dB		board_Z_c	90	Ohm
C_p	[0.87e-4 0]	nF	[TX RX]		ERL Pass threshold	5	dB		z_bp (TX)	50	mm
R_0	50	Ohm			DER_0	1.00E-05			z_bp (NEXT)	50	mm
R_d	[45 50]	Ohm	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	50	mm
A_v	0.41	V			FORCE_TR	1	logical		z_bp (RX)	0	mm
A_fe	0.41	V			Include PCB	0	logical				
A_ne	0.6	V			TDR and ERL options						
L	4				TDR	1	logical				
M	32				ERL	1	logical				
filter and Eq					ERL_ONLY	0	logical				
f_r	0.75	*fb			TR_TDR	0.01	ns				
c(0)	0.65		min		N	300					
c(-1)	[-0.2:0.02:0]		[min:step:max]	0.7	TDR_Butterworth	1	logical				
c(-2)	[0:.02:0.1]		[min:step:max]		beta_x	1.70E+09					
c(1)	[-0.1:0.02:0]		[min:step:max]		rho_x	0.18					
N_b	4	UI			fixture delay time	0					
b_max(1)	0.5				TDR_W_TXPKG	1					
b_max(2..N_b)	0.2				N_bx	4	UI				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Receiver testing						
f_z	18.55345912	GHz			RX_CALIBRATION	0	logical				
f_p1	53.1	GHz			Sigma BBN step	5.00E-03	V				
f_p2	28.2	GHz									
g_DC_HP	[-3:0.5:-1]		[min:step:max]		Noise, jitter						
f_HP_PZ	1.3275	GHz			sigma_RJ	0.01	UI				
ffe_pre_tap_len	0	UI			A_DD	0.02	UI				
ffe_post_tap_len	0	UI			eta_0	8.20E-09	V^2/GHz				
ffe_tap_step_size	0				SNR_TX	33	dB				
ffe_main_cursor_min	0.7				R_LM	0.95					
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.15										
ffe_backoff	1										

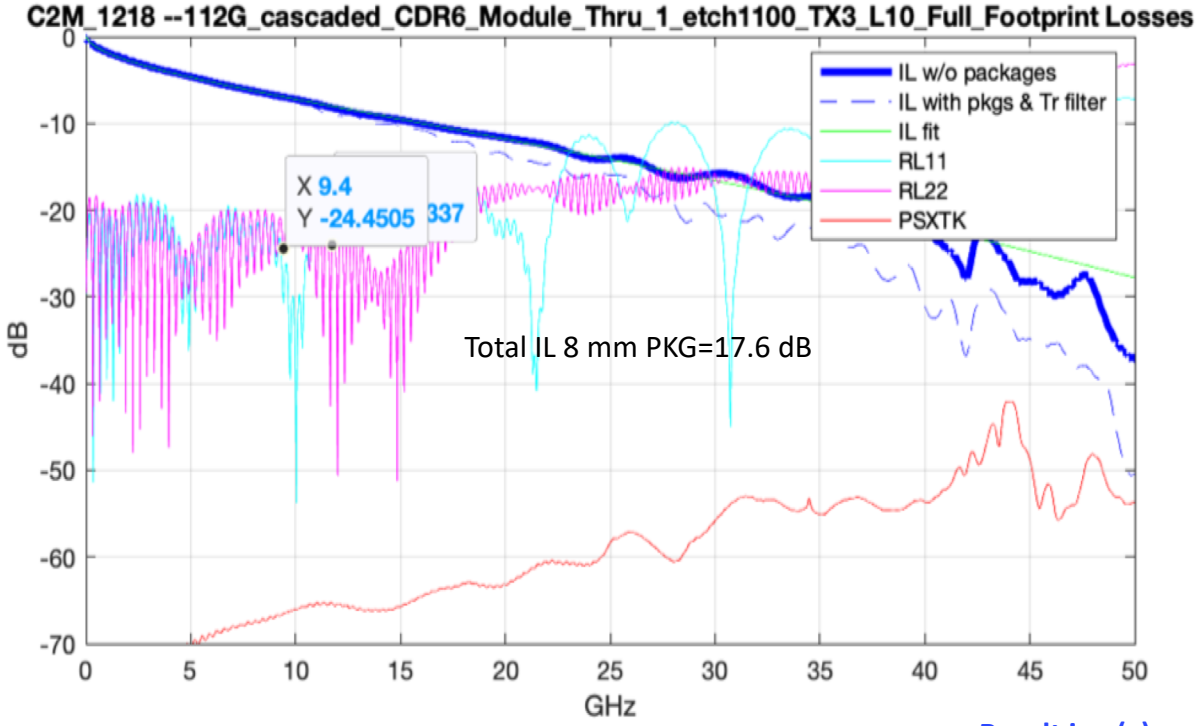
COM 2.5.8 Module to Host Slicer Input (CDR PKG 2-8 mm)

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5]	Ohm
C_d	[0.85e-4 1.1e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
z_p select	[1 2]		[test cases to run]		Port Order	[2 4 1 3]			Table 92–12 parameters		
z_p (TX)	[2 8]	mm	[test cases]		RUNTAG	C2M_1218			Parameter	Setting	
z_p (NEXT)	[2 8]	mm	[test cases]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (FEXT)	[2 8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (RX)	[15 30]	mm	[test cases]		COM Pass threshold	1	dB		board_Z_c	90	Ohm
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]		ERL Pass threshold	5	dB		z_bp (TX)	50	mm
R_0	50	Ohm			DER_0	1.00E-05			z_bp (NEXT)	50	mm
R_d	[45 45]	Ohm	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	50	mm
A_v	0.41	V			FORCE_TR	1	logical		z_bp (RX)	0	mm
A_fe	0.41	V			Include PCB	0	logical				
A_ne	0.6	V			TDR and ERL options						
L	4				TDR	1	logical				
M	32				ERL	1	logical				
filter and Eq					ERL_ONLY	0	logical				
f_r	0.75	*fb			TR_TDR	0.01	ns				
c(0)	0.65		min		N	300					
c(-1)	[-0.2:0.02:0]		[min:step:max]	0.8	TDR_Butterworth	1	logical				
c(-2)	[0:.02:0.1]		[min:step:max]		beta_x	1.70E+09					
c(1)	[-0.1:0.02:0]		[min:step:max]		rho_x	0.18					
N_b	0	UI			fixture delay time	0					
b_max(1)	0.5				TDR_W_TXPKG	1					
b_max(2..N_b)	0.2				N_bx	4	UI				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Receiver testing						
f_z	18.55345912	GHz			RX_CALIBRATION	0	logical				
f_p1	53.1	GHz			Sigma BBN step	5.00E-03	V				
f_p2	28.2	GHz									
g_DC_HP	[-3:0.5:-1]		[min:step:max]		Noise, jitter						
f_HP_PZ	1.3275	GHz			sigma_RJ	0.01	UI				
ffe_pre_tap_len	0	UI			A_DD	0.02	UI				
ffe_post_tap_len	4	UI			eta_0	8.20E-09	V^2/GHz				
ffe_tap_step_size	0				SNR_TX	33	dB				
ffe_main_cursor_min	0.7				R_LM	0.95					
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.2										
ffe_backoff	1										

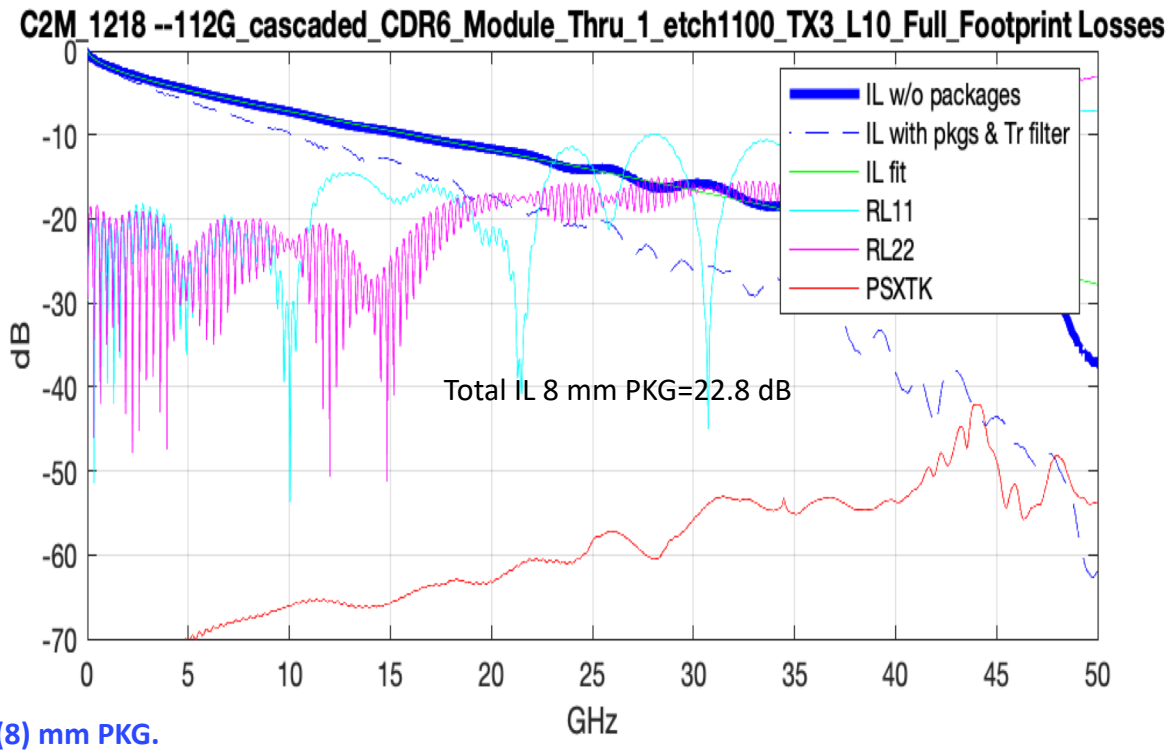
COM Analysis on Lim Channel3 – Module to ASIC TP5

- **Lim channel 3 (short via) Legacy QSFP-dd contacts include retimer foot print at TP5 and slicer input**

TP5, FOM_ILD=0.2, ICN=0.77 mV, ICR=43 dB, ERL11=10.8, ERL22=15.2
5T FFE: COM=5.4 (5.5) dB, EH=20.1 (20.1) mV, VEC=6.3 (6.7) dB
TX FFE [0.02, -0.14, 0.8, -0.04] Optimum
5T FFE+1DFE: COM=6.1 (5.8) dB, EH=30.0 (26.9) mV, VEC=5.9 (6.2) dB
TX FFE[0.02, -0.14, 0.84,0] Optimum
4T DFE: COM=5.9 (5.9) dB, EH=28.6 (27.2) mV, VEC=5.9 (6.1) dB
TX FFE[0.02, -0.14, 0.82,-0.02] Optimum



Slicer Input, FOM_ILD=0.2, ICN=0.77 mV, ICR=43 dB, ERL11=10.8, ERL22=15.2
5T FFE: COM=3.7 (4.1) dB, EH=10.0 (10.3) mV, VEC=9.2 (8.6) dB
TX FFE [0.04, -0.18, 0.74, -0.04] Optimum
5T FFE+1T DFE: COM=4.6 (4.3) dB, EH=19.9 (17.8) mV, VEC=7.7 (8.1) dB
TX FFE[0.04, -0.2, 0.72,-0.04] Optimum
4T DFE: COM=4.6 (4.3) dB, EH=19.9 (17.8) mV, VEC=7.7 (8.1) dB
TX FFE[0.04, -0.2, 0.72,-0.04] Optimum

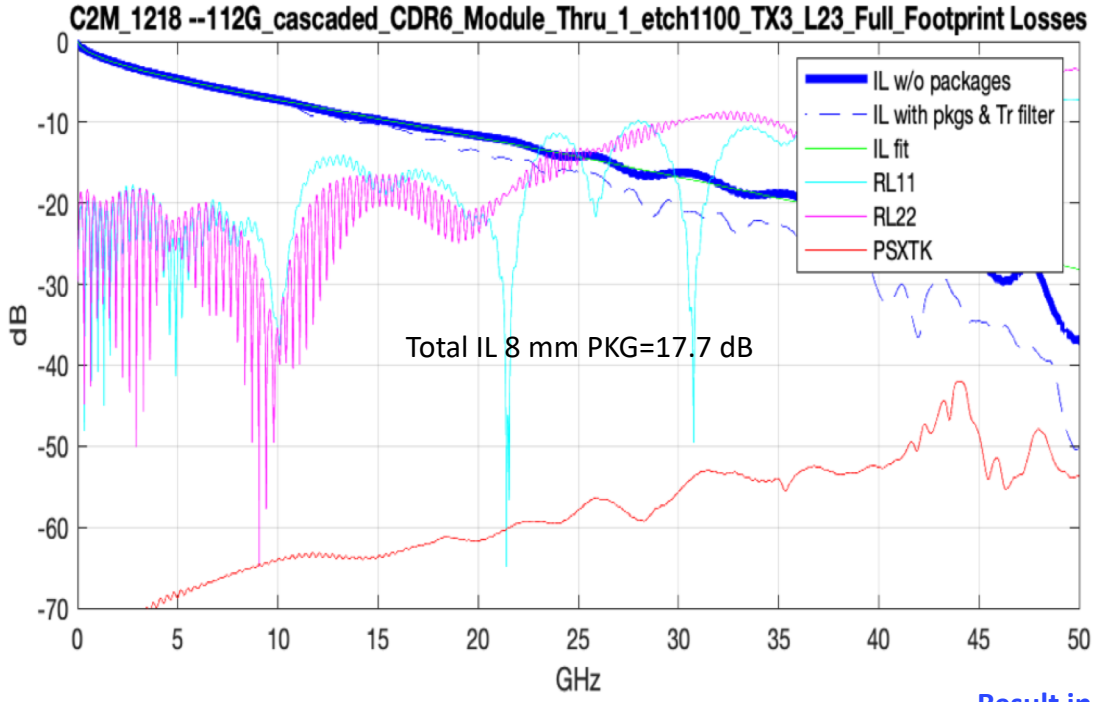


Result in x(y) are for 2(8) mm PKG.

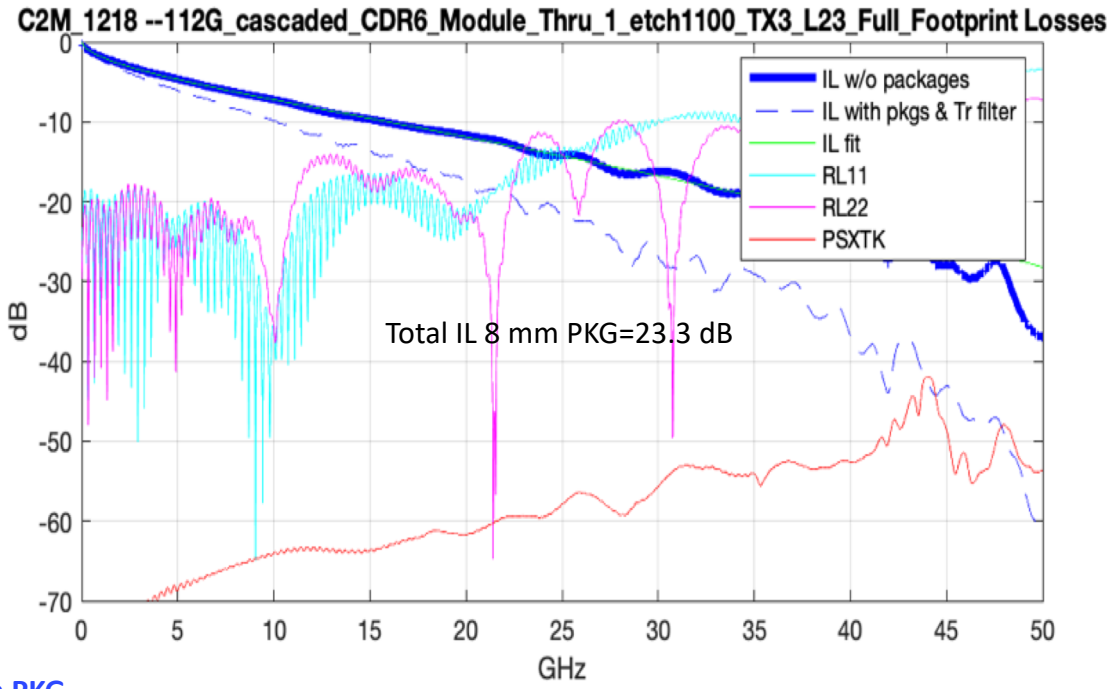
COM Analysis on Lim Channel 4 – Module to ASIC

- **Lim channel 4 (long via) Legacy QSFP-dd contact include retimer foot print at TP5 and slicer input**

TP5, FOM_ILD=0.18, ICN=0.85 mV, ICR=42 dB, ERL11=10.7, ERL22=14.5
5T FFE(4 post) TP5: COM=5.7 (5.4) dB, EH=20.1 (19.4) mV, VEC=6.3 (6.7) dB
TX FFE [0.02, -0.14, 0.76, -0.08] Optimum
5T FFE(4 post) : COM=6.0 (5.8) dB, EH=29.2 (26.6) mV, VEC=6.1 (6.2) dB
TX FFE [0.02, -0.14, 0.82, -0.02] Optimum
4T DFE: COM=5.1 (5.1) dB, EH=26.7 (26.0) mV, VEC=6.2 (6.2) dB
TX FFE[0.02, -0.14, 0.82,-0.02]



Slicer Input, FOM_ILD=0.18, ICN=0.85 mV, ICR=42 dB, ERL11=10.7, ERL22=14.5
5T FFE(4 post): COM=3.11 (3.9) dB, EH=8.1 (9.6) mV, VEC=10.4 (8.8) dB
TX FFE [0.04, -0.18, 0.74, -0.04] Optimum
5T FFE(4 post): COM=4.1 (3.7) dB, EH=18.2 (15.7) mV, VEC=8.5 (9.1) dB
TX FFE[0.04, -0.2, 0.72,-0.04] Optimum
4T DFE: COM=4.6 (4.3) dB, EH=19.9 (17.8) mV, VEC=7.7 (8.1) dB
TX FFE[0.04, -0.2, 0.72,-0.04] Optimum

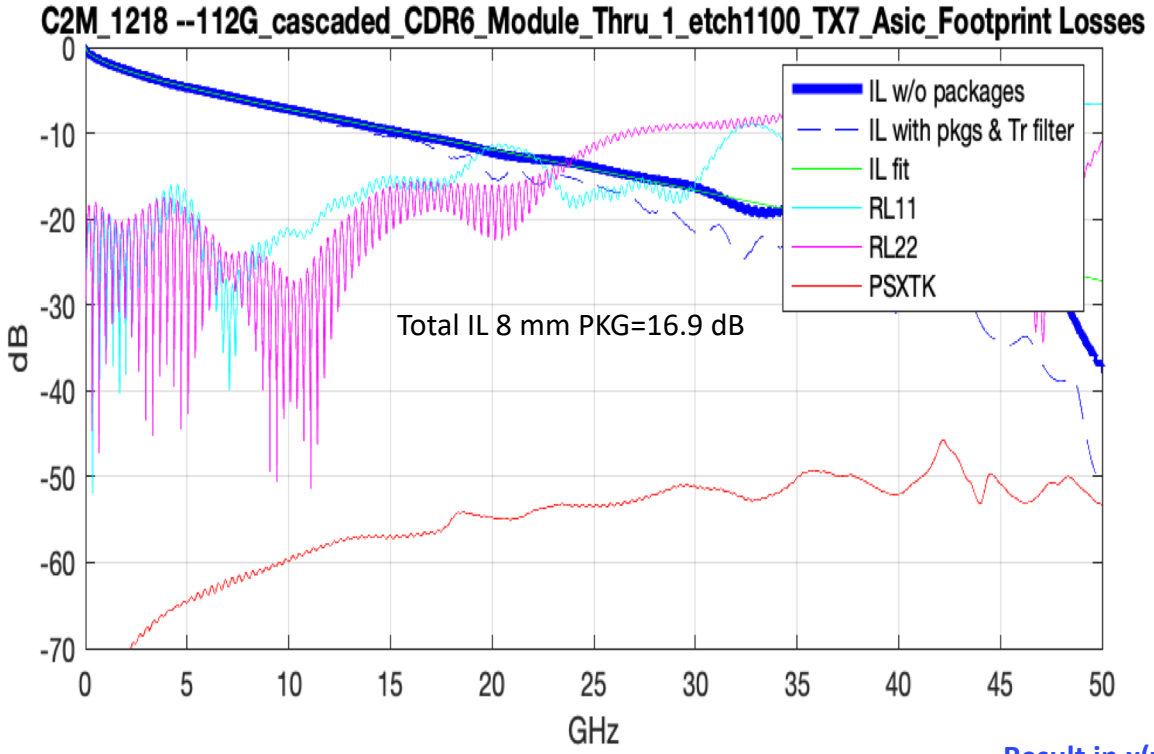


Result in x(y) are for 2(8) mm PKG.

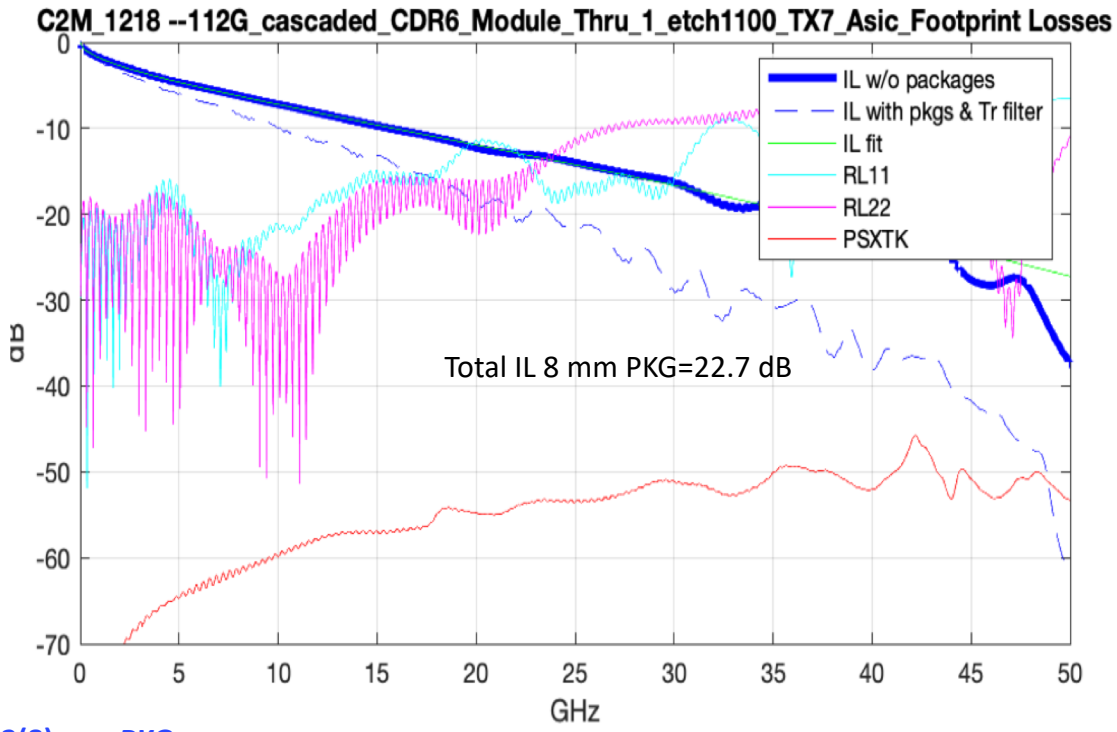
COM Analysis on Lim Channel 5 – Module to ASIC

- **Lim channel 5 QSFP-dd new contact includes ASIC foot print at TP5 and slicer input**

TP5, FOM_ILD=0.2, ICN=1.4 mV, ICR=38.2 dB, ERL11=10.2, ERL22=14.8
5T FFE: COM=5.4 (4.0) dB, EH=25.9 (15.5) mV, VEC=6.7 (8.7) dB
TX FFE [0, -0.14, 0.78, -0.1] Optimum
5T FFE+1T DFE: COM=5.7 (4.9) dB, EH=26.8 (24.2) mV, VEC=6.4 (7.2) dB
TX FFE[0.02, -0.14, 0.84,0] Optimum
4TDFE: COM=5.6 (5.3) dB, EH=26.5 (25.5) mV, VEC=6.5 (6.8) dB
TX FFE[0.02, -0.14, 0.84,0] Optimum



Slicer Input, FOM_ILD=0.2, ICN=1.4 mV, ICR=38.2 dB, ERL11=10.2, ERL22=14.2
5T FFE: COM=1.3 (3.9) dB, EH=3.8 (10.5) mV, VEC=17 (8.7) dB
TX FFE [0.04, -0.14, 0.76, -0.02] Optimum
5T FFE(4 post)+1T DFE: COM=2.8 (4.8) dB, EH=12 (13.5) mV, VEC=11.1(7.4) dB
TX FFE [0.04, -0.18, 0.78, 0] Optimum
4T DFE: COM=2.5 (5.1) dB, EH=10.8 (14.1) mV, VEC=12(7.0) dB
TX FFE [0.04, -0.18, 0.78, 0] Optimum

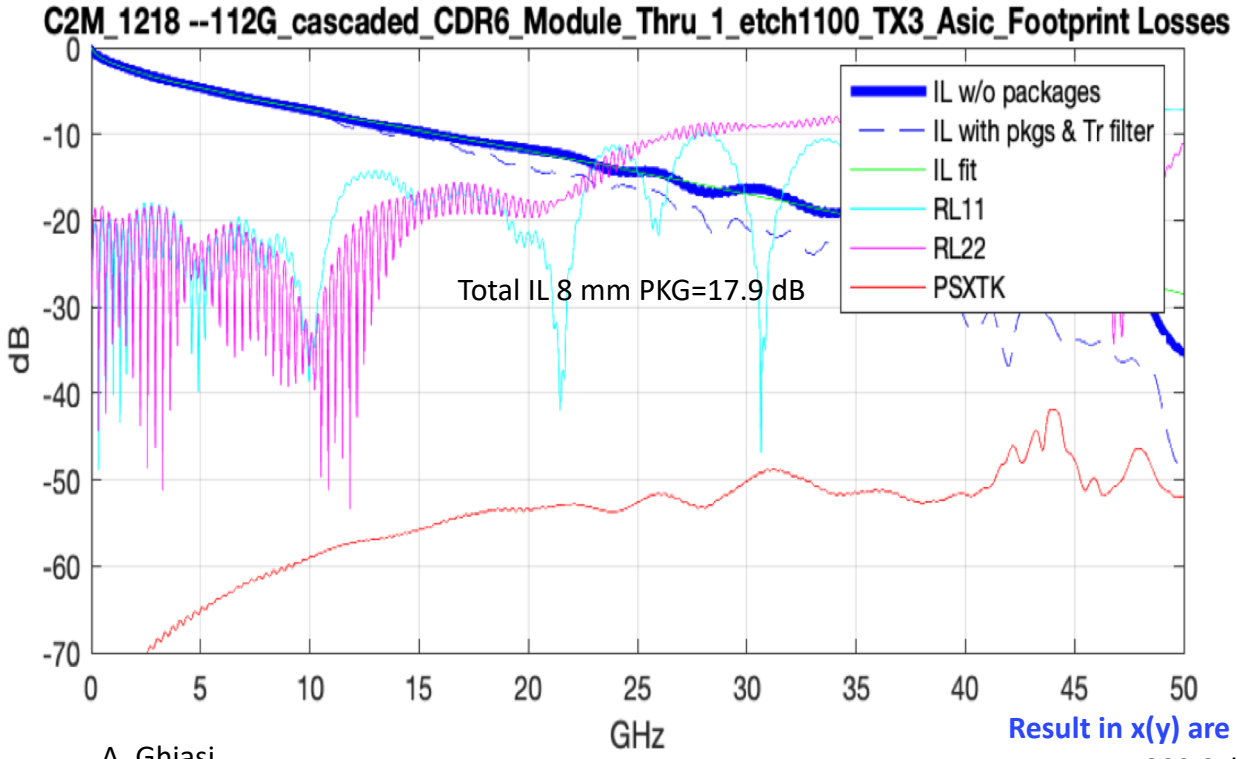


Result in x(y) are for 2(8) mm PKG.

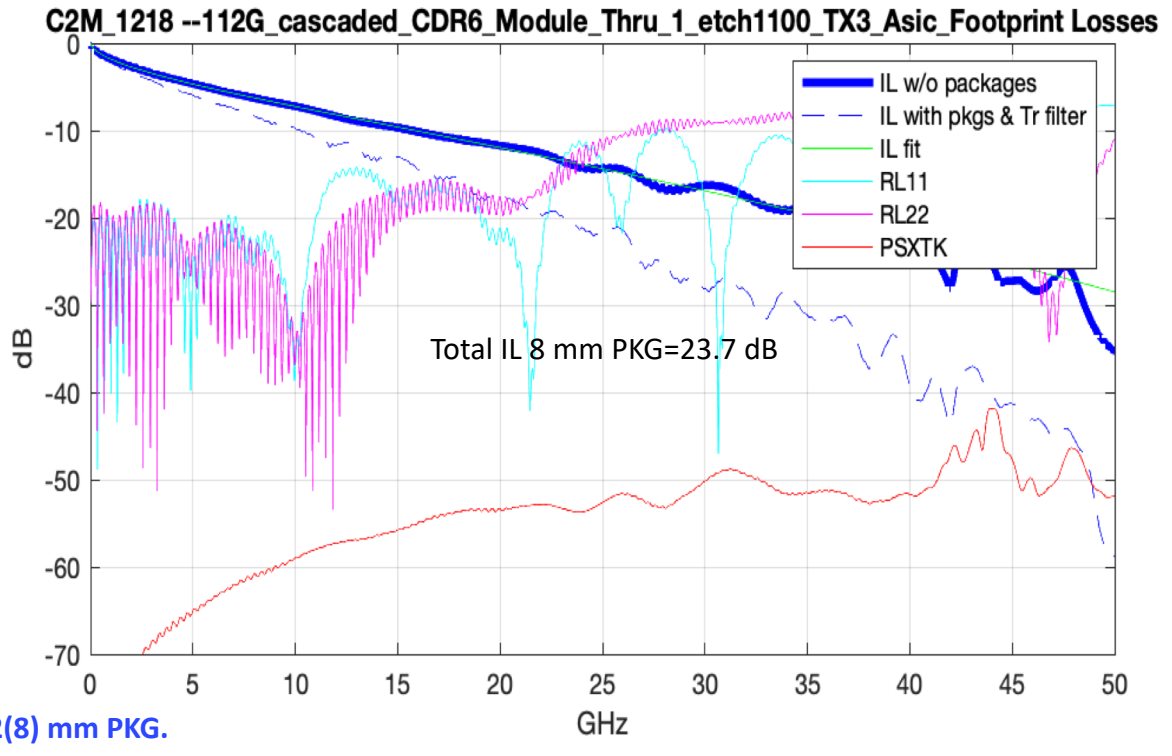
COM Analysis on Lim Channel6 - Module-ASIC

- **Lim channel 6 QSFP-dd Legacy contacts includes ASIC foot print at TP5 and slicer input**

TP5, FOM_ILD=0.17, ICN=1.56 mV, ICR=36.8 dB, ERL11=10.2, ERL22=15.2
5T FFE(4 post): COM=5.2 (5.0) dB, EH=16.8 (22.5) mV, VEC=6.9 (7.1) dB
TX FFE [0.04, -0.18, 0.78, 0] Optimum
5T FFE(4 post): COM=5.5 (5.5) dB, EH=24.7 (24.4) mV, VEC=6.5 (6.6) dB
TX FFE[0.04, -0.18, 0.78,0] Optimum
4TDFE: COM=5.4 (5.6) dB, EH=25.7 (25.0) mV, VEC=6.7 (6.5) dB
TX FFE[0.04, -0.18, 0.78,0] Optimum



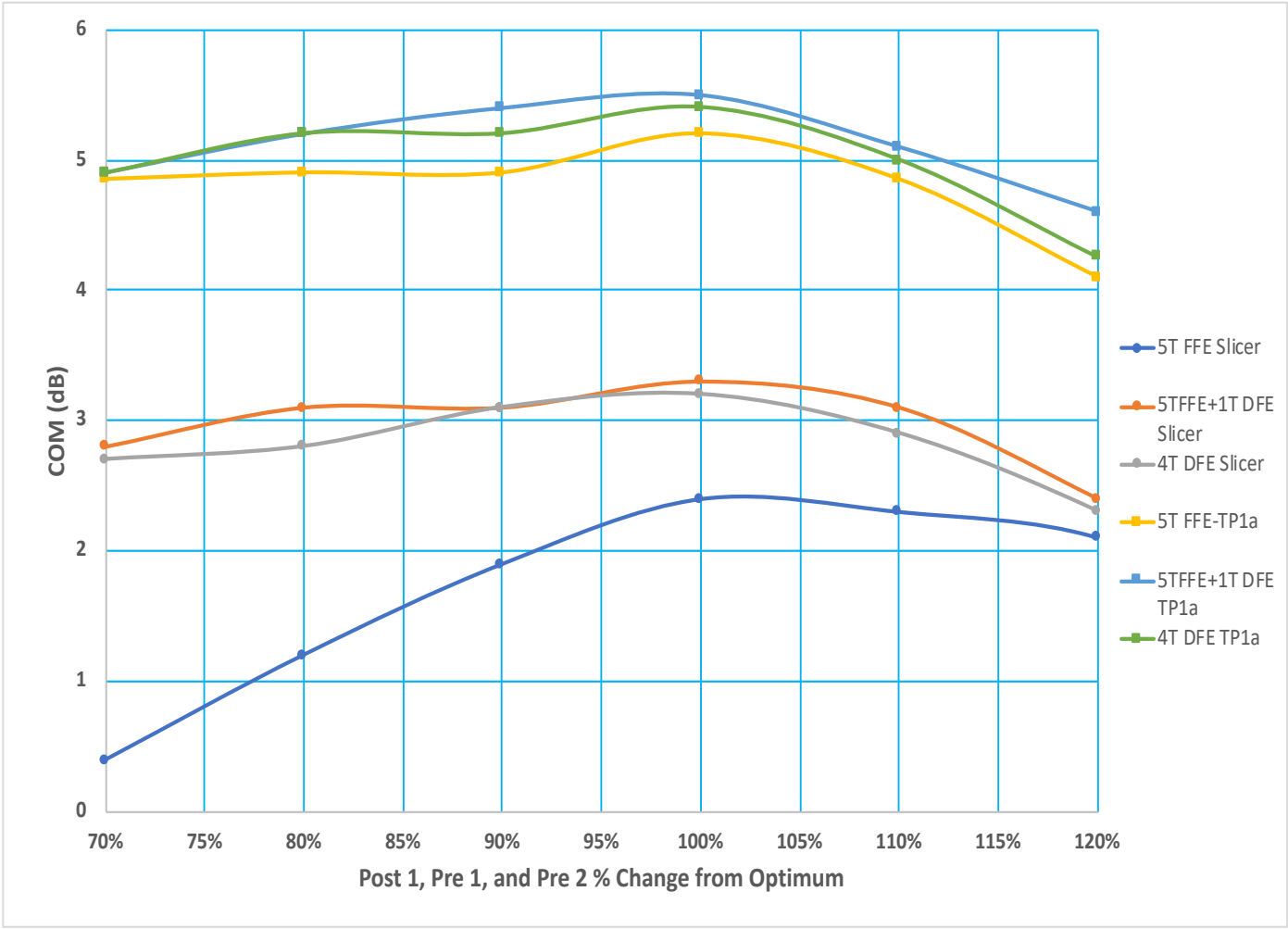
Slicer Input, FOM_ILD=0.17, ICN=1.56 mV, ICR=36.8 dB, ERL11=10.8, ERL22=15.2
5T FFE(4 post): COM=2.4 (3.8) dB, EH=6.4 (8.6) mV, VEC=12.3 (9.1) dB
TX FFE [0.04, -0.18, 0.72, -0.06] Optimum
5T FFE(4 post)+1T DFE: COM=3.3 (3.5) dB, EH=13.4 (13.7) mV, VEC=10.1 (7.9) dB
TX FFE [0.04, -0.2, 0.76, 0] Optimum
4T DFE: COM=3.2 (4.4) dB, EH=12.7 (13.1) mV, VEC=10.2(8.1) dB
TX FFE [0.04, -0.2, 0.76, 0] Optimum



Result in x(y) are for 2(8) mm PKG.

COM Sensitivity Analysis as Function of TX FIR @ ASIC Slicer Input

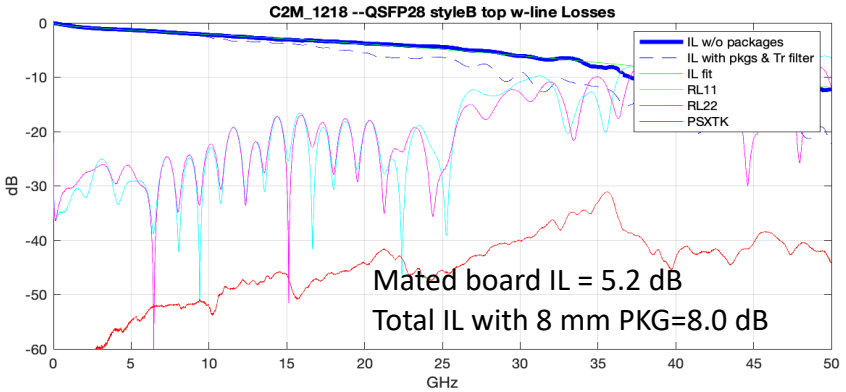
- **Lim channel 6 with ASIC package foot print**
  - COM results are for worst package combinations and [2,8] mm
- **Optimum TX FFE at TP1a**
  - 5T TX FFE [0.04, -0.18, 0.72, -0.06]
  - 5T FFE+1T DFE [0.04, -0.2, 0.76, 0]
  - 4T DFE [0.04, -0.2, 0.76, 0]
- **Optimum TX FFE at slicer**
  - 5T TX FFE FIR [0.04, -0.18, 0.7, -0.08]
  - 5T FFE+1T DFE [0.02, -0.16, 0.82, 0]
  - 4T DFE [0.04, -0.2, 0.76, 0]

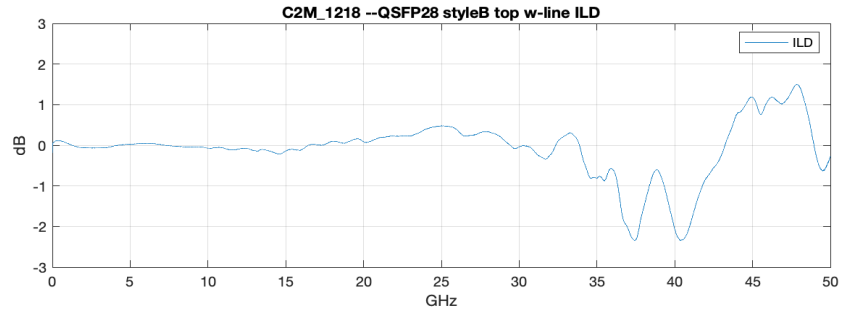


TP4/TP5 Analysis with Yamaichi QSFP-56 Mated Boards

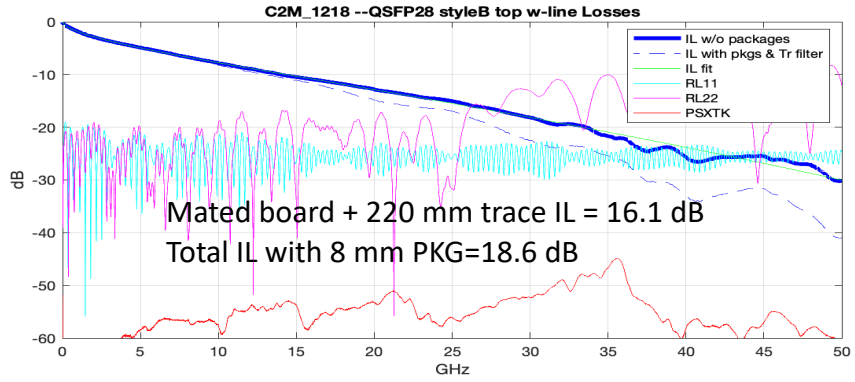
- **COM improves by 1+ dB at TP5 compare to TP4!**
  - A 5T FFE+1DFE or 4T DFE reference EQ at TP4/TP5 may allow modules that should fail pass in turn requiring even stronger host EQ.

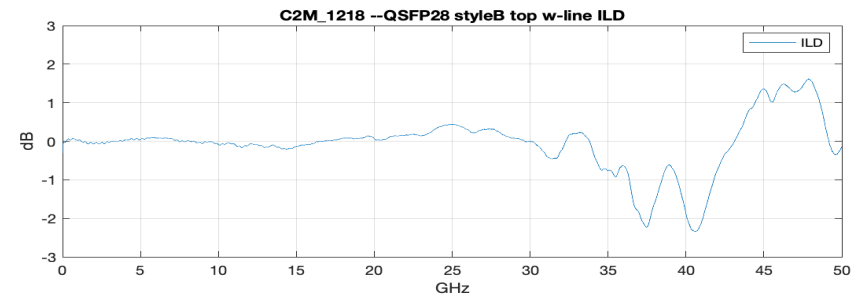
TP4, FOM_ILD=0.18, ICN=5.2 mV, ICR=39.5 dB, ERL11=14.6, ERL22=10.7
5T FFE(4 post): COM=5.7 (4.9) dB, EH=51.5 (46.4) mV, VEC=6.3 (7.3) dB
TX FFE [0.02, -0.14, 0.8, -0.04] Optimum
5T FFE(4 post): COM=5.1 (4.5) dB, EH=54.2 (45.8) mV, VEC=7.2 (7.8) dB
TX FFE [0.02, -0.14, 0.84, 0] Optimum
4T DFE: COM=5.1 (4.5) dB, EH=53.1 (45.6) mV, VEC=7.1 (7.9) dB
TX FFE [0.02, -0.14, 0.82, 0] Optimum





TP5, FOM_ILD=0.17, ICN=1.6 mV, ICR=39.1 dB, ERL11=14.6, ERL22=10.7
5T FFE(4 post): COM=6.6 (6.3) dB, EH=19.3 (20.9) mV, VEC=5.5 (5.8) dB
TX FFE [0.04, -0.18, 0.76, -0.02] Optimum
5T FFE(4 post): COM=6.7 (6.8) dB, EH=25.1 (26.0) mV, VEC=5.4 (5.3) dB
TX FFE [0.04, -0.2, 0.76, 0] Optimum
4T DFE: COM=6.7 (6.6) dB, EH=26.5 (24.0) mV, VEC=5.4 (5.5) dB
TX FFE [0.04, -0.18, 0.78, 0] Optimum





Why FFE Is Preferred Reference Equalizer

- **All 802.3bs and 802.3cd PAM4 PMDs require 5 tap T spaced FFE with up to 2 pre-cursor taps**
  - 4 tap DFE flatly fails as an optics receiver
  - Every optics CDR already has ≥ 5 tap FFE and possibly one tap DFE
  - Clause 121.8.5.4 defines TDECQ reference equalizer as a 5 tap, T spaced, feed-forward equalizer (FFE)
- **It has been raised that zero forcing DFE in COM is easier to adapt**
  - COM is not a normative requirement of C2M
  - The normative C2M test will be performed on scopes at TP1a and TP4/TP5 measuring EW and EH
  - Keysight and Tek both have developed TDECQ scope algorithm already based on 5 tap FFE
  - Reusing 5 tap FFE for electrical test is trivial
- **Why not duplicate the optics CDR core with 5 tap FFE (+ 1T DFE?) on the electrical side?**
- **Real use for 100G/lane AUI will be 800G modules where PD is critical 5 Tap FFE+1DFE offer more flexible architecture where 1T DFE is not turned on many channels**
  - Over time may find 1T DFE is not necessary
- **5T FFE or 5T FFE+1T DFE with bmax≤0.5 removes concern with burst error on segmented link**
- **TP1a and TP4/TP5 are observation point to estimate signal quality at slicer**
  - 5T FFE+1T DFE or 4T DFE EQ at TP4/TP5 may allow modules that should fail to pass such that host EQ based on 5T FFE+1T DFE or 4T DFE will fail
  - FFE inherently preserves the analog signal and will provide better direct correlation than a DFE clipped signal!

Summary

- **Summary of Lim 3/19 channels simulations at TP1a/TP5 and at slicer input**
  - The 5 tap FFE+1DFE or 4 tap DFE equalizers cover broader set channels but come at a cost/power
  - COM degradation from TP1a to CDR slicer input is ~0.5 dB given that HCB has additional degradation in practice COM at TP1a and the slicer likely about the same
  - COM degradation from TP5 to ASIC slicer input is ~ 2 dB, based on the limit set at TP5 may end up either with excess margin or negative margin
- **With time the channel/connectors will improve including migration to stubless PCB boards**
  - The 5 tap FFE + 1T DFE offer the option to turn off the DFE on most channels and save power
  - 5 tap FFE + 1T DFE (bmax ≤0.5) has synergy with optics 5T FFE without burst error risk that 4T DFE may have
- **Reference EQ for TP4/TP5 should not be based on 5T FFE+1T DFE or 4T DFE otherwise channel that should fail may pass**
  - 5T FFE is best choice for TP1a and TP4/TP5 observation reference EQ
  - Actual receiver likely will be something more capable
- **C2M TP1, TP4, and TP5 recommended limits based on 5T FFE (4 post) scope reference equalizer**
  - TP1a EH=10 mV, VEC=12 dB, EW=TBD
  - TP4 EH=40 mV, VEC=8 dB, EW=TBD
  - TP5 EH=15 mV, VEC=10 dB, EW=TBD.