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Representing imperfections for CR Host Board

David Katz
Meir Hasko
Liav Ben-Artsi
Marvell Semiconductor Inc.

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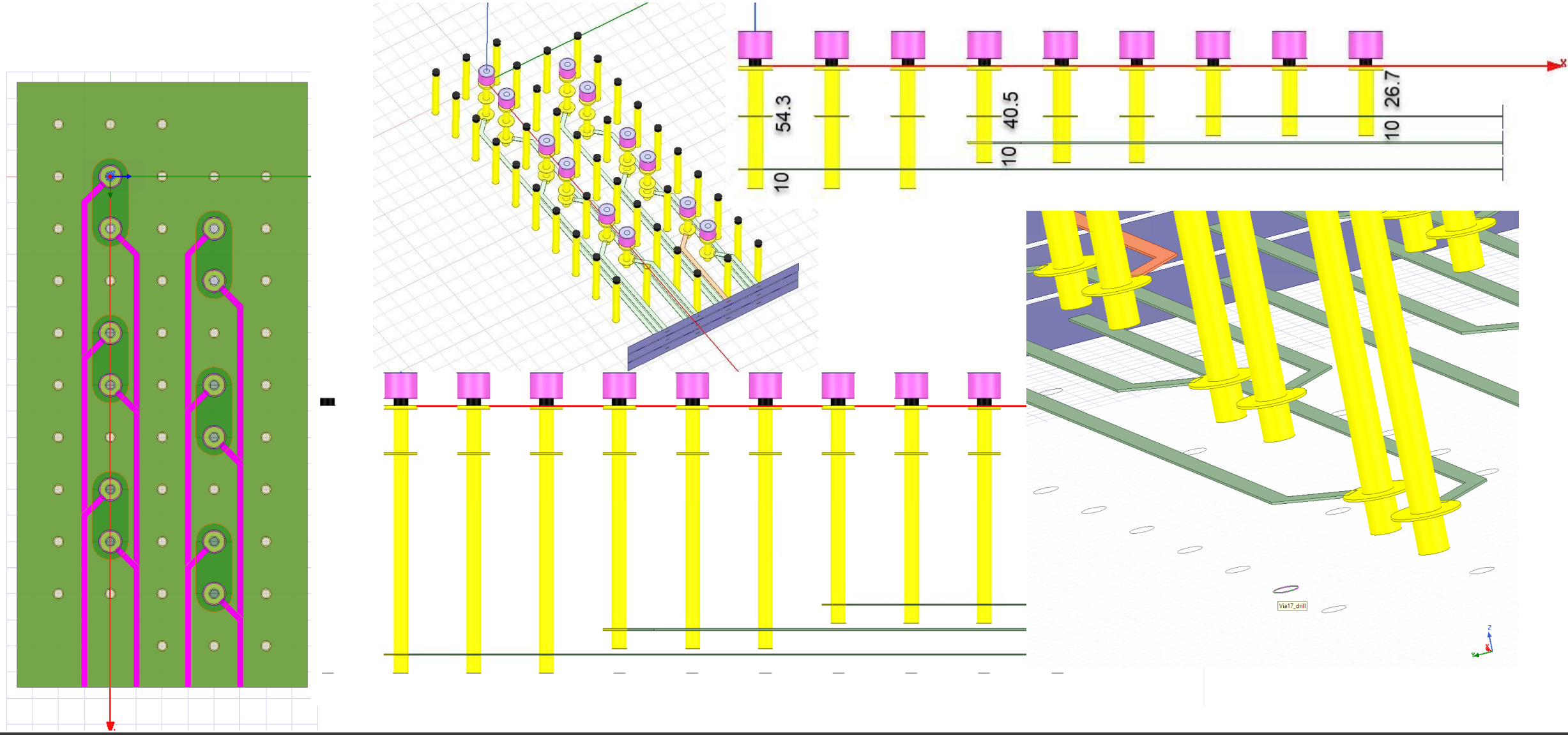
Executive Summary

- Include PCB initial representation was shown to have lower “reflection stamping” in reference to an optimized chip break-out & connector via area
- A “step at the right direction” will be recommended though not fully representing all phenomena
- One of the capacitive discontinuities of BO section and connector via were correlated to 29fF and 19fF respectively and presented during July Vienna Plenary – In a COM run, the resulting COM of capacitive discontinuities was still optimistic relative to BO section extraction by-itself – Correlation was done to the capacitance value rather than COM result – Nevertheless still recommend using this methodology going forward, even though it underestimates the effect on COM
- Crosstalk Tx and Rx sections were extracted and correlated to SNDR& Eta0 values

Models Extraction & Correlation Methodology Specifications

- Ball-out used for extraction was specified by a selected group of 802.3ck participants
- Long via field extracted and put @ Tx section (~2.5mm via + 10mil stub)
- Short via field extracted and put @ Rx section utilizing the upper section of the board stack-up (~1.0mm via with a 10mil stub)
- Swapping via length between Tx & Rx done as well to come up with alternative interconnect constellation
- Runs were done using COM 2.7 on multiple cable interconnects to correlate Tx crosstalk to SNDR effect and Rx crosstalk to Eta0 effect
- 8 lanes are of the same device origin – Is the assumption of no-correlation whatsoever between lanes adequate? Nevertheless was assumed here according to COM methodology to derive SNDR and eta0

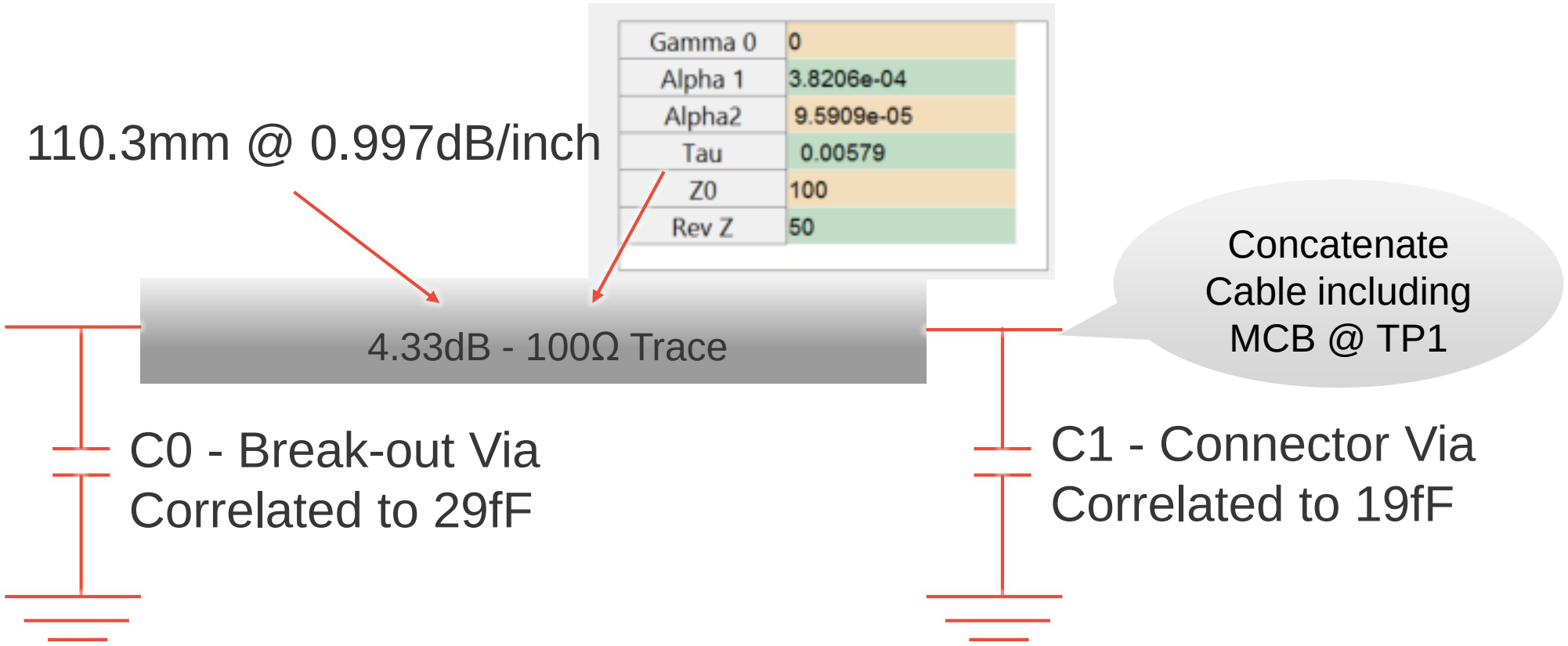
Models Extraction & Correlation Methodology Specifications



Models Extraction & Correlation Methodology Specifications

1. A Through lane(s) was concatenated with Tx and Rx through-break-out sections and run in COM for base-line reference – Baseline COM recorded
2. Breakout Tx crosstalk sections concatenated to the same interconnect(s) + Rx through BO section. COM was run with full ball-out surrounding – Target Crosstalk COM was recorded.
3. Rerun Phase1 with altering SNDR to come up with the Target Crosstalk COM by lowering SNDR – Result = 32.5dB/32.9dB
4. Breakout Tx through section was concatenated to the same interconnect(s) + Rx crosstalk section(s) - COM was run with full ball-out surrounding – Target Crosstalk COM was recorded.
5. Rerun Phase1 with altering ETA0 to come up with the target Crosstalk COM by increasing ETA0 – Result = 8.36e-9/9.35e-9

Model to be Inserted as “Include PCB” - Reminder



Summary, Conclusions, Recommendations & Next Steps

- Optimized break-out section effect on multiple lanes was translated to an updated Tx SNDR value of 32.5dB and Eta0 =8.36E-9 (if aggressors were changed to short, Eta0 =8.69E-9) Recommending using these values for CR COM, or SNDR=32.9 & Eta0= 9.35E-09
- Re-extracting the model with minimal via drill inaccuracy showed no actual effect on correlated SNDR/Eta0
- Resulting SNDR & ETA0 assumed no statistical correlation between aggressor lanes (as is done in COM) – Recommend further analysis if this assumption is appropriate/relevant for multi-lane port and adjust COM and SNDR/Eta0 accordingly.
- Recommend using C0/C1 and trace parameters following slide #6 for “include_PCB” = 1

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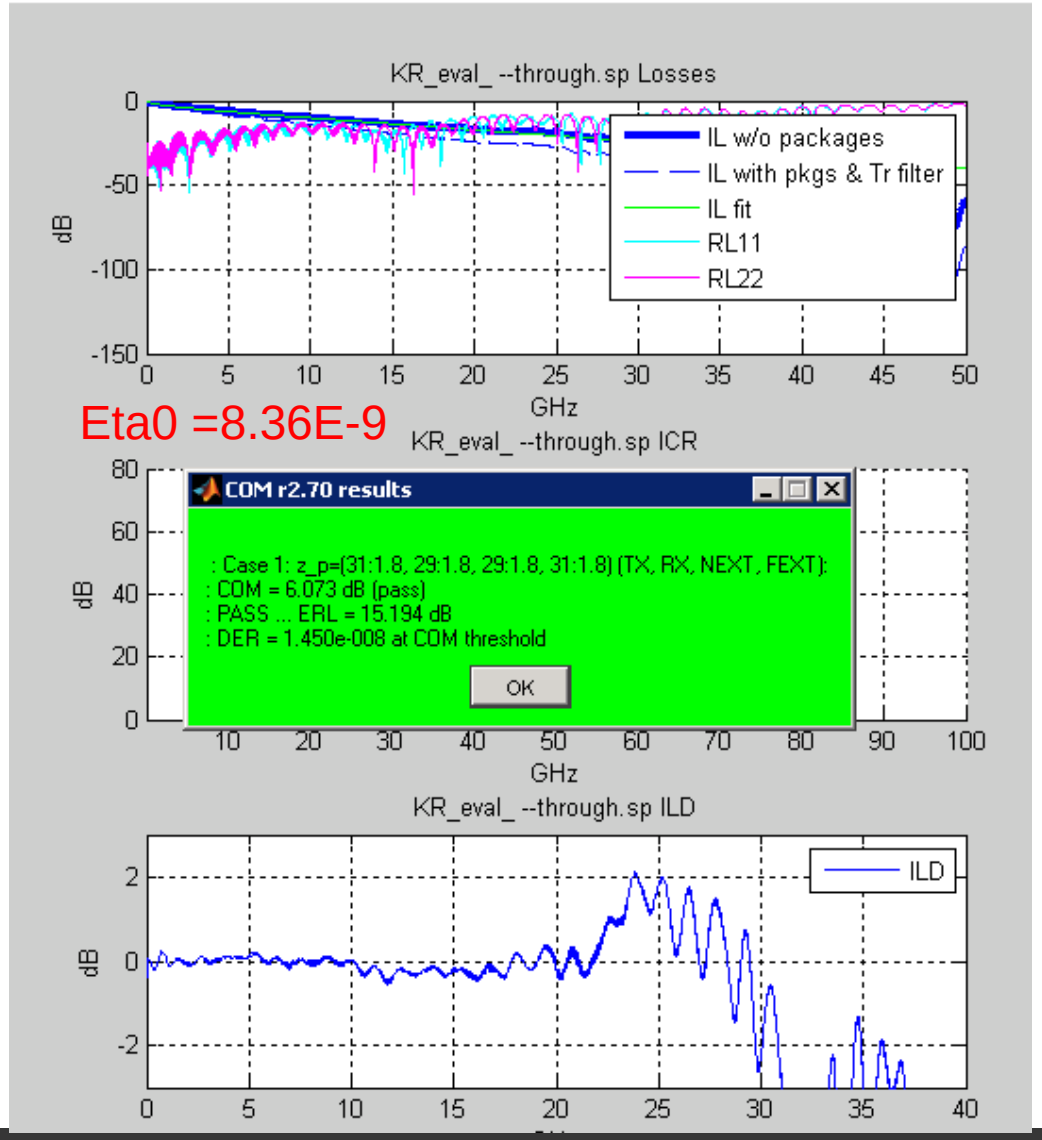
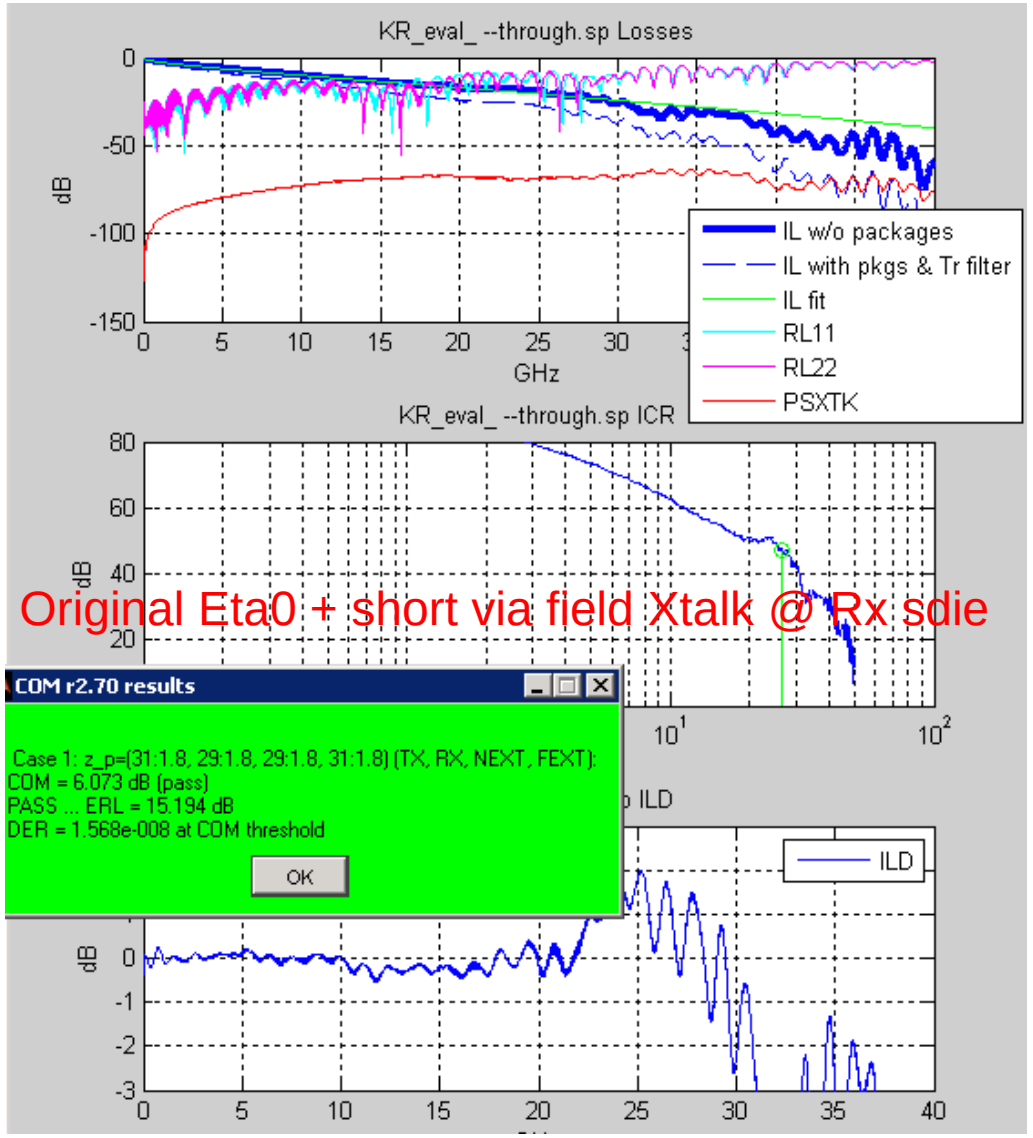
Backup

Two Possible Combination of SNDR/Eta0 according to Current Extraction

Cable	SNDR	Eta0	COM
P1_Tx4	32.5	8.36E-09	3.479
P1_Tx4	32.9	9.35E-09	3.363
P2_Tx3	32.5	8.36E-09	3.863
P2_Tx3	32.9	9.35E-09	3.742

Rx Short Via Eta0 Correlation Test Example





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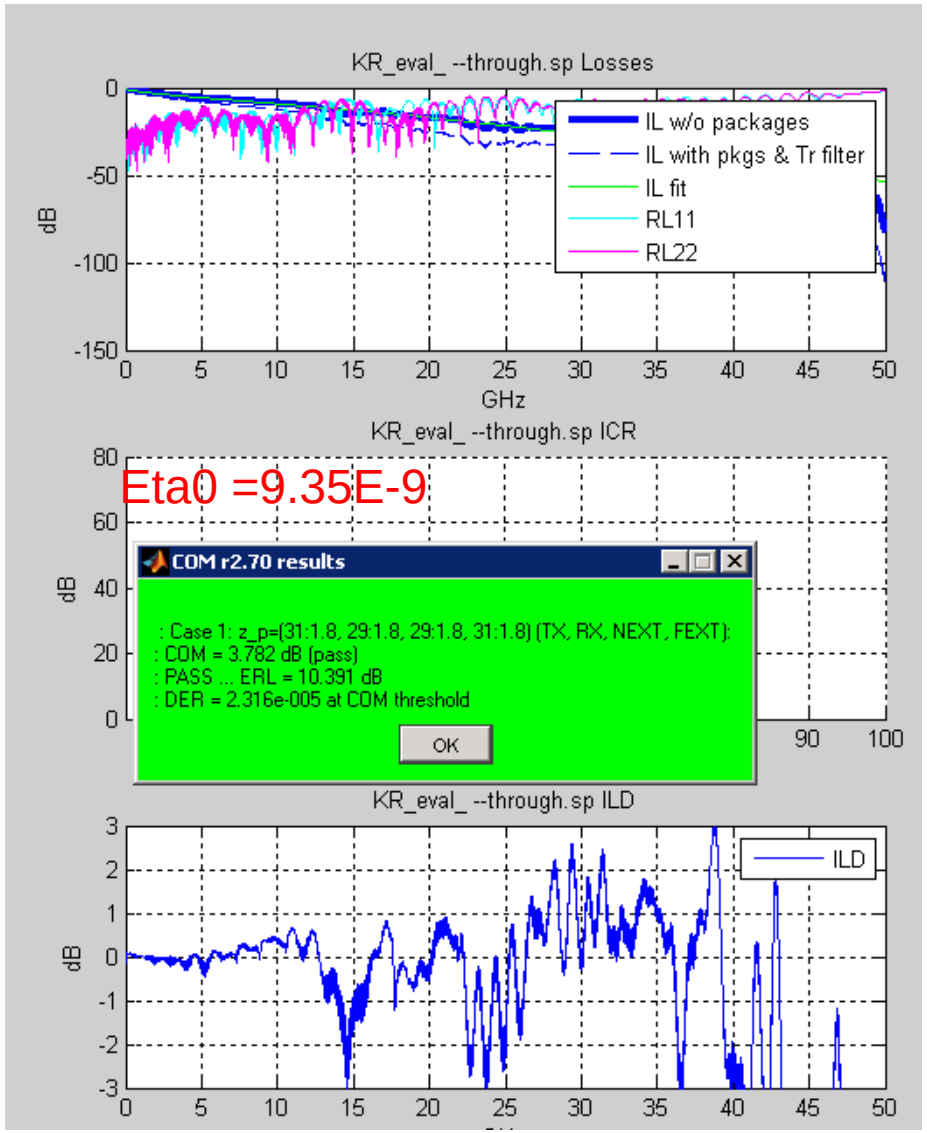
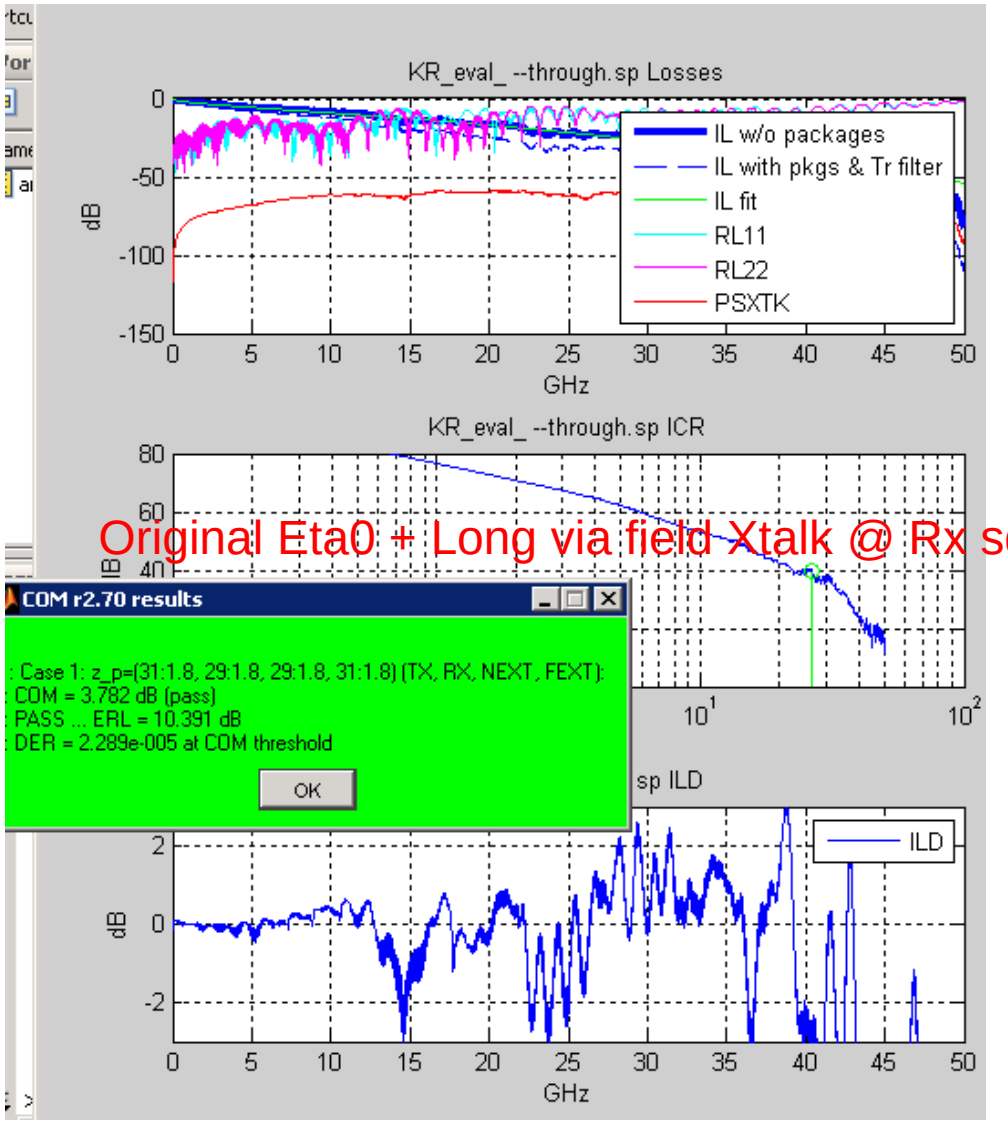
Rx Long Via Correlation Example





COM Spread-Sheet

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]
L_s	[0.12, 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[2]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX]
A_v	0.39	V	vp/vf=.694
A_fe	0.39	V	vp/vf=.694
A_ne	0.578	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.5		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02: 0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	12	UI	
b_max(1)	0.85		
b_max(2..N_b)	0.3		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_[date]	
SAVE_FIGURES	1	logical
Port Order	[1 2 3 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-04	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3000	
beta_x	2.53E+09	
rho_x	**0.25**	
fixture delay time	0	s
TDR_W_TXPKG	0	
N_bx	24	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	9.35E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A-3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92-12 parameters 5.2dB at 26.56GHz		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	286 dB/in or 0.0506 dB/mm at 100 ohms
board_tl_tau	6.141E-03	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	102.7	mm
z_bp (NEXT)	102.7	mm
z_bp (FEXT)	102.7	mm
z_bp (RX)	102.7	mm

Floating Tap Control		
N_bg	**3**	**0 1 2 or 3 groups**
N_bf	3	taps per group
N_f	40	UI span for floating taps
bmaxg	0.1	max DFE value for floating taps

yellow indicates WIP