C2M Link Analysis at Host and Module Outputs

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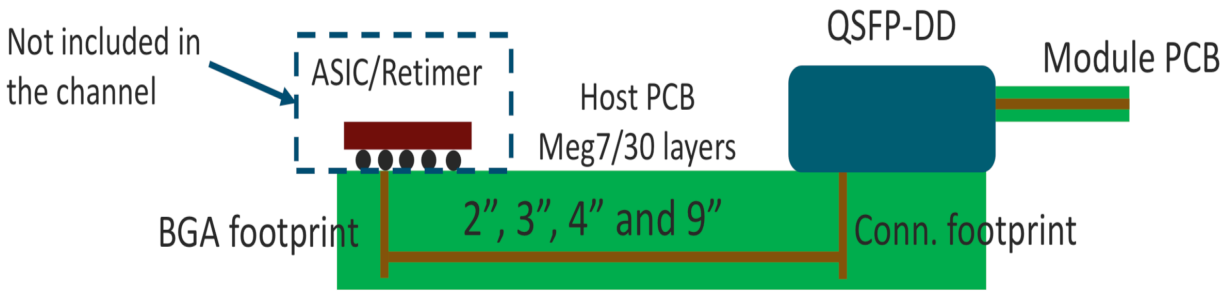
Overview

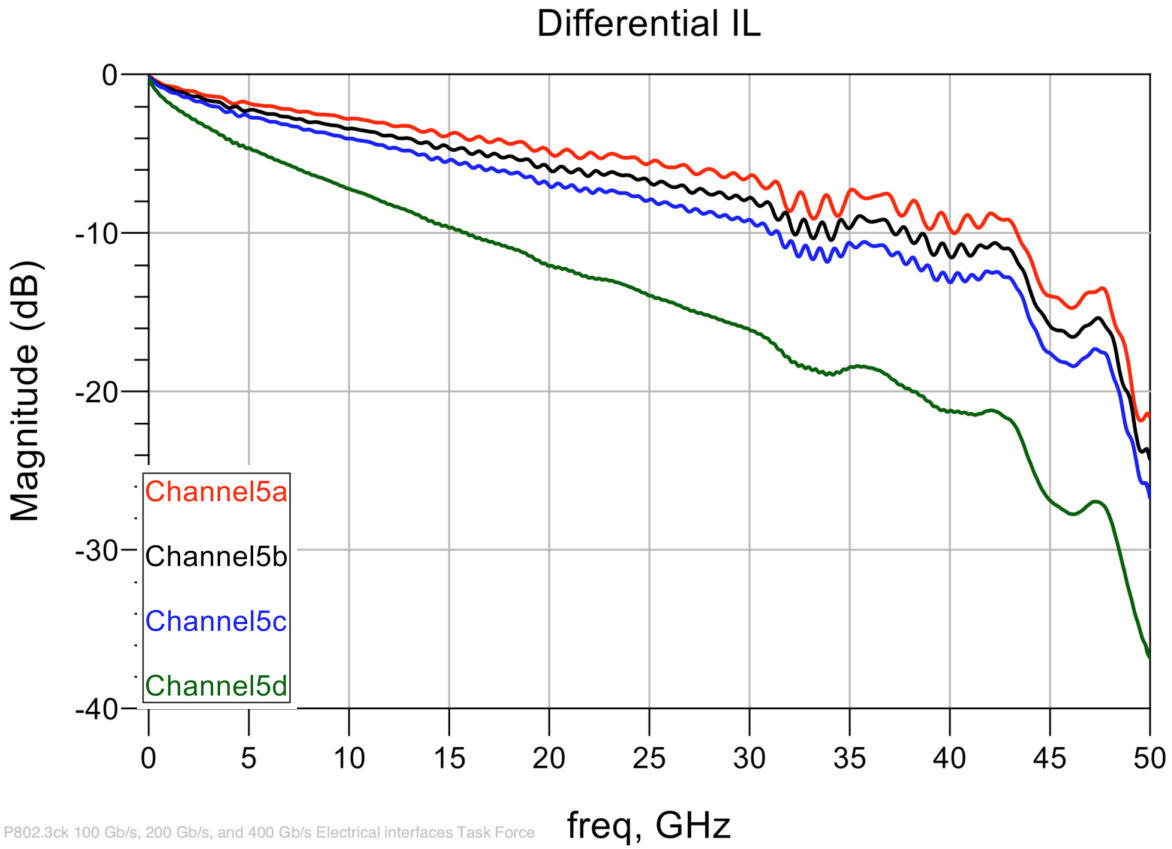
- **Updated analysis uses T-coil model for both host ASIC and module CDR**
  - ASIC and CDR T-coil inductor Ls=0.12 nf
  - ASIC Cd=120 ff but CDR Cd=100 ff
  - Some results from ghiasi_3ck_02a_0919
  - This analysis uses updated lim_3ck_adhoc_02_073119 channels
  - COM analysis at TP1a/Slicer and TP5/Slicer on min/max loss channels with Lim channels
- **Best choice for reference equalizer**
- **Summary.**

C2M Channels for Updated Analysis

- **Channel based on lim_3ck_adhoc_02_073119 as shown**
  - 16 pairs (8 Tx, 8 Rx) QSFP-DD SMT Connector with host PCB footprint
  - PCB stackup is 30 layers, 150 mils thick, based on Meg7 material
  - PCB via stub length is modeled as 10 mils
  - Diff pair trace width/spacing is 4.5 mils /8.5 mils
  - ASIC and retimer footprint are simulated with actual BGA ball-out using the same PCB stackup.



- **This analysis uses min loss channel 5a and max loss channel 5d.**



COM Code 2.70 Host-Module TP1a

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12 0]	nF	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[13 31; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[13 31; 1.8 1.8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[13 31; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	232	mm
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	232	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	232	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.7	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	0	UI			N_bx	4	UI				
b_max(1)	0.75				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	4	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.125										
ffe_backoff	1										

COM Code 2.70 Host-Module Slicer Input

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 1e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12 0.12]	nF	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[13 31; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[13 31; 1.8 1.8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[13 31; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	50	mm
z_p (RX)	[2 8 ; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	50	mm
C_p	[0.87e-4 0.65e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	50	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 45]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.9	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	0	UI			N_bx	4	UI				
b_max(1)	0.75				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	4	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.35										
ffe_post_tap1_max	0.35										
ffe_tapn_max	0.2										
ffe_backoff	1										

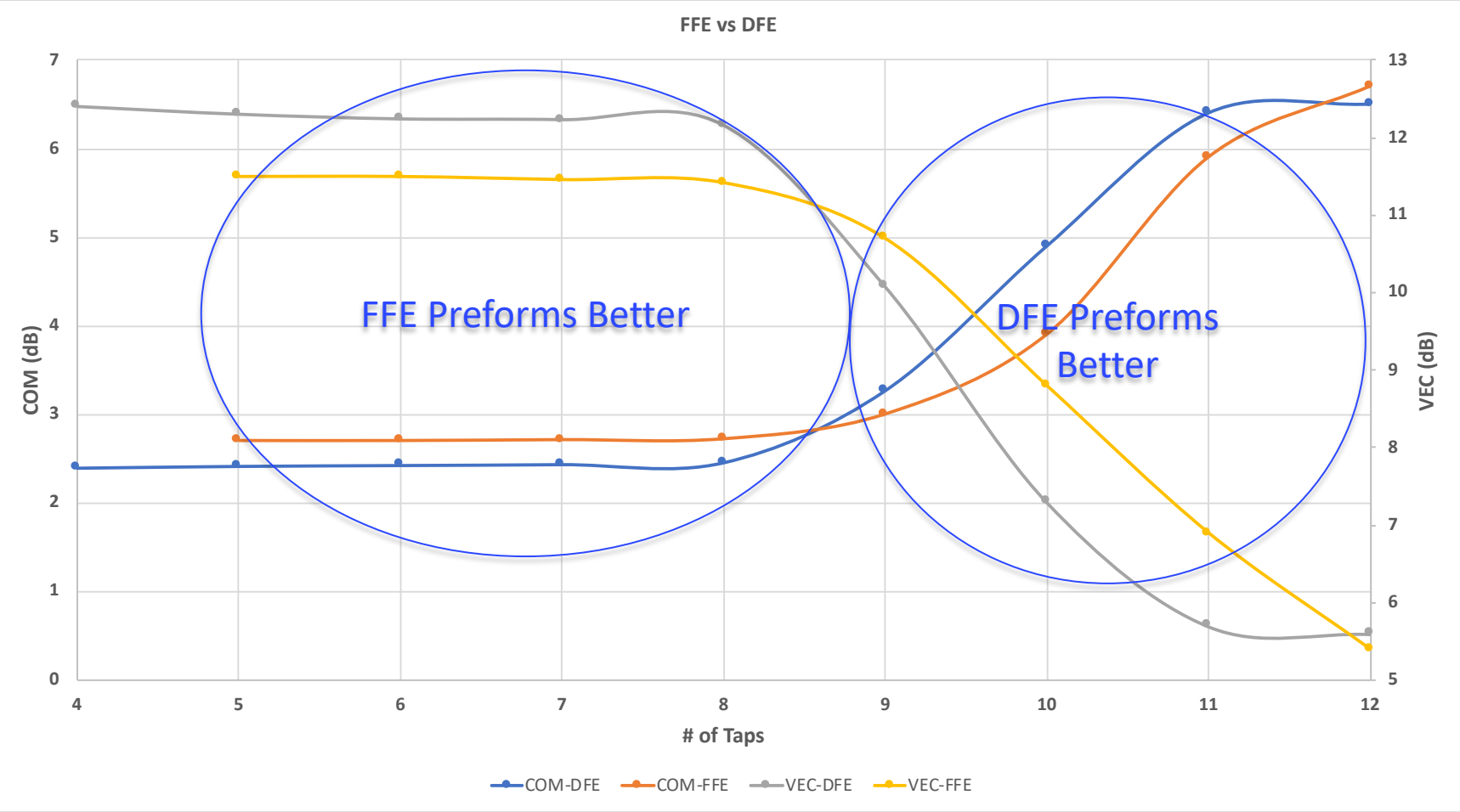
COM Analysis on Lim Channel 1 and 4 – ASIC to Module

- **Include BGA foot print+(mid length via)+ 2" or 9" host PCB+QSFP-dd connector (new pair) + Legacy QSFP-dd + module PCB.**

Channel	Equalizer	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO Case I	VEO Case II	VEC Case I	VEC Case II	COM Case I	COM Case II
Lim Channel 2" at TP1a FOM ILD = 0.16 ICN = 3.7 mV ERL11=12.3 dB ERL22=9.3 dB	5T FFE	5.9 dB	12.5 dB	21.4	31.3	11.5	6.0	2.7	6.0
	5T FFE + 1DFE	5.9 dB	12.5 dB	24.9	37.9	12.9	6.2	2.4	5.8
	4T DFE	5.9 dB	12.5 dB	24.4	38.0	12.3	6.2	2.4	5.8
	10T FFE	5.9 dB	12.5 dB	25.6	32.4	8.8	5.8	3.9	6.3
Lim Channel 2" At Slicer FOM ILD = 0.16 ICN = 3.7 mV ERL11=12.3 dB ERL22=9.3 dB	5T FFE	5.9 dB	14.5 dB	11.7	22.4	14.6	7.9	1.8	4.5
	5T FFE + 1DFE	5.9 dB	14.5 dB	17.3	29.0	14.6	7.7	1.8	4.5
	4T DFE	5.9 dB	14.5 dB	18	29.3	14.2	7.7	1.9	4.6
	10T FFE	5.9 dB	14.5 dB	16.9	21.4	11.4	7.7	2.7	4.8
Lim Channel 9" at TP1a FOM ILD = 0.13 ICN = 1.44 mV ERL11=16 dB ERL22=11.3 dB	5T FFE	14.8	21.4	11.2	14.2	10.7	6.4	3.0	5.6
	5T FFE + 1DFE	14.8	21.4	21.4	21.6	7.6	6.9	4.7	5.9
	4T DFE	14.8	21.4	20.0	17.1	8.2	6.3	4.3	5.8
	10T FFE	14.8	21.4	11.2	13.4	8.9	6.2	3.9	5.8
Lim Channel 9" At Slicer FOM ILD = 0.13 ICN = 1.44 mV ERL11=16.0 dB ERL22=11.3 dB	5T FFE	14.8	23.2	7.9	9.7	12.2	7.9	2.4	4.5
	5T FFE + 1DFE	14.8	23.2	18.6	16.9	8.0	6.9	4.4	5.2
	4T DFE	14.8	23.2	16.1	13.6	8.6	7.2	4.1	5.0
	10T FFE	14.8	23.2	8.0	10.2	10.4	7.3	3.1	4.9

Performance of FFE and DFE on Reflective Channel

- **COM and VEC for Lim 2” channel for 13 mm package**
  - Where DFE performs better than FFE would be too power hungry for the module – non starter!



COM 2.70 Module to Host (CDR PKG 2-8 mm)

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5]	Ohm
C_d	[1e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12 0]	nF	[TX RX]		Port Order	[2 4 1 3]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[2 8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[2 8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	215	mm
z_p (RX)	[0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	215	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	215	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 50]	Ohm	[TX RX]		Include PCB	1	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.7	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	0	UI			N_bx	4	UI				
b_max(1)	0.75				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	4	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.15										
ffe_backoff	1										

COM 2.75 Module to Host (CDR PKG 2-8 mm) with addition of C0/C1

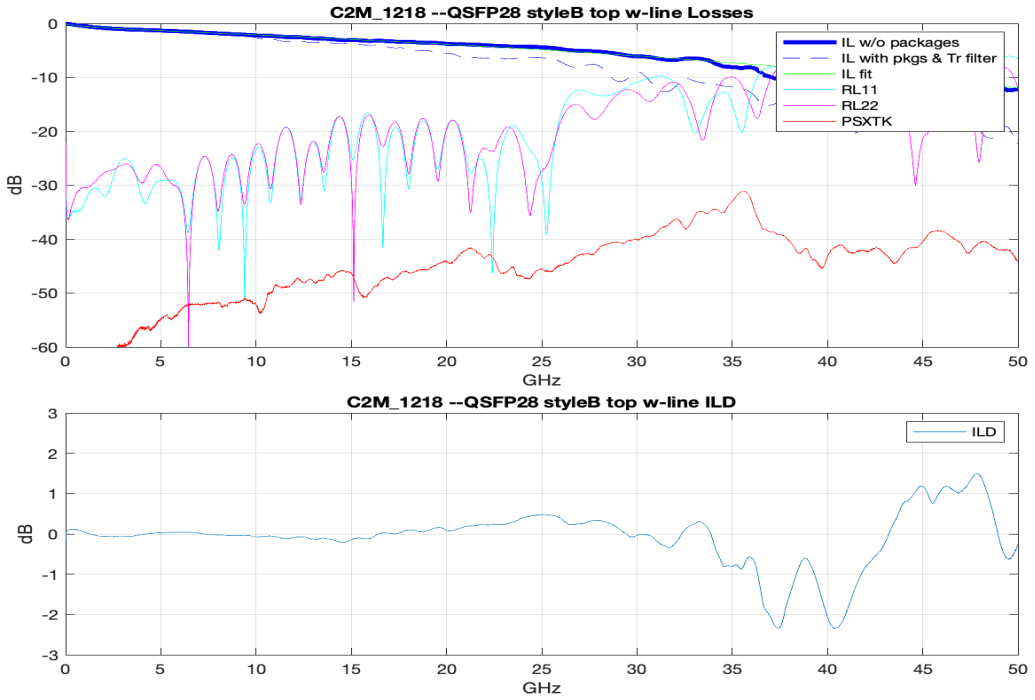
Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5]	Ohm
C_d	[1e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12 0]	nF	[TX RX]		Port Order	[2 4 1 3]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[2 8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[2 8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	68	mm
z_p (RX)	[0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	68	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	68	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 50]	Ohm	[TX RX]						C_0	[0.29e-4]	nF
A_v	0.41	V			TDR and ERL options				C_1	[0.19e-4]	nF
A_fe	0.41	V			TDR	1	logical		Include PCB	1	logical
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.7	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	0	UI			N_bx	4	UI				
b_max(1)	0.75				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.37E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	32.5	dB				
ffe_post_tap_len	4	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.15										
ffe_backoff	1										

COM 2.70 Module to Host at Slicer T-Coil Model (CDR PKG 2-8 mm)

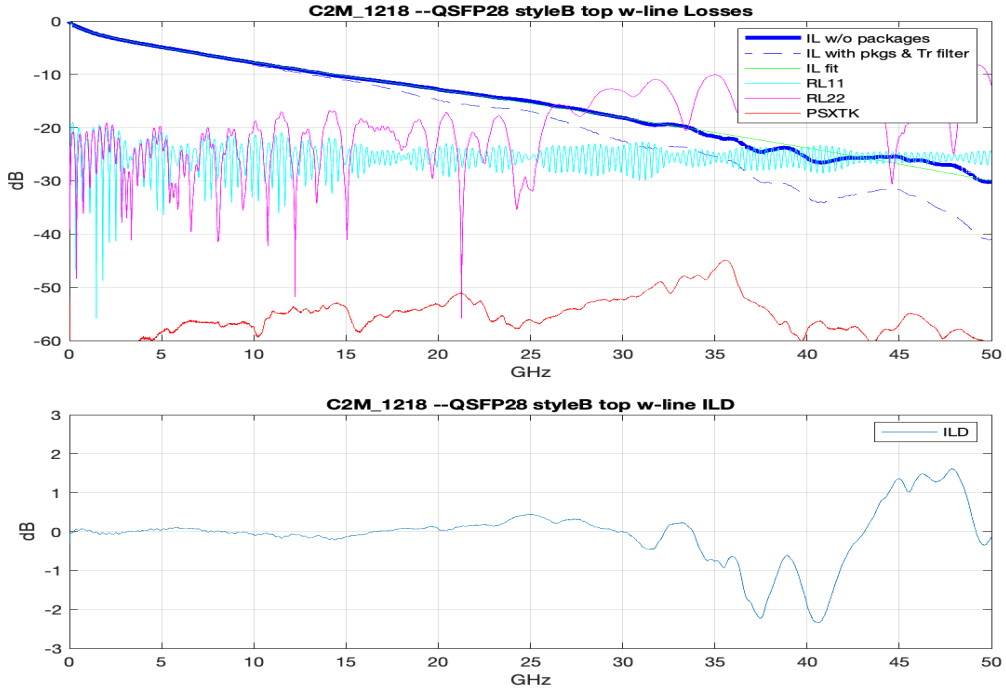
Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5; 92.5 92.5]	Ohm
C_d	[1e-4 1.2e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.1 0.12]	nF	[TX RX]		Port Order	[2 4 1 3]			Table 92–12 parameters		
C_b	[0 0.3e-4]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[2 8; 0.01 0.01]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 8; 0.01 0.01]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[2 8; 0.01 0.01]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	215	mm
z_p (RX)	[13 29; 1.8 1.8]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	215	mm
C_p	[0.65e-4 0.87e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	215	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 45]	Ohm	[TX RX]		Include PCB	1	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.8	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	4	UI			N_bx	4	UI				
b_max(1)	0.75				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	0	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.2										
ffe_backoff	1										

TP4/TP5 Analysis with Yamaichi QSFP-56 Mated Boards

Mated board IL = 5.2 dB
Total IL with 8 mm PKG=8.0 dB



Mated board + 220 mm trace IL = 16.1 dB
Total IL with 8 mm PKG=18.6 dB



Yamaichi QSFP56 Mated Board Near End and Far End Results

❑ Mated board COM with addition of PCB trace and C0/C1*

- Near end results with addition of 68 mm trace improves COM ~0.7 dB but after adding C0/C1 degrades COM by 0.5 dB
- Far end TP5 results degrades by 0.5 dB with addition of C0/C1.

Channel	Equalizer	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO Case I	VEO Case II	VEC Case I	VEC Case II	COM Case I	COM Case II
Yamaichi QSFP56 FOM ILD = 0.18 ICN = 5.2 mV ERL11=14.6 dB ERL22=10.7 dB TP4/Nearend	5T FFE	5.2	8.0	53.2	53	6.2	6.1	5.8	6.0
	4 DFE COM	5.2	8.0	55.1	53	6.9	6.7	5.2	5.4
	5T FFE + 68 mm	8.6	11.1	42.8	35.9	5.3	5.4	6.8	6.7
	4DFE + 68 mm	8.6	11.1	44.2	42.7	5.7	5.6	6.4	6.4
	5T FFE+68 mm+C0/C1	8.6	11.6	35.9	39.2	6.2	6.7	5.9	5.4
	4T DFE+68 mm+C0/C1	8.6	11.6	39.3	35.7	6.4	7.2	5.6	5.0
Yamaichi QSFP56 FOM ILD = 0.17 ICN = 1.6 mV ERL11=14.6 dB ERL22=10.7 dB TP5	5T FFE+215mm	15.8	18.6	21.0	18.0	5.3	5.7	6.8	6.3
	4T DFE+215mm	15.8	18.6	28.2	25.8	5.2	5.6	6.9	6.5
	5T FFE+215mm+C0/C1	15.8	19.2	16.9	16.3	6.5	6.3	5.6	5.8
	4T DFE+215mm+C0/C1	15.8	19.2	25.4	22.9	5.8	6.4	6.2	5.7

* Using CR COM reduced TX SNR and increased eta_0.

Yamaichi QSFP56 Mated Board at Slicer

- **Mated board COM with addition of PCB trace and C0/C1***
  - With addition of C0/C1 COM decreases by about 1.5 dB
  - The Slicer behavior with addition of C0/C1 is now more similar to Lim channels which include vias and BGA footorint
    - But Lim 2” channel still 0.7 dB worse even with addition of C0/C1.

Channel	Equalizer	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO Case I	VEO Case II	VEC Case I	VEC Case II	COM Case I	COM Case II
Yamaichi QSFP56 FOM ILD = 0.18 ICN = 5.2 mV ERL11=14.6 dB ERL22=10.7 dB At Slicer	5T FFE	5.2	12.8	36.3	27.9	8.6	6.7	4.0	5.3
	4 DFE COM	5.2	12.8	27.7	22.5	8.2	6.2	4.3	5.8
	5T FFE + 68 mm	8.6	15.5	36.3	27.9	8.6	6.7	4.0	5.3
	4DFE + 68 mm	8.6	15.5	35.3	38.0	8.8	6.7	3.9	5.4
	5T FFE+68 mm+C0/C1	8.6	16.4	16.3	16.5	12.1	8.7	2.5	4.0
	4T DFE+68 mm+C0/C1	8.6	16.4	20.8	22.7	10.5	8.1	3.1	4.4
Yamaichi QSFP56 FOM ILD = 0.17 ICN = 1.6 mV ERL11=14.6 dB ERL22=10.7 dB At Slicer	5T FFE+215mm	15.8	23.2	12.7	11.1	6.9	7.9	5.2	4.5
	4T DFE+215mm	15.8	23.2	15.7	13.0	6.5	6.7	5.6	5.4
	5T FFE+215mm+C0/C1	15.8	24.3	7.5	7.7	11.3	9.2	2.7	3.7
	4T DFE+215mm+C0/C1	15.8	24.3	14.3	10.6	9.0	7.8	3.8	4.6

* Using CR COM reduced TX SNR and increased eta_0.

Min/Max Channel Loss at Slicer with Yamaichi QSFP-56 Mated Boards

- **COM at slicer for min loss 5.2 dB channel and max loss 16 dB channel are about the same!**
  - The optimum TX FIR for 5T FFE and 4T DFE for Yamaichi mated board with 68 mm and C0/C1 were [0.04, -0.2, 0.76, 0]
  - The follow on simulations TX FIR was set to [0.04, -0.18, 072, -0.04].

Channel	Equalizer	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO Case I	VEO Case II	VEC Case I	VEC Case II	COM Case I	COM Case II
Yamaichi QSFP56 At TP5 FOM ILD = 0.18 ICN = 5.2 mV ERL11=14.6 dB ERL22=10.7 dB Optimum TX FIR	5T FFE	5.2	12.8	36.3	27.9	8.6	6.7	4.0	5.3
	4 DFE COM	5.2	12.8	27.7	22.5	8.2	6.2	4.3	5.8
	5T FFE + 68 mm	8.6	15.5	36.3	27.9	8.6	6.7	4.0	5.3
	4DFE + 68 mm	8.6	15.5	35.3	38.0	8.8	6.7	3.9	5.4
	5T FFE+68 mm+C0/C1	8.6	16.4	16.3	16.5	12.1	8.7	2.5	4.0
	4T DFE+68 mm+C0/C1	8.6	16.4	20.8	22.7	10.5	8.1	3.1	4.4
Yamaichi QSFP56 At Slicer FOM ILD = 0.17 ICN = 1.6 mV ERL11=14.6 dB ERL22=10.7 dB Optimum TX FIR	5T FFE+215mm	15.8	23.2	12.7	11.1	6.9	7.9	5.2	4.5
	4T DFE+215mm	15.8	23.2	15.7	13.0	6.5	6.7	5.6	5.4
	5T FFE+215mm+C0/C1	15.8	24.3	7.5	7.7	11.3	9.2	2.7	3.7
	4T DFE+215mm+C0/C1	15.8	24.3	14.3	10.6	9.0	7.8	3.8	4.6

COM Analysis on Lim Channel 1 and 4 – Module to ASIC

- **Lim 2” or 9” host PCB with QSFP-dd connector, mid-depth via, and ASIC foot printed included**
  - Non-optimum TX FIR is the optimum setting for Yamaichi mated board + 68 mm with CR C0/C1 included
  - Sub-optimum TX FIR has about 0.5 dB penalty on 5T FFE and 4T DFE at TP5!

Channel	Equalizer	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO Case I	VEO Case II	VEC Case I	VEC Case II	COM Case I	COM Case II
Lim Channel 2” at TP5 FOM ILD = 0.16 ICN = 3.7 mV ERL11=12.3 dB, ERL22=9.3 dB Optimum TX FIR	5T FFE	5.9	8.6	49.7	47.5	6.6	6.4	5.5	6.0
	5T FFE + 1DFE	5.9	8.6	51.6	50.7	7.1	6.7	5.0	5.3
	4T DFE	5.9	8.6	51.1	50.7	7.1	6.8	5.0	5.8
	10T FFE	5.9	8.6	51.4	45.2	6.3	5.9	5.7	6.1
Lim Channel 2” at TP5 FOM ILD = 0.16 ICN = 3.7 mV ERL11=12.3 dB , ERL22=9.3 dB TX FIR=[0.04, -0.18, 0.74, -0.04]	5T FFE	5.9	8.6	43.7	40.5	7.1	7.0	5.0	5.2
	5T FFE + 1DFE	5.9	8.6	38.1	37.1	8.3	8.0	4.2	4.4
	4T DFE	5.9	8.6	37.8	38.1	8.4	8.0	4.2	4.4
	10T FFE	5.9	8.6	44.9	42.1	6.9	6.6	5.2	5.5
Lim Channel 9” at TP5 FOM ILD = 0.13 ICN = 1.44 mV ERL11=11.8 dB, ERL22=14.8 dB Optimum TX FIR	5T FFE	14.8	16.8	20.8	22.4	6.2	6.5	5.8	5.5
	5T FFE + 1DFE	14.8	16.8	30.2	26.0	5.7	6.1	6.3	5.9
	4T DFE	14.8	16.8	28.2	24.7	5.8	6.1	6.2	5.9
	10T FFE	14.8	16.8	21.1	19.5	5.9	5.8	6.1	6.2
Lim Channel 9” at TP5 FOM ILD = 0.13 ICN = 1.44 mV ERL11=11.8 dB, ERL22=14.8 dB TX FIR=[0.04, -0.18, 0.74, -0.04]	5T FFE	14.8	16.8	23.3	19.2	6.4	6.6	5.6	5.5
	5T FFE + 1DFE	14.8	16.8	25.3	24.8	6.2	6.2	5.9	5.8
	4T DFE	14.8	16.8	24.5	25.0	6.2	6.1	5.8	5.9
	10T FFE	14.8	16.8	24.1	24.5	6.2	6.1	5.8	5.9

COM Analysis on Lim Channel 1 and 4 – Module to ASIC

- **Lim 2” or 9” host PCB with QSFP-dd connector, mid-depth via, and ASIC foot printed included**
  - Non-optimum TX FIR is the optimum setting for Yamaichi mated board + 68 mm with CR C0/C1 included
  - The 5T FFE has negligible penalty for sub-optimum TX FIR but the 4T DFE has about 0.5 dB penalty at the slicer!

Channel	Equalizer	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO Case I	VEO Case II	VEC Case I	VEC Case II	COM Case I	COM Case II
Lim Channel 2” At Slicer FOM ILD = 0.16 ICN = 3.7 mV ERL11=11.3 dB, ERL22=10.5 dB TX FIR Optimum	5T FFE	5.9	14.3	12.8	26.5	14.4	7.2	1.8	4.5
	5T FFE + 1DFE	5.9	14.3	16.4	32.2	14.9	7.1	1.7	5.7
	4T DFE	5.9	14.3	16.4	32.2	14.9	7.1	1.7	5.1
	10T FFE	5.9	14.3	18.0	23.1	11.1	6.7	2.8	5.3
Lim Channel 2” At Slicer FOM ILD = 0.16 ICN = 3.7 mV ERL11=11.3 dB, ERL22=10.5 dB TX FIR=[0.04, -0.18, 0.74, -0.04]	5T FFE	5.9	14.3	12.1	26.8	14.5	7.4	1.8	4.9
	5T FFE + 1DFE	5.9	14.3	11.8	29.0	16.6	7.4	1.4	4.8
	4T DFE	5.9	14.3	11.9	29.0	16.6	7.4	1.4	4.8
	10T FFE	5.9	14.3	18.9	23.8	11.1	7.0	2.8	5.2
Lim Channel 9” at Slicer FOM ILD = 0.13 ICN = 1.44 mV ERL11=11.8 dB, ERL22=14.8 dB TX FIR Optimum	5T FFE	14.8	23.0	8.0	12.7	11.9	7.0	2.5	5.1
	5T FFE + 1DFE	14.8	23.0	18.6	17.1	7.6	6.3	4.5	5.8
	4T DFE	14.8	23.0	16.9	14.1	8.5	6.5	4.1	5.6
	10T FFE	14.8	23.0	8.2	12.5	10.3	6.5	3.2	5.6
Lim Channel 9” At Slicer FOM ILD = 0.13 ICN = 1.44 mV ERL11=11.8 dB, ERL22=15.1 dB TX FIR=[0.04, -0.18, 0.74, -0.04]	5T FFE	14.8	23.0	10.4	12.9	12.2	7.1	2.4	5.1
	5T FFE + 1DFE	14.8	23.0	14.8	17.4	9.2	6.3	3.7	5.7
	4T DFE	14.8	23.0	14.0	13.9	9.7	6.5	3.5	5.5
	10T FFE	14.8	23.0	8.9	11.7	10.4	6.5	3.1	5.6

Key Observations

- **Compliance results are at TP1a, TP4, and TP5**
  - Normative specifications are VEC, VEO, EW
  - Results are measured on the scope with reference equalizer and not with COM
  - Slicer results and COM values are listed to give an idea on the chip requirements
- **The VEC at TP1a ~10 dB but at TP5 is only ~ 6 dB**
  - TP5 test point is less stressful because the ASIC BGA is not included
- **At TP1a**
  - 5T FFE performs better than 4T DFE but 4T DFE performs better on high loss channel
  - On short channels unless the receiver can operate with ~12.5 dB VEC then a receiver such as 10T FFE would be required
- **At TP5**
  - Given ASIC BGA not included the VEC even for weakest equalizer need to be set to ≤ 7 dB.

Summary

- **The reference equalizer is a software equalizer in the scope**
  - The reference equalizer has to be weaker than actual equalizer given the slicer has 2-4 dB higher VEC
- **Receiver considered for this study are 5T FFE, 4T DFE, 5T FFE+1T DFE, and 10T FFE**
  - 4T DFE performs better than 5T FFE on high loss channels
  - But 5T FFE actually performs better on low loss/reflective channels
  - To mitigate (reduce VEC< 9 dB) on short reflective channels ~10T FFE or DFE maybe be necessary
- **One option is to go ahead and define 10T FFE or floating tap DFE with 10T span to mitigate reflective channel effects but this will result in high power for every implementation**
  - Given that signal is very large > 20 mV on short reflective channel some receiver may be able to operate with ~12.5 dB of VEC
  - But some receivers instead of operating with high VEC instead may implement longer FFE/DFE or other scheme to mitigate the package reflections
- **TP4 output is too optimistic and may not add value measuring EH/EW but TP4 should be used for return loss/ERL measurements**
  - TP5-L1 (~4.5 dB host PCB loss) and TP5-L2 (11.9 dB host PCB loss) are more representative short and long host channels by using CR C0/C1 and increased eta_0
  - TP5-L1 is used to set the module TX FIR and with the same setting TP5-L2 must be met.