What should the CTLE range be for Chip to Module?

Sept 2021

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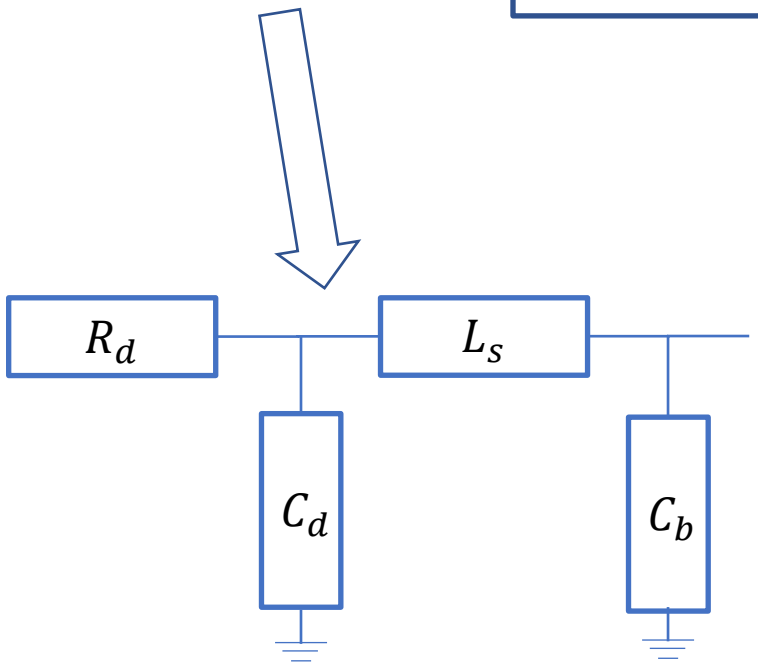
Introduction

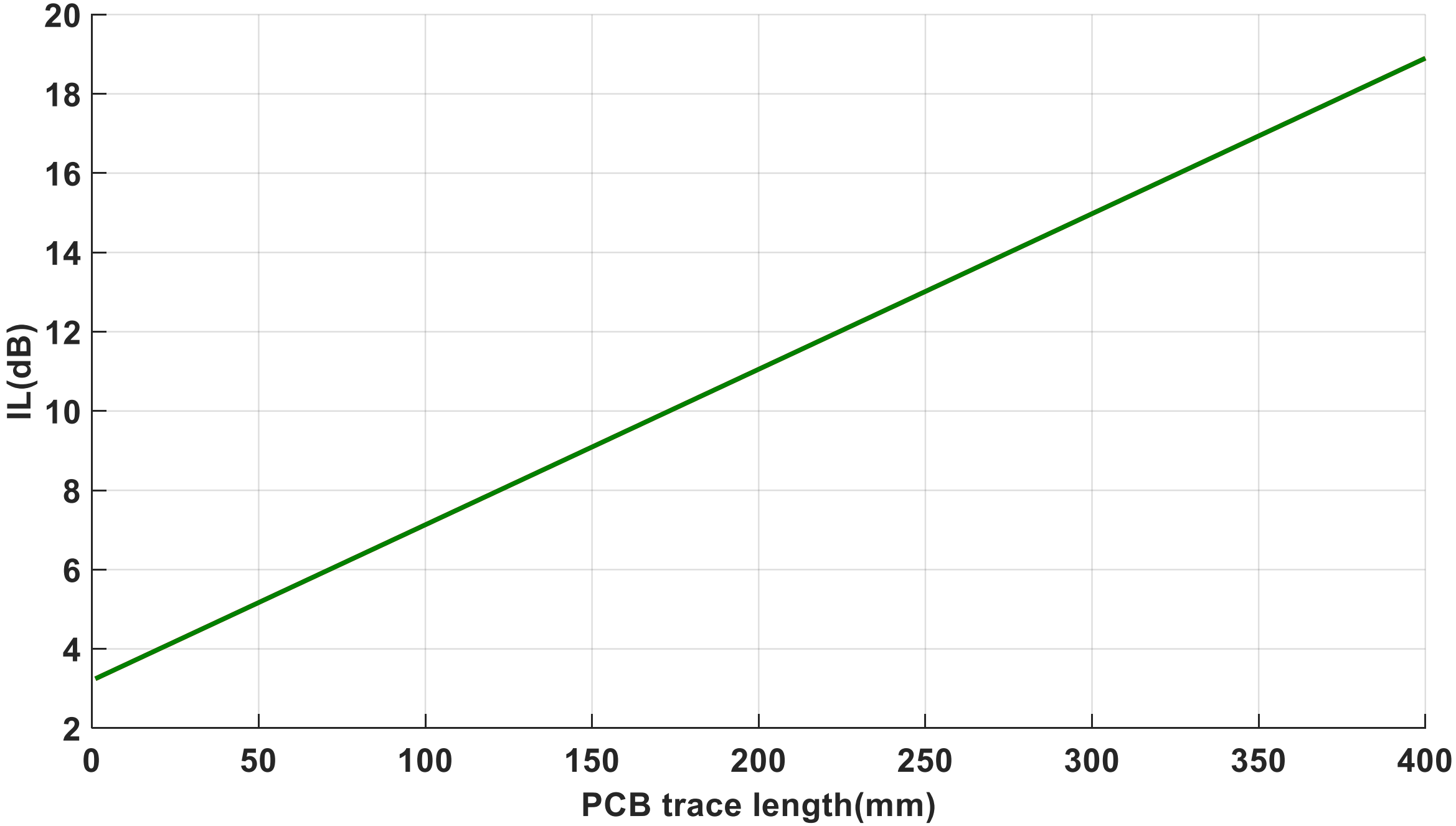
- This presentation explores the optimum CTLE setting for the Chip to Module reference receiver at TP1a as a function of channel loss
- Simulations use the ASIC parameters in 802.3ck draft 2.2
- The Tx FIR tap weights, CTLE gains and DFE tap weights are optimized at each channel length.
- The presentation shows that the 13dB minimum gain used for calibrating the module stressed input is not optimum.
- It recommends changes to the CTLE ranges.

Chip to Module Block Diagram

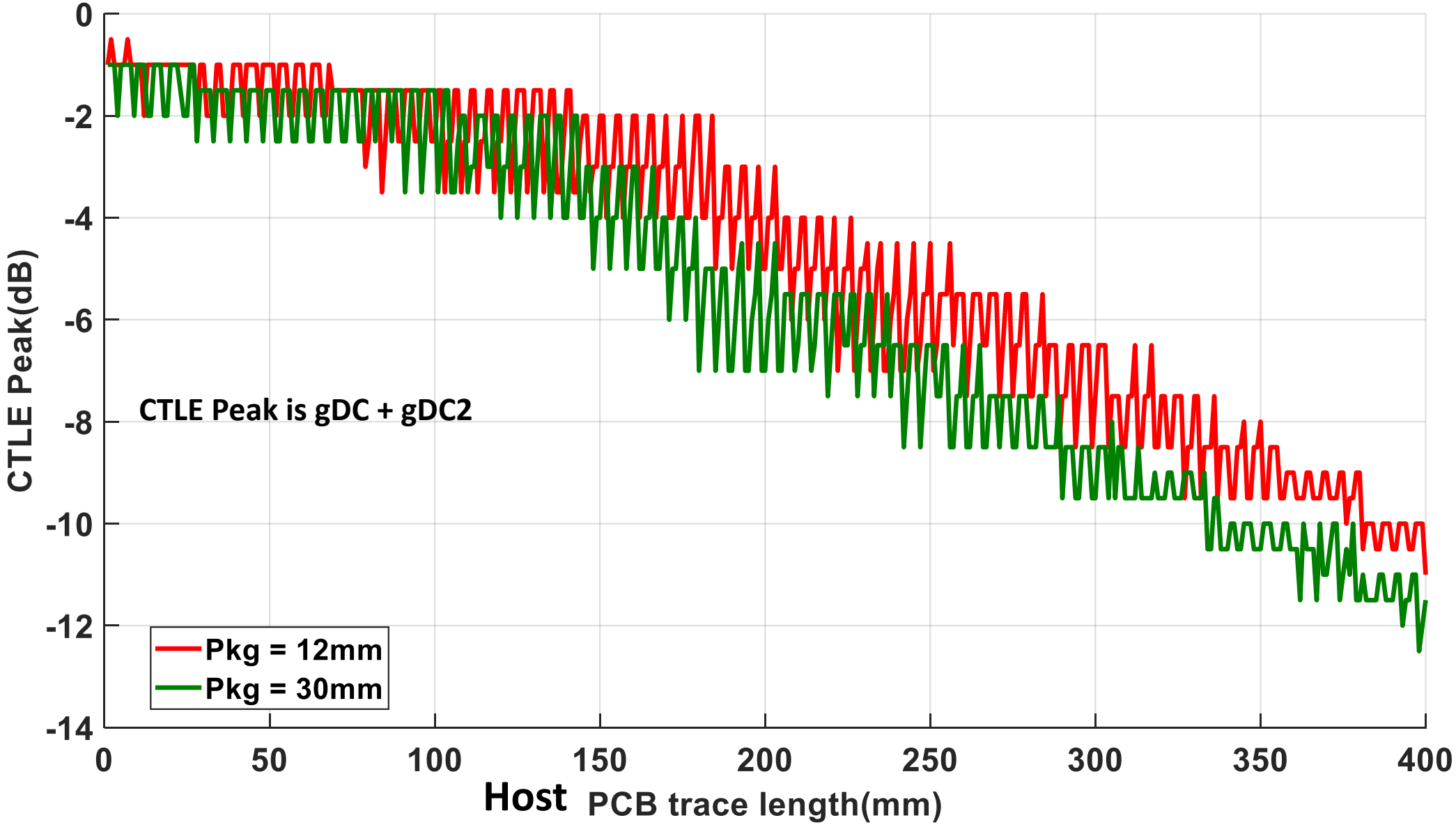


On-die inductor termination

com_ieee8023_93a_320.m


20
18
16
14
12
10
8
6
4
2
IL(dB)
0
50
100
150
200
250
300
350
400
PCB trace length(mm)

Optimum CTLE peak as a function of Host PCB Trace Length

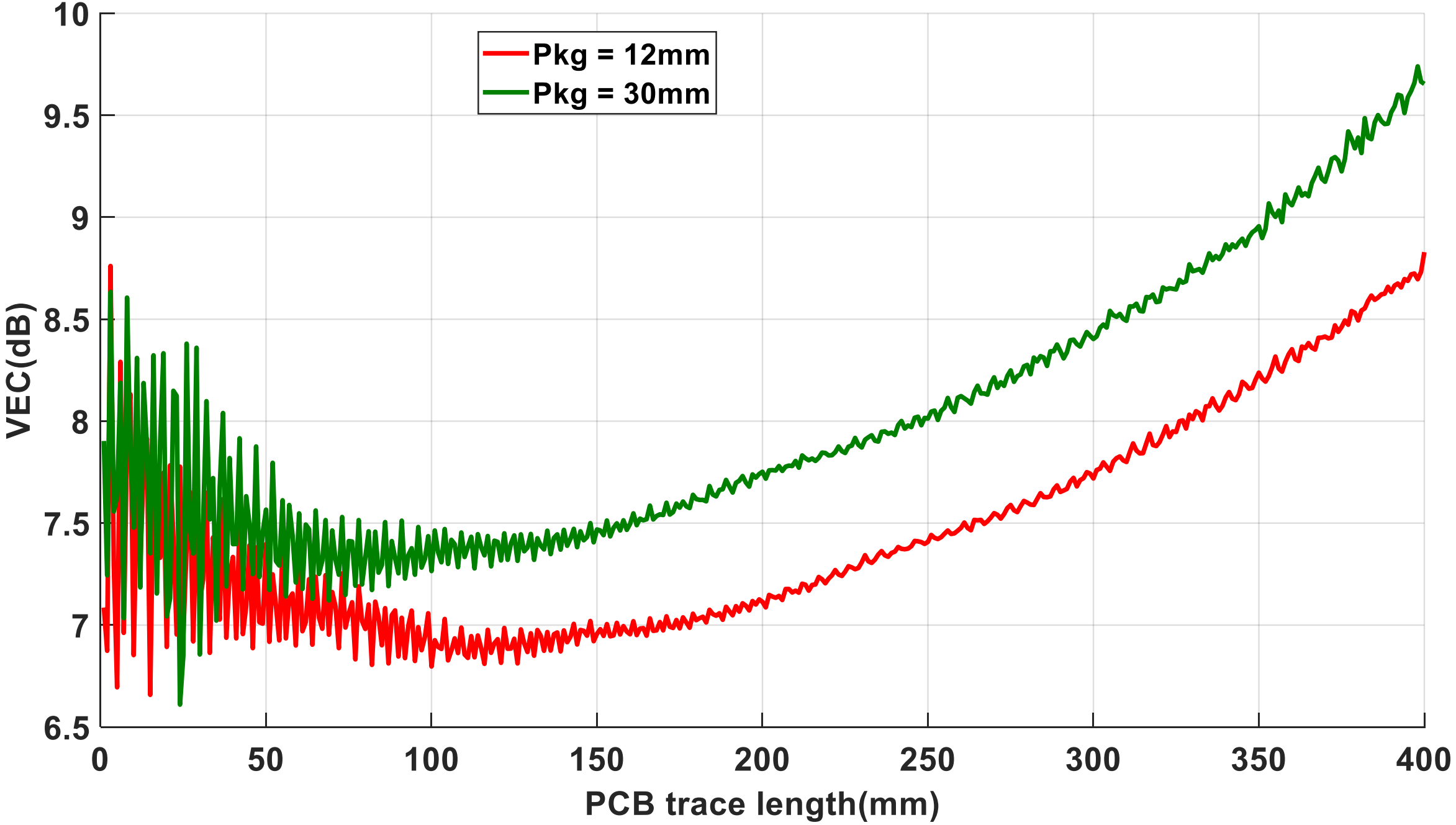


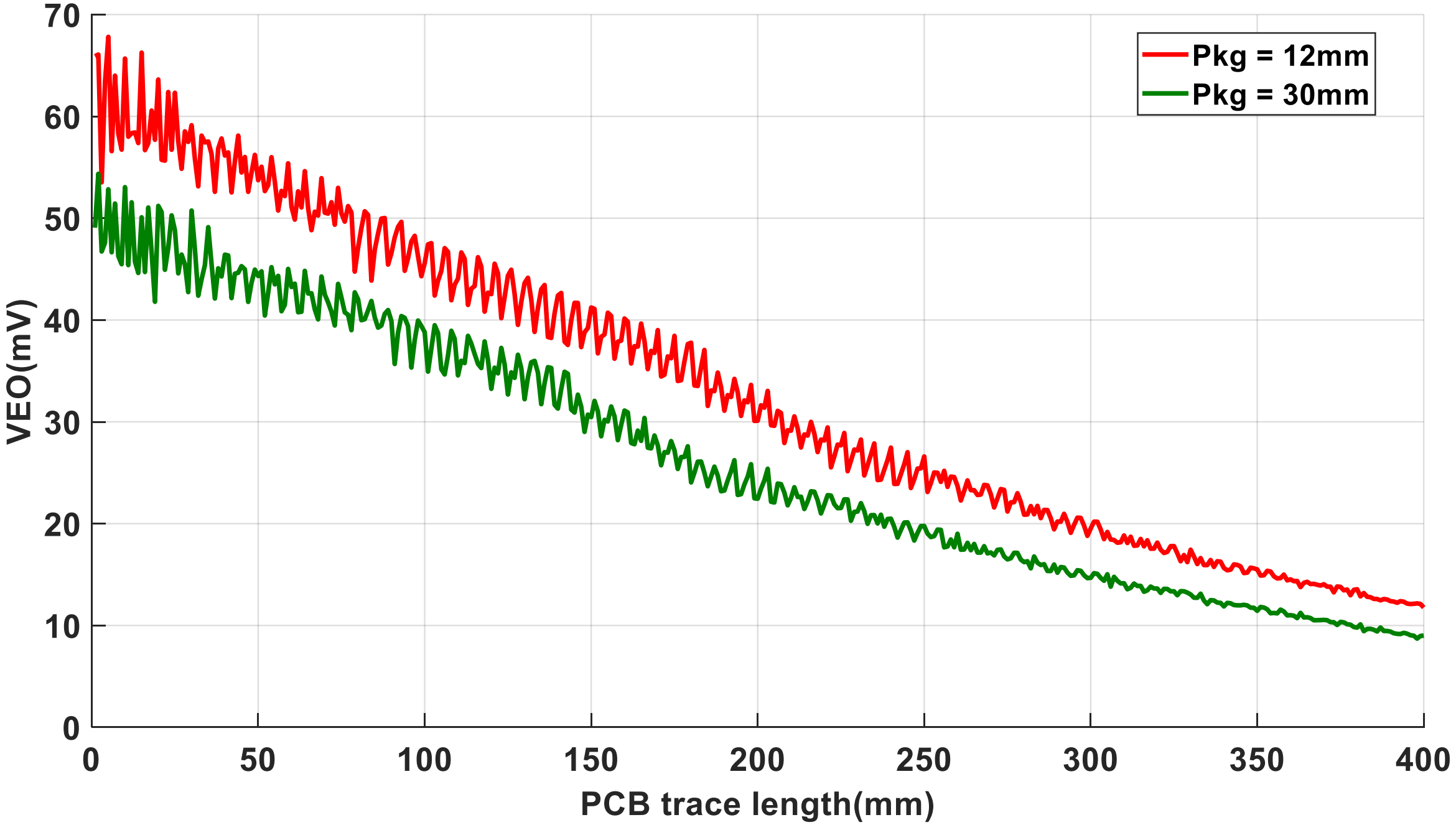
Conclusion

- With 16dB channel loss and the 30mm package the optimum CTLE peak is 9.5dB
- With 18.2dB channel loss and the 12mm package the optimum CTLE peak is 10.5dB
- Requiring a minimum gain of 13dB for the module stressed input signal calibration is significantly far from the optimum. The minimum gain should be reduced to 10.5dB for this calibration.

- Allowing the hosts to pass specification by using high CTLE gains will result in sub-optimum host Tx FIR settings and will require more gain than necessary in the module receivers. The max CTLE gains for the host testing should be reduced to approximately 11dB.
- Recommended change to the CTLE ranges is

-1<gDC2 <0 gDC range -2 to -11,
-2<gDC2 <-1 gDC range -4 to -10,
-3<GDC2 <-2 gDC range -4 to -9

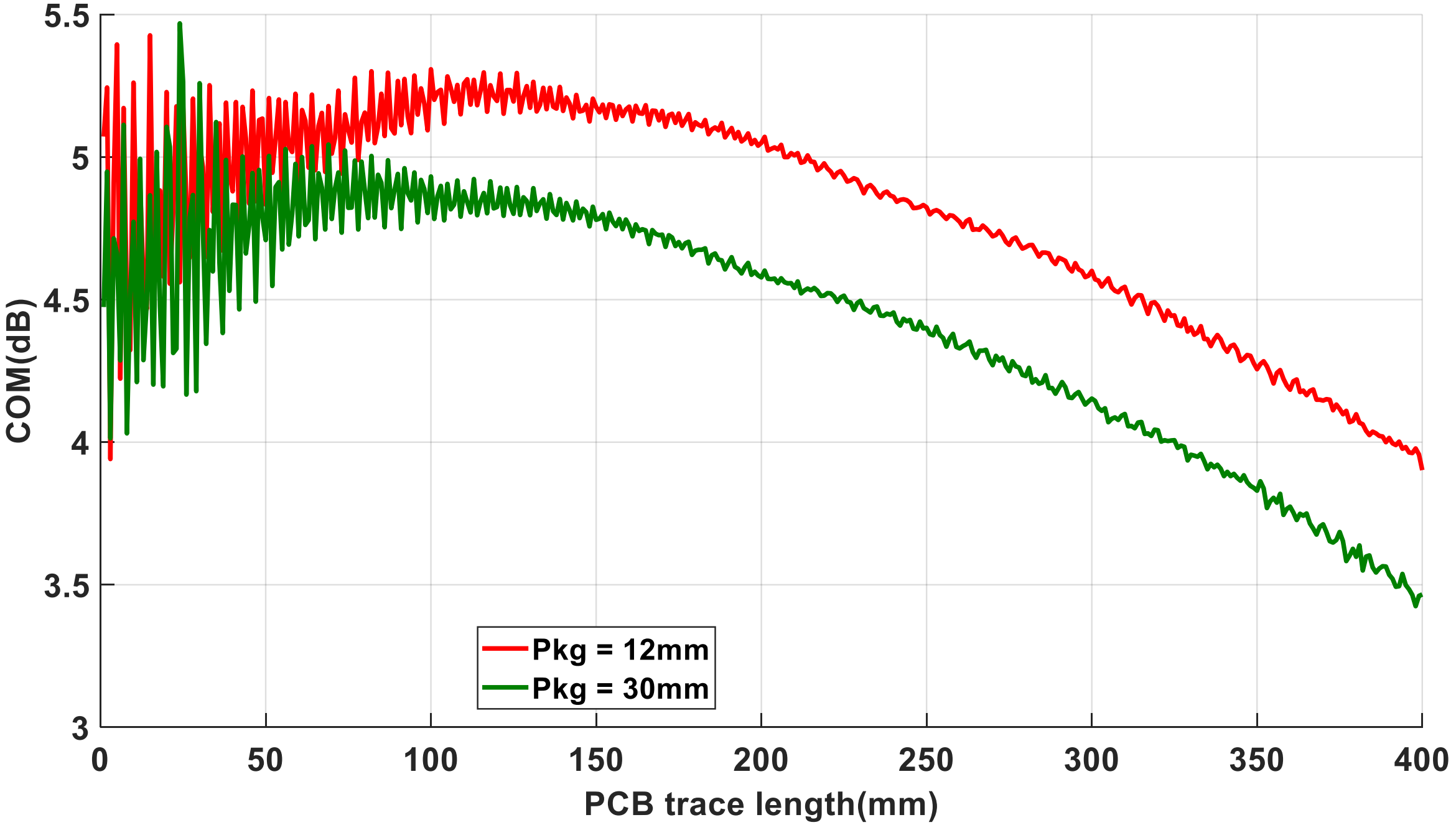

Pkg = 12mm
Pkg = 30mm
VEC(dB)
10
9.5
9
8.5
8
7.5
7
6.5
0
50
100
150
200
250
300
350
400
PCB trace length(mm)


Pkg = 12mm
Pkg = 30mm
VEO(mV)
PCB trace length(mm)
0
10
20
30
40
50
60
70
0
50
100
150
200
250
300
350
400

Backup

COM spreadsheet

Table 93A-1 parameters					I/O control			Table 93A–3 parameters		
Parameter	**Setting**	**Units**	**Information**		DIAGNOSTICS	0	logical	**Parameter**	**Setting**	**Units**
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical	package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	0	logical	package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_C2M_host_{d		package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical	**ICN & FOM_ILD parameters**		
L_s	[0.12 0]	nH	[TX RX]		Port Order	[1 3 2 4]		f_v	0.594	*Fb
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	C2M_eval_		f_f	0.594	Hz f_r specified in first column
z_p select	[1]		[test cases to run]		COM_CONTRIBUTION	0	logical	f_n	0.594	GHz
z_p (TX)	[15 30; 1.8 1.8]	mm	[test cases]		Local Search	2		f_2	40	GHz
z_p (NEXT)	[0 0 ; 0 0]	mm	[test cases]		**Operational**			A_ft	0.600	V
z_p (FEXT)	[15 30; 1.8 1.8]	mm	[test cases]		VEC Pass threshold	12	db	A_nt	0.600	V
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]		EH_min	10	mV			
C_p	[0.87e-4 0]	nF	[TX RX]		ERL Pass threshold	7.3	dB			
R_0	50	Ohm			Min_VEO_Test	10	mV			
R_d	[50 50]	Ohm	[TX RX]		DER_0	0.00001		Histogram_Window_Weigh	gaussian	Seletions (rectangle, gaussian,
A_v	0.415	V			T_r	0.0075	ns			
A_fe	0.415	V			FORCE_TR	1	logical			
A_ne	0.450	V			PMD_type	C2M				
L	4				BREAD_CRUMBS	0	logical			
M	32	Samp/UI			SAVE_CONFIG2MAT	1	logical			
samples_for_C2M	100	Samp/UI			PLOT_CM	0	logical			
T_O	50	mUI			**TDR and ERL options**					
AC_CM_RMS	0	V	[test cases]	[0.0235 0.0256]	TDR	1	logical			
filter and Eq					ERL	1	logical			
f_r	0.75	*fb			ERL_ONLY	0	logical			
c(0)	0.54		min		TR_TDR	0.01	ns			
c(-1)	[-0.2:0.02:0]		[min:step:max]		N	800				
c(-2)	[0:0.02:0.1]		[min:step:max]		beta_x	0				
c(-3)	[0]		[min:step:max]		rho_x	0.618				
c(1)	[-0.1:0.02:0]		[min:step:max]		fixture delay time	[0 0.3e-9]	port1 port2]			
N_b	4	UI			TDR_W_TXPKG	1				
b_max(1)	**0.4**		**As/dffe1**		N_bx	0	UI			
b_max(2..N_b)	**[0.15 0.15 0.1]**		**As/dfe2..N_b**		Tukey_Window	1				
b_min(1)	**0.1**		**As/dffe1**		**Receiver testing**					
b_min(2..N_b)	**[-0.15 - 0.15 - 0.05]**		**As/dfe2..N_b**		RX_CALIBRATION	0	logical			
g_DC	[-13:1:-0]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V			
f_z	12.58	GHz			**Noise, jitter**					
f_p1	20	GHz			sigma_RJ	0.01	UI			
f_p2	28	GHz			A_DD	0.02	UI			
g_DC_HP	[-3:0.5:0]		[min:step:max]		eta_0	4.10E-08	V^2/GHz			
f_HP_PZ	1.328125	GHz			SNR_TX	32.5	dB			


5.5
5
4.5
4
3.5
3
COM(dB)
0
50
100
150
200
250
300
350
400
PCB trace length(mm)
Pkg = 12mm
Pkg = 30mm