Mixed-mode return loss limits P802.3ck D3.0 comment 185

Piers Dawe, Nvidia January 2022

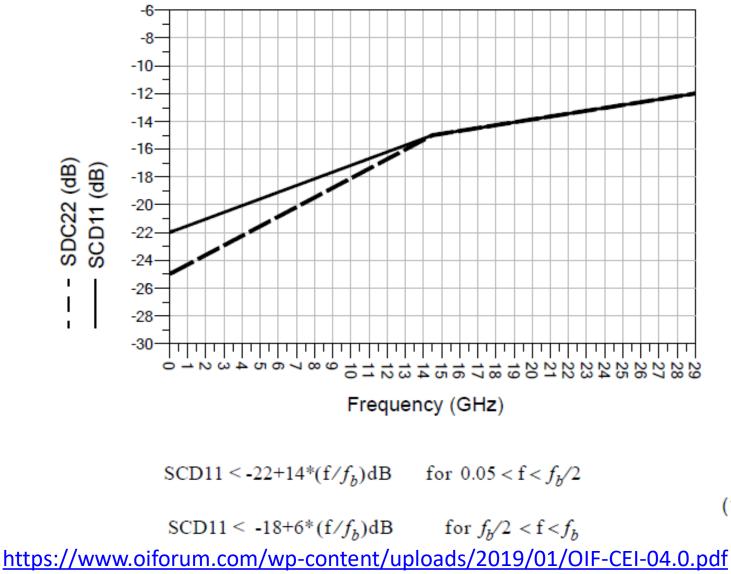
Introduction

- We have mixed-mode return loss specs to reduce the amount of the desired differential signal being reflected back upstream by an input into the common mode, then being reflected back downstream by an output into the differential mode, interfering with the original
- Both in CR and C2M
- OIF CEI-xG-VSR and previous C2M AUIs have such specs
- The specs in this draft are "PAM2 grade", and probably need tightening because:
- This is PAM4
- 12 dB VEC limit allows poor eyes even after a much more capable reference equalizer, so more susceptible
- The higher compliance board loss makes the same headline number of dB deliver fewer dB at the connector

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OIF CEI-56G-VSR-PAM4

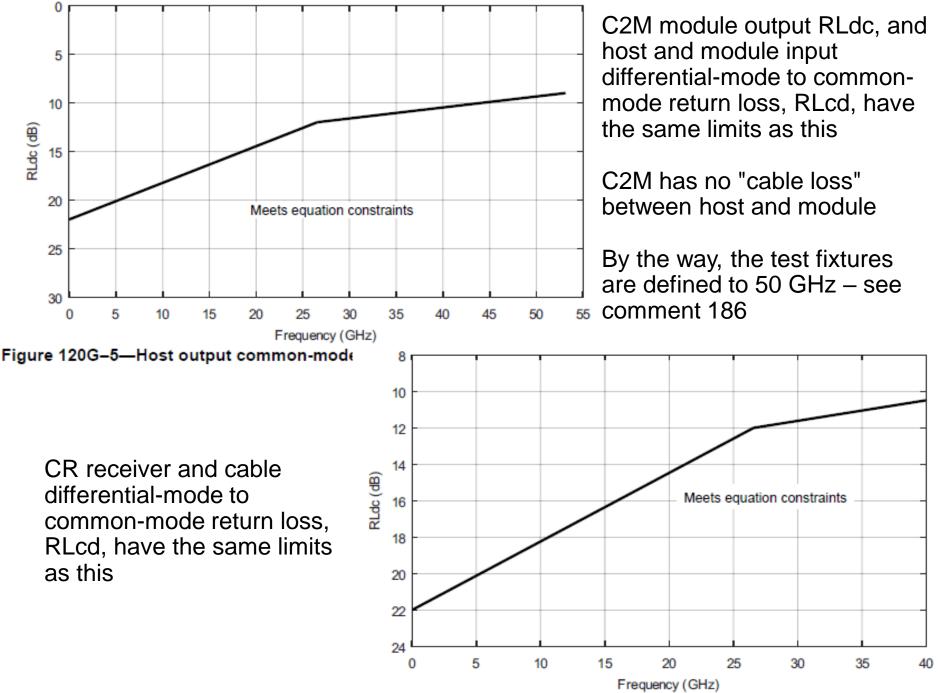
Figure 16-3. SCD11 for module input (TP1) and host input (TP4a), and SDC22 for module output (TP4) and host output (TP1a) (for f_b=29 GHz)



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(16-2)

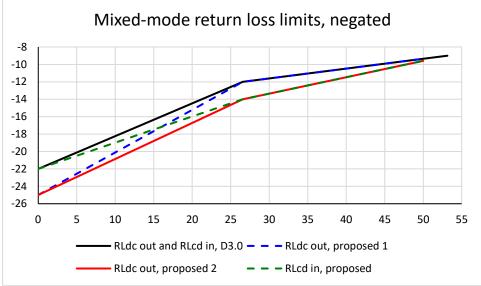


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Figure 162-4-Transmitter common-mode to differential-mode return loss

Comment 185 for C2M

Specs should be tightened



- This is what the comment proposes:
 - In Equation 120G-1, change 22 -20f/fb to 25 -26f/fb
 - If correcting for increased compliance board loss,
 - change Equation 120G-1 from 22 -20f/fb, 15 -6f/fb to 25 -22f/fb, 19 -10f/fb,
 - change Equation 120G-2 from 22 -20f/fb, 15 -6f/fb to
 22 -16f/fb, 19 -10f/fb

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Minor bug

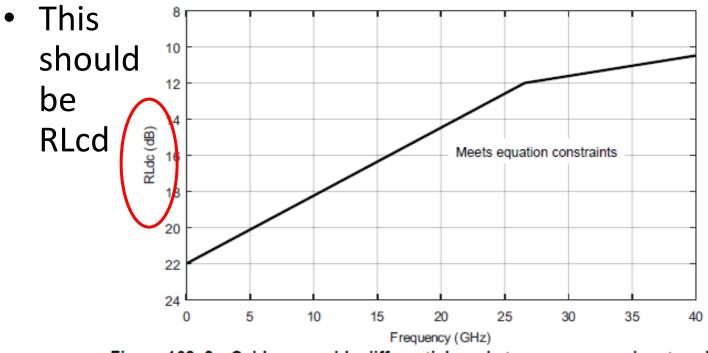


Figure 162-8—Cable assembly differential-mode to common-mode return loss