Validating C2M VEC and VEO Limits

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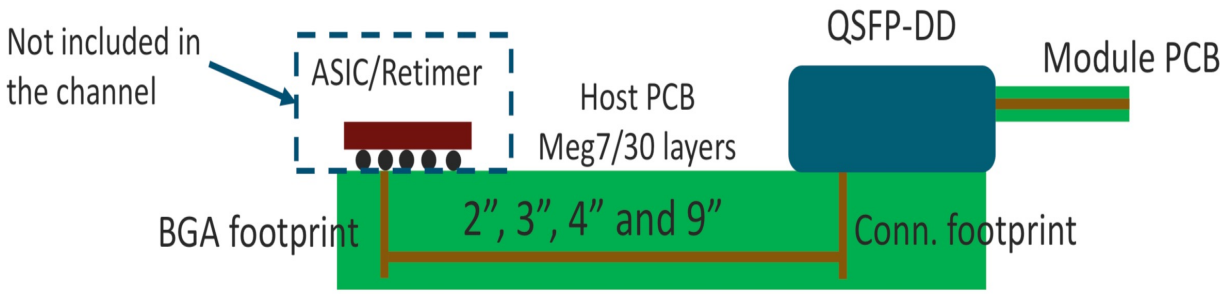
Overview

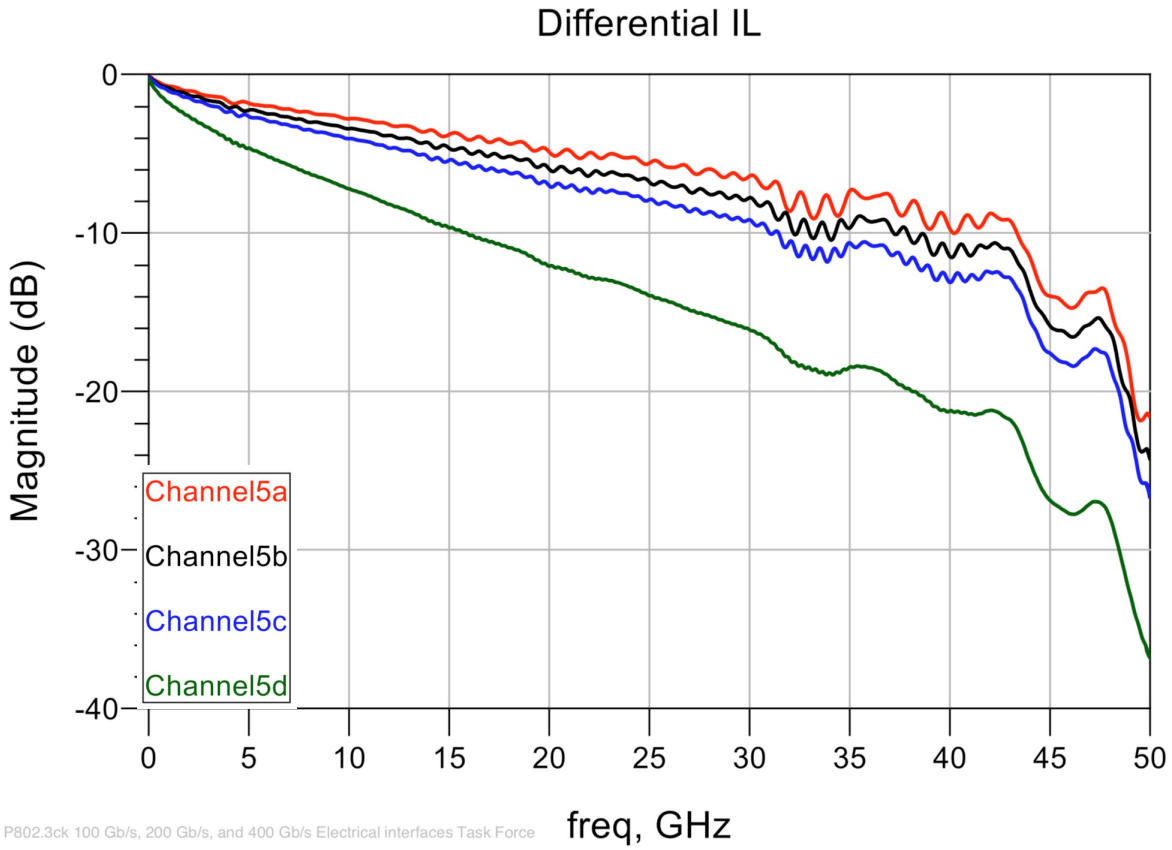
- **Updated analysis is with COM 3.1.0**
  - The updated TP1a analysis uses lim_3ck_adhoc_02_073119 channels
  - The updated TP4 analysis uses lim_3ck_02_0719 channels
- **COM analysis investigates impact of ts=+/-50 mUI rectangular window on established VEO/VEC limits of D1.3 draft**
  - The intention was to only adjust the TP1a/TP4 limits due to ts=+/-50 mUI rectangular window
  - But D2.0 VEO/VEC limits at TP1a have been tighten compare to D1.3 without rectangular window for the host and relaxed for the module
  - Tightening the VEO/VEC limits results in some of Lim TP1a channels failing that previously passed
- **Addressing D2.0 comments 34, 41, 42, 46, and 48.**

C2M TP1a Channels for Updated Analysis

- **Channel based on lim_3ck_adhoc_02_073119 as shown**
  - 16 pairs (8 Tx, 8 Rx) QSFP-DD SMT Connector with host PCB footprint
  - PCB stackup is 30 layers, 150 mils thick, based on Meg7 material
  - PCB via stub length is modeled as 10 mils
  - Diff pair trace width/spacing is 4.5 mils /8.5 mils
  - ASIC and retimer footprint are simulated with actual BGA ball-out using the same PCB stackup.

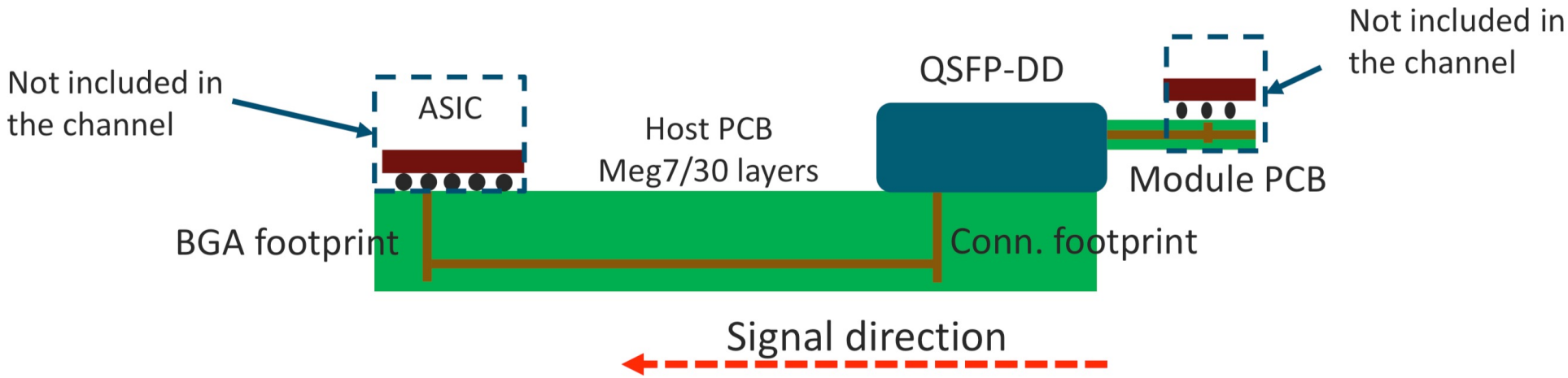


- **This analysis uses min loss channel 5a and max loss channel 5d.**



C2M TP4 Channels for Updated Analysis

- **Channel based on lim_3ck_02_0719 shown**
  - 16 pairs (8 Tx, 8 Rx) QSFP-DD SMT Connector and host PCB footprint are solved as one piece in HFSS
  - PCB stackup is 30 layers, 150mil thick, with Meg7 material
  - PCB via stub length is modelled as 10mil
  - Diff pair trace width/spacing is 4.5mil/8.5mil, 2 different trace lengths are used (2" & 9")
  - ASIC footprint are simulated with actual BGA ball-out using the same PCB stackup
  - Module CDR footprint is not included in the. Channel.



COM Code 3.1.0 Host-Module TP1a

❑ Test case I/II (13, 31 mm) ASIC packages.

Table 93A-1 parameters				
Parameter	**Setting**	**Units**	**Information**	
f_b	53.125	GBd		
f_min	0.05	GHz		
Delta_f	0.01	GHz		
C_d	[1.2e-4 0]	nF	[TX RX]	
L_s	[0.12 0]	nH	[TX RX]	
C_b	[0.3e-4 0]	nF	[TX RX]	
z_p select	[1 2]		[test cases to run]	
z_p (TX)	[13 31; 1.8 1.8]	mm	[test cases]	
z_p (NEXT)	[0 0 ; 0 0]	mm	[test cases]	
z_p (FEXT)	[13 31; 1.8 1.8]	mm	[test cases]	
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]	
C_p	[0.87e-4 0]	nF	[TX RX]	
R_0	50	Ohm		
R_d	[50 50]	Ohm	[TX RX]	
A_v	0.415	V	vp/vf=.694	
A_fe	0.415	V	vp/vf=.694	
A_ne	0.608	V		
L	4			
M	32	Samp/UI		
samples_for_C2M	100	Samp/UI		
T_O	50	mUI		
AC_CM_RMS	[0, 0]	V	[test cases]	[0.0235 0.0256]
filter and Eq				[0.015, 0.015]
f_r	0.75	*fb		[0, 0]
c(0)	0.54		min	
c(-1)	[-0.2:0.02:0]		[min:step:max]	
c(-2)	[0:0.02:0.1]		[min:step:max]	
c(-3)	[0]		[min:step:max]	
c(1)	[-0.1:0.02:0]		[min:step:max]	
N_b	4	UI		
b_max(1)	0.4		As/dffe1	
b_max(2..N_b)	[0.15 0.1 0.1]		As/dfe2..N_b	
b_min(1)	0.1		As/dffe1	
b_min(2..N_b)	[0.1 - 0.15 - 0.05]		As/dfe2..N_b	
g_DC	[-13:1:-3]	dB	[min:step:max]	
f_z	12.58	GHz		
f_p1	20	GHz		
f_p2	28	GHz		
g_DC_HP	[-3:0.5:1]		[min:step:max]	
f_HP_PZ	1.328125	GHz		
G_Qual	[-2 -9 ;-2 -12; -4 -12;-6 -13]	dB	ranges	
G2_Qual	[0 -1 -2 -3]	dB	ranges	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_C2M_host_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_eval_	
COM_CONTRIBUTION	0	logical
Local Search	2	
Operational		
VEC Pass threshold	12	db
EH_min	10	mV
ERL Pass threshold	7.3	dB
DER_0	0.00001	
T_r	0.01	ns
FORCE_TR	1	5
PMD_type	C2M	
BREAD_CRUMBS	0	logical
SAVE_CONFIG2MAT	1	logical
PLOT_CM	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	800	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0.2e-9]	[port1 port2]
TDR_W_TXPKG	1	
N_bx	0	UI
Tukey_Window	1	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	4.10E-08	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
ICN & FOM_ILD parameters		
f_v	0.445	*Fb
f_f	0.445	GHz f_r specified in first column
f_n	0.445	GHz
f_2	40	GHz
A_ft	0.600	V
A_nt	0.600	V

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[0 0.2e-9] [port1 port2]

COM Code 3.1.0 Module to Host TP4

- **Test case I/II (4, 7 mm) CDR packages.**

Table 93A-1 parameters				
Parameter	**Setting**	**Units**	**Information**	
f_b	53.125	GBd		
f_min	0.05	GHz		
Delta_f	0.01	GHz		
C_d	[1.0e-4 0]	nF	[TX RX]	
L_s	[0.12 0]	nH	[TX RX]	
C_b	[0.3e-4 0]	nF	[TX RX]	
z_p select	[1 2]		[test cases to run]	
z_p (TX)	[4 7; 0 0]	mm	[test cases]	
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]	
z_p (FEXT)	[4 7; 0 0]	mm	[test cases]	
z_p (RX)	[0 0; 0 0]	mm	[test cases]	
C_p	[0.65e-4 0]	nF	[TX RX]	
R_0	50	Ohm		
R_d	[50 50]	Ohm	[TX RX]	
A_v	0.415	V	vp/vf=.694	
A_fe	0.415	V	vp/vf=.694	
A_ne	0.608	V		
L	4			
M	32	Samp/UI		
samples_for_C2M	100	Samp/UI		
T_O	50	mUI		
AC_CM_RMS	[0, 0]	V	[test cases]	[0.0235 0.0256]
filter and Eq				[0.015, 0.015]
f_r	0.75	*fb		[0, 0]
c(0)	0.72		min	
c(-1)	-0.18		[min:step:max]	
c(-2)	0.04		[min:step:max]	
c(-3)	[0]		[min:step:max]	
c(1)	0		[min:step:max]	
N_b	4	UI		
b_max(1)	0.4		As/dffe1	
b_max(2..N_b)	[0.15 0.15 0.1]		As/dfe2..N_b	
b_min(1)	0.1		As/dffe1	
b_min(2..N_b)	[-0.15 -0.15 -0.05]		As/dfe2..N_b	
g_DC	[-13:1:-1]	dB	[min:step:max]	
f_z	12.58	GHz		
f_p1	20	GHz		
f_p2	28	GHz		
g_DC_HP	[-3:0.5:1]		[min:step:max]	
f_HP_PZ	1.328125	GHz		
G_Qual	[-1 -9 ;-1 -12; -4 -12; -5 -13]	dB	ranges	
G2_Qual	[0 -1 -2 -3]	dB	ranges	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_C2M_host_{date}\	
SAVE_FIGURES	0	logical
Port Order	[2 4 1 3]	
RUNTAG	C2M_eval_	
COM_CONTRIBUTION	0	logical
Local Search	2	
Operational		
VEC Pass threshold	9	db
EH_min	15	mV
ERL Pass threshold	7.3	dB
DER_0	0.00001	
T_r	0.0075	ns
FORCE_TR	1	5
PMD_type	C2M	
BREAD_CRUMBS	0	logical
SAVE_CONFIG2MAT	1	logical
PLOT_CM	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	800	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0.2e-9]	[port1 port2]
TDR_W_TXPKG	1	
N_bx	0	UI
Tukey_Window	1	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	4.10E-08	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5; 92.5 92.5]	Ohm
ICN & FOM_ILD parameters		
f_v	0.594	*Fb
f_f	0.594	GHz f_r specified in first column
f_n	0.594	GHz
f_2	40	GHz
A_ft	0.600	V
A_nt	0.600	V
Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*200*	mm
z_bp (NEXT)	*200*	mm
z_bp (FEXT)	*200*	mm
z_bp (RX)	*0*	mm
Include PCB	**0**	**logical**

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Floating Tap Control			
N_bg	0	0 1 2 or 3 groups	
N_bf	3	taps per group	
N_f	40	f span for floating taps	
bmaxg	0.2	DFE value for floating taps	
for TP4-->	[1.2e-4 0]	nF	[TX RX]
	[0.12 0]	nH	[TX RX]
	[0.3e-4 0]	nF	[TX RX]
	[1 2 3]		[test cases to run]
	[2 7 8]	mm	[test cases]
	[0 0 0]	mm	[test cases]
	[2 7 8]	mm	[test cases]
	[0 0 0]	mm	[test cases]
	[0 0.87e-4]	nF	[TX RX]

COM Analysis on Lim Channel 1 and 4 – ASIC to Module

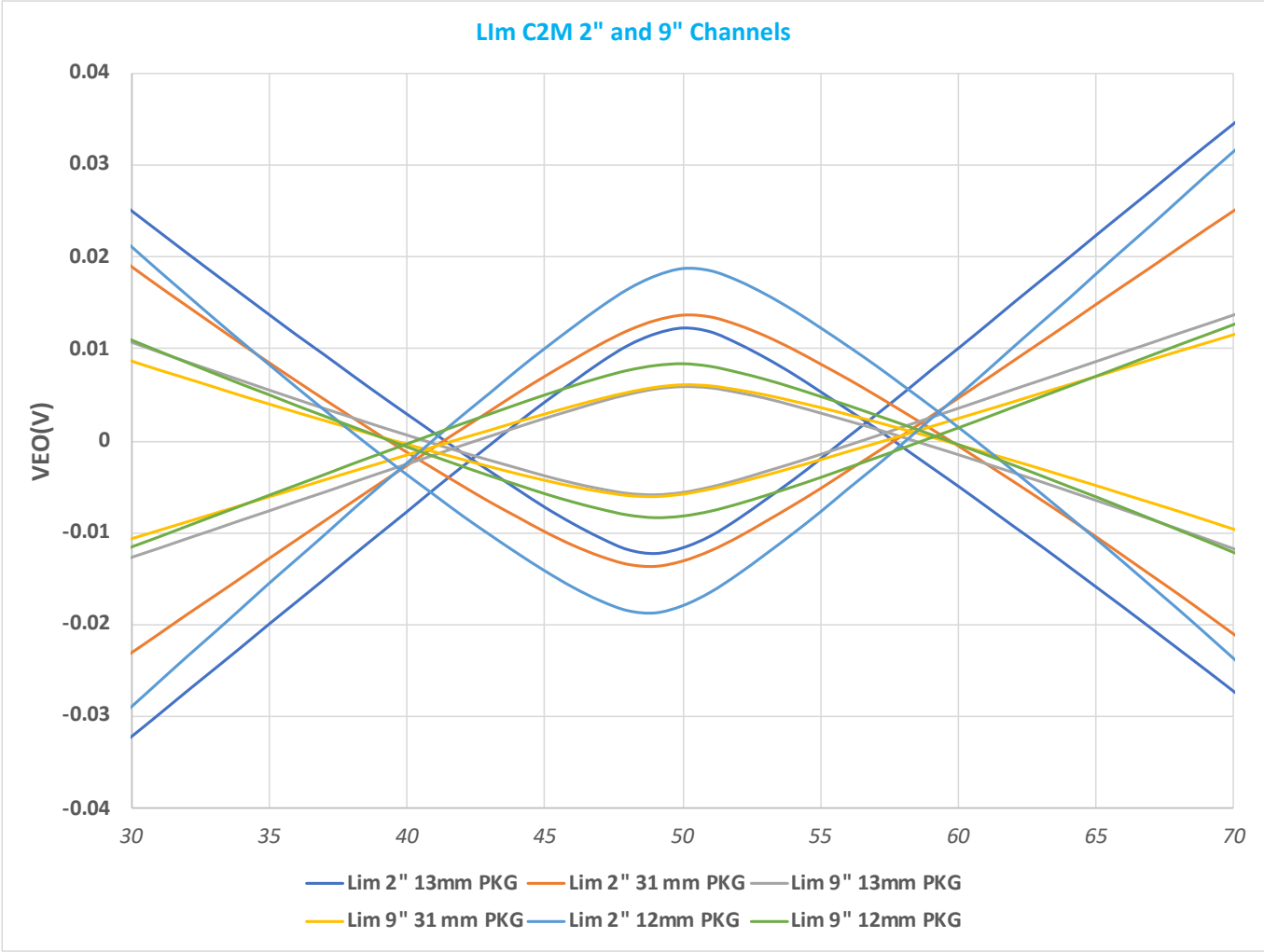
- **Lim channels include BGA footprint, via, host stripline, via, QSFP-DD connector and module module PCB**
  - Results for test case I=13 mm is pathological and consistent when timing window ts=0
  - VEO results with 50 mUI window are reduced by ~half and VEC increases by ~4 dB
- **VEO and VEC limits**
  - D1.3 window=0 mUI, VEO= 15 mV and VEC= 9 dB
  - D2.0 window +/- 50 mUI, VEO= 10 mV and VEC= 12 dB
- **VEO/VEC limits have become more difficult for host to pass with addition of timing window ts= +/- 50 mUI**
  - The VEO/VEC were to suppose to be adjusted for +/- 50 mUI window and limits have shifted the specifications!

Channel	Window	Fitted IL@26.56 GHz	IL wPKG@26.55 GHz	VEO Case I/II/III 12/13/31 mm	VEC Case I/II/III 12/13/31 mm	EW Case I/II/III 12/13/31 mm	COM Case I/II/III* 12/13/31 mm
Lim Channel 2" at TP1a ILD = 0.084, ICN = 4.0 mV ERL[11,22]= [9.1, 9.1] dB	0	5.9 dB	11.3 dB	37.5/25.5/27.3	6.8/11.1/7.8	0.19/0.14/0.18	5.3/2.83/4.5
	+/- 50 mUI	5.9 dB	11.3 dB	26.2/13.3/18.7	9.9/16.4/11.1	0.19/0.14/0.18	3.3/1.4/2.8
Lim Channel 9" at TP1a ILD = 0.066, ICN = 1.7 mV ERL[11,22]=[10.9,11.4] dB	0	14.7 dB	20.3 dB	16.7/11.8/12.1	7.2/10/8.1	0.19/0.15/0.17	5.0/3.3/4.3
	+/- 50 mUI	14.7 dB	20.3 dB	11.3/7.1/7.9	10.6/14.4/11.8	0.19/0.15/0.17	1.8/2.6/3.0

*** Per COM definition results with timing window ts=0 is only applicable.**

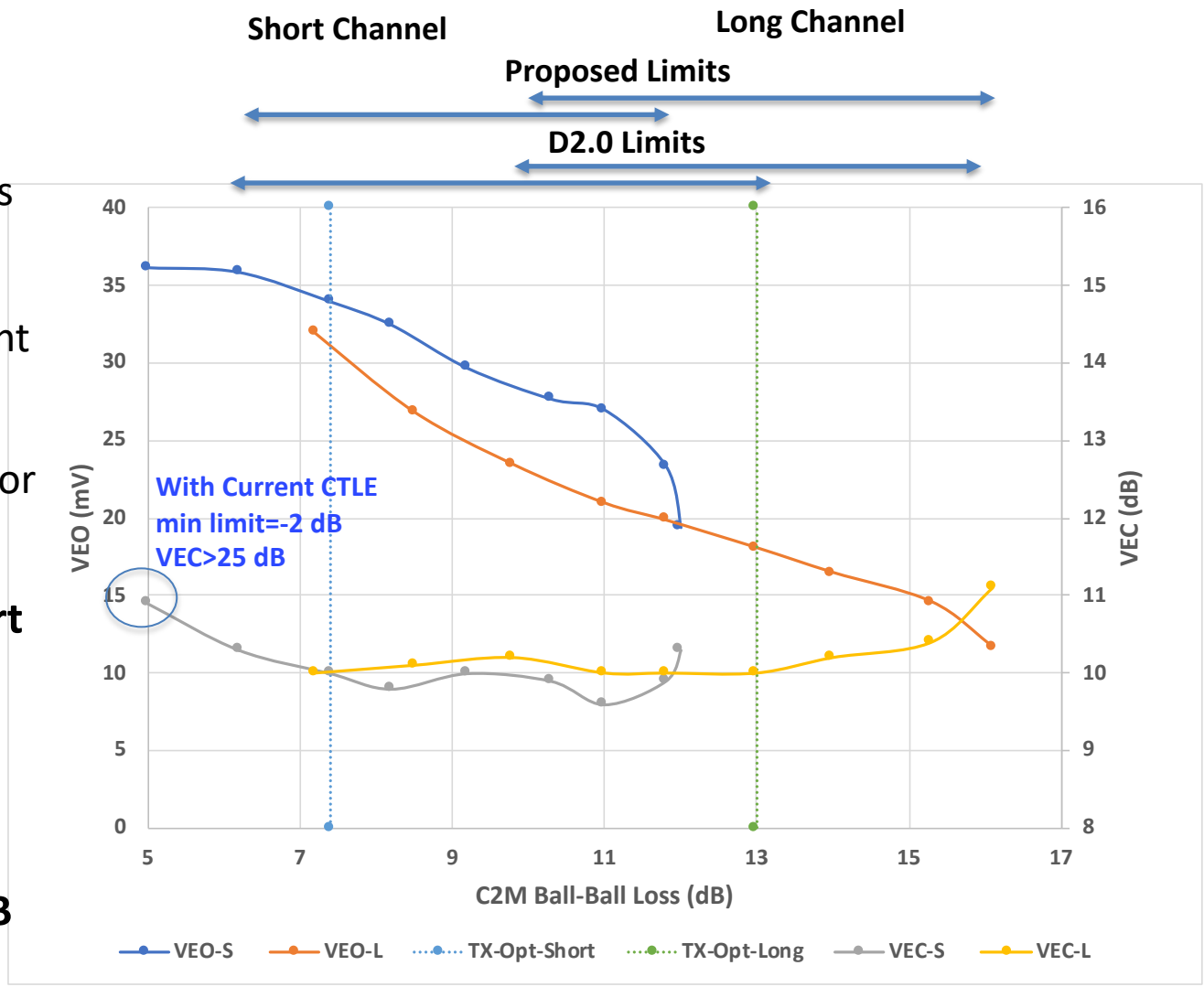
TP1a Eyes for 2” and 9” Lim Channels

- **The eye show the impact of sampling window on the VEO and associated VEC**
  - Given the eye shape there could be as much as 5 dB of VEC penalty due to +/- 50 mUI window
  - The same eye with the window may have ½ the eye opening.



M2C Short and Long Channels

- **Current D2.0 definition of TP4 short and long**
  - Short 0 – 160 mm (6.6 dB) + MTF Loss
  - Long 80 mm (3.1 dB) – 244.7 mm (9.6 dB) + MTF Loss
    - 9.6 dB + 6.6 dB MTF loss exceed max 16 dB
    - 244.7 mm should be reduced to 239.7 mm (9.4 dB)
  - Short channel max loss up to 13.2 results in significant VEC/VEO degrading
    - Propose to reduce short channel max loss to 12 dB
  - Not clear if MTF variations should be accounted or nor with current procedure explicitly specifying added trace
- **Proposed new limit for TP4 short/long adjusting short max loss and accounting for MTF loss**
  - Assumes MTF loss of 6.6 dB
    - Short range will be from 6.6 – 11.8 dB (0 – 132.6 mm)
    - Long range will be from 9.7 – 16 dB (80 – 239.7 mm)
- **If one allow short range to go to as low as 5 dB VEC> 25 dB but this issue is avoided if one adjust for 1.6 dB MTF loss difference otherwise gDC need to be reduced from -2 dB to -1 dB.**



COM Analysis on Lim Channel 1a, 2a, 2b – Module to ASIC

- **Module to ASIC package results in less of impairments compare to ASIC to module**
  - In D2.0 VEO= 15 mV and VEC= 12 dB were added replacing TBD based on timing window of ts=+/- 50 mUI
  - D2.0 VEO and VEC are inline with results below and no change is necessary
  - TP1a test point is equivalent to TP4 far end test point.

Channel	ILD, ICN, ERL	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO mV Case I/II	EW UI Case I/II	VEC dB Case I/II	COM dB Case I/ II
Lim Channel 1a * TP4 near end	ILD = 0.1, ICN = 2.8 mV ERL11=10.9 dB, ERL22=10.7 dB	5.4	6.0	30/27	0.25/0.23	12.3/13	2.4/2.3
Lim Channel 2a * TP4 near end	ILD = 0.11, ICN = 4.9 mV ERL11=11.3 dB, ERL22=11.1 dB	5.9	6.7	24/21.6	0.19/0.20	13.7/14.6	2.0/1.8
Lim Channel 1a ** +200 mm TP4 far end	ILD = 0.1, ICN = 2.8 mV ERL11=10.9 dB, ERL22=10.7 dB	15.5	16.1	18.2/15.3	0.23/0.21	8.2/9.5	4.3/3.5
Lim Channel 2a ** +200 mm TP4 far end	ILD = 0.11, ICN = 4.9 mV ERL11=11.3 dB, ERL22=11.1 dB	16.1	16.8	16.2/13.8	0.22/0.22	8.9/10.1	3.9/3.2
Lim Channel 1b ** TP4 far end	ILD = 0.1, ICN = 2.1 mV ERL11=10.6 dB, ERL22=11.7 dB	14.8	15.8	16.0/11.1	0.21/0.18	9.5/12.8	3.5/2.3
Lim Channel 2b ** TP4 Far end	ILD = 0.12, ICN = 0.70 mV ERL11=11.7 dB, ERL22=10.3 dB	15.0	16.0	17.8/11.6	0.22/0.18	8.9/12.3	3.9/2.4

*** TX FIR for short channel [0.02 -0.16 0.82 0]**

**** TX FIR for long channel [0.04 -0.18 0.78 0]**

Summary

- **With introduction of timing window ts=+/-50 mUI the VEC=12 dB and VEO=10 mV at TP1a have been relax where it will result in large % of host channels failing**
  - The agreement was not to shift the specifications in favor of the module or the host
  - The intention was to just adjust VEC/VEO for the timing window ts=+/-50 mU
  - Lim host-module channel which are well constructed failing is concerning
- **The limits at TP4/TP4 far end with VEC=12 dB and VEO=15 mV are right on**
- **Given that ASIC-TP1a and CDR-TP4 are not symmetrical interfaces**
  - ASIC package has significantly greater amount impairment compare to CDR
  - Host channel also has greater amount of impairments compare to MCB and the synthetic channel
  - Then how is it possible that the standard has identical VEC at TP1a and TP4
- **Please adjust VEC and VEO to not penalize host and significantly drive their cost up**
  - Propose limits at TP1a are: VEO=8 mV and VEC=13.5 dB.