100G C2M Simulations

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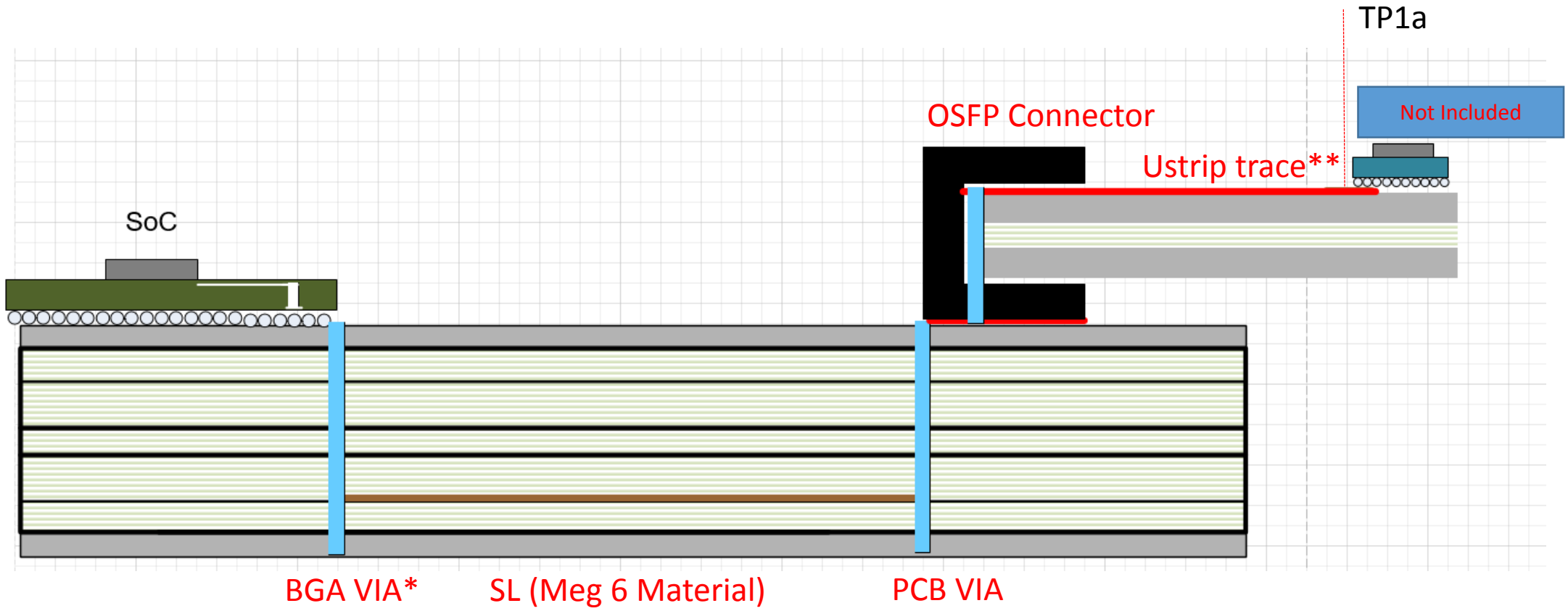
Summary

- **Goal**: Is to analyze the impact of package length on margin performance
- 93 ohm Chip to Module from Intel used
  - BGA to TP1a
  - 1 Tap DFE at DFE2 location
- Exercise swept package lengths from 1mm to 19mm
  - Only data for 6mm to 17mm shown
  - Prior analysis used 16mm package length
- 9mm package length provided the best performance
  - 7mm had the worse
  - Initial hypothesis was that 13mm would be the worst case
  - High performance variability still observed for PCB lengths shorter than 1 in
    - Package Length

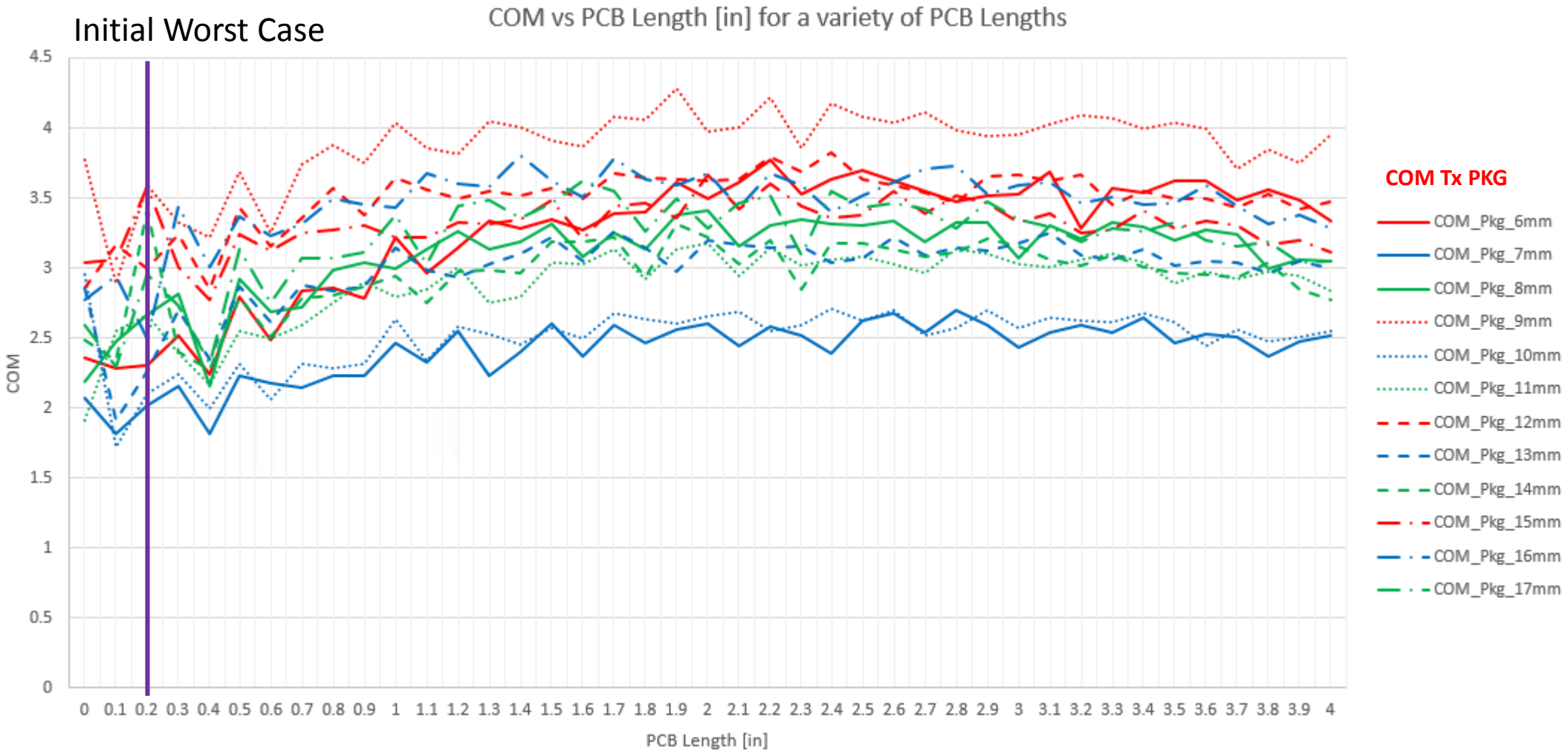
100G Chip to Module Channel



*BGA footprint and breakout are included in the channel

**Module Loss is 2.5dB @ 26.56 GHz

Initial Worst Case



BACK UP

COM SHEET

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 0]	nF	[TX RX]
L_s	[0.12 0]	nH	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	[16 30; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[16 30; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0; 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 50]	Ohm	[TX RX]
A_v	0.391	V	vp/vf=.694
A_fe	0.391	V	vp/vf=.694
A_ne	0.489	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.1]		[min:step:max]
c(-3)	[-0.04:0.02:0]		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	2	UI	
b_max(1)	0		
b_max(2..N_b)	0.2		
g_DC	[-14:1:-3]	dB	[min:step:max]
f_z	12.58	GHz	
f_p1	20	GHz	
f_p2	28	GHz	
g_DC_HP	[-3:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	0	UI	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	1		
Floating Tap Control			
N_bg	0		0 1 2 or 3 groups
N_bf	0		taps per group
N_f	40		UI span for floating taps

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\Phil\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_4TAPDFE_p_d2	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	400	
TDR_Butterworth	1	logical
beta_x	0.00E+00	
rho_x	**0.32**	
fixture delay time	0	enter sec
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92–12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	*[0.3 8206e-4 9.5909e-5]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*119*	mm
z_bp (NEXT)	*119*	mm
z_bp (FEXT)	*119*	mm
z_bp (RX)	*119*	mm

COM version: com_ieee8023_93a_270.m