A Proposed ADC-DSP Receiver Reference Model for COM

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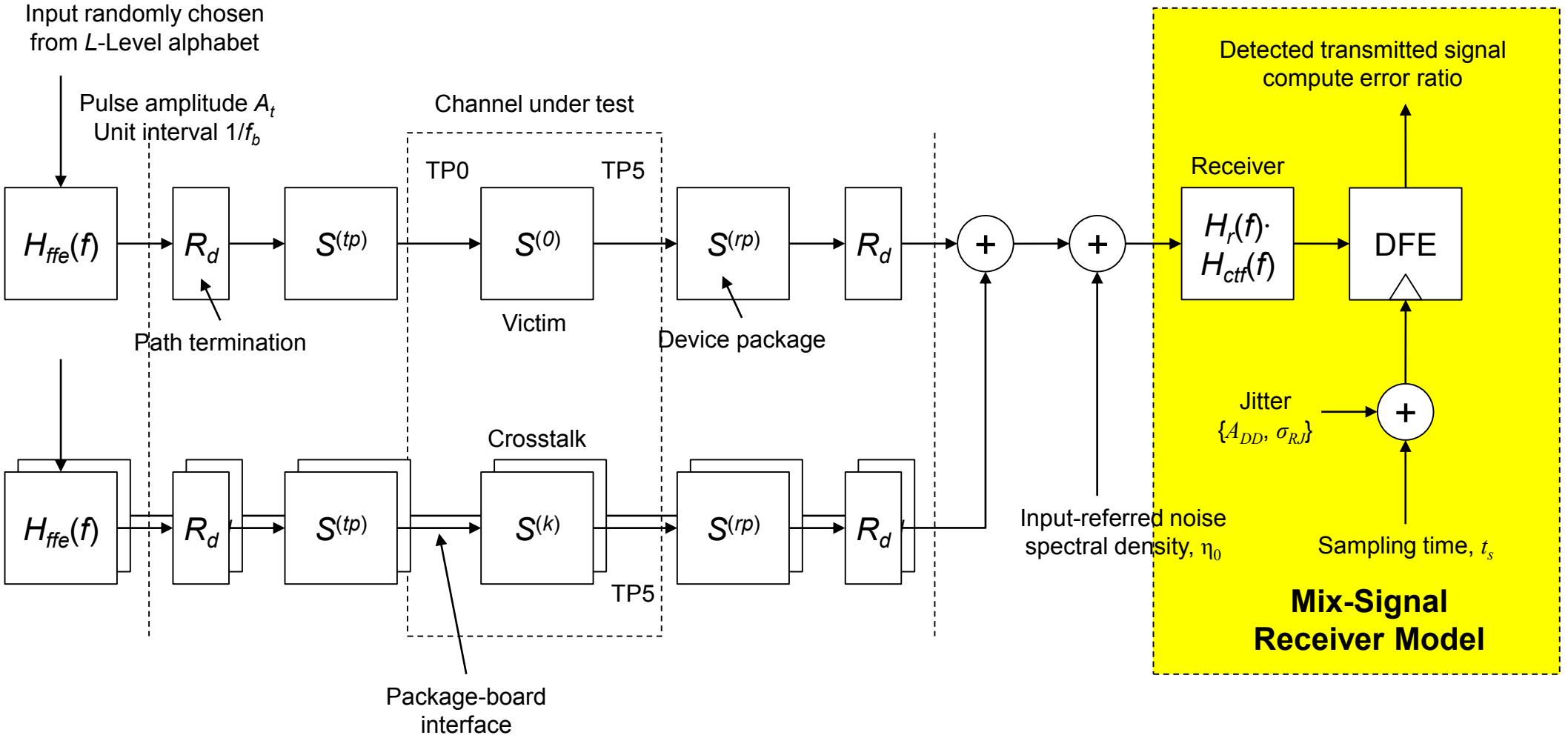
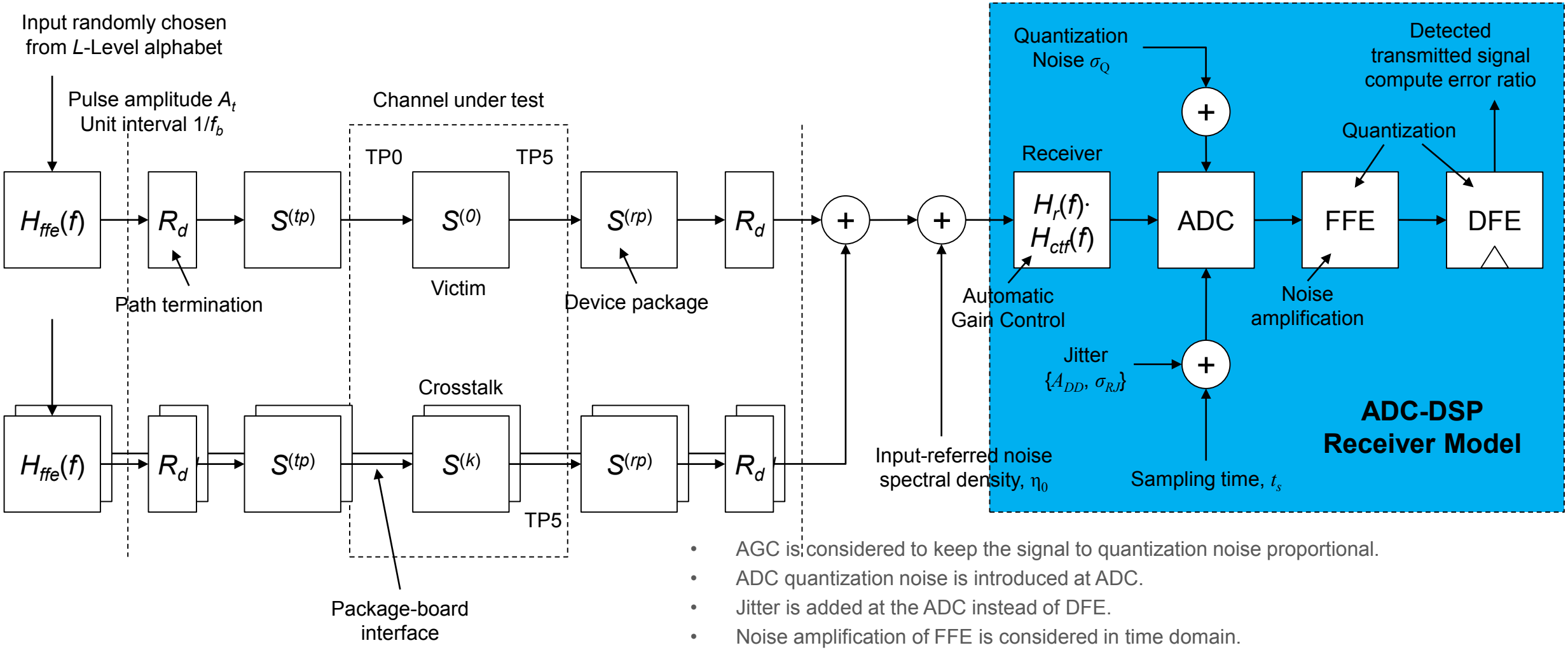


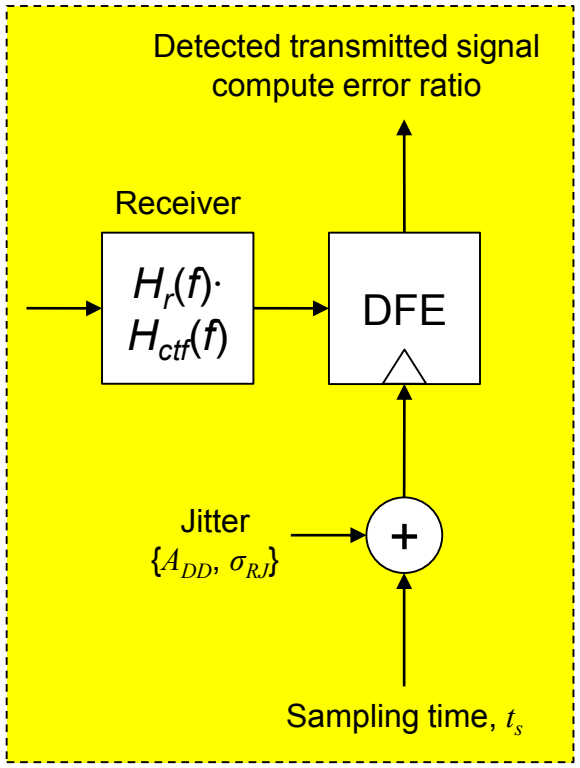
Reference: IEEE Std 802.3-2015, Annex 93A

Proposed ADC-DSP Receiver Model

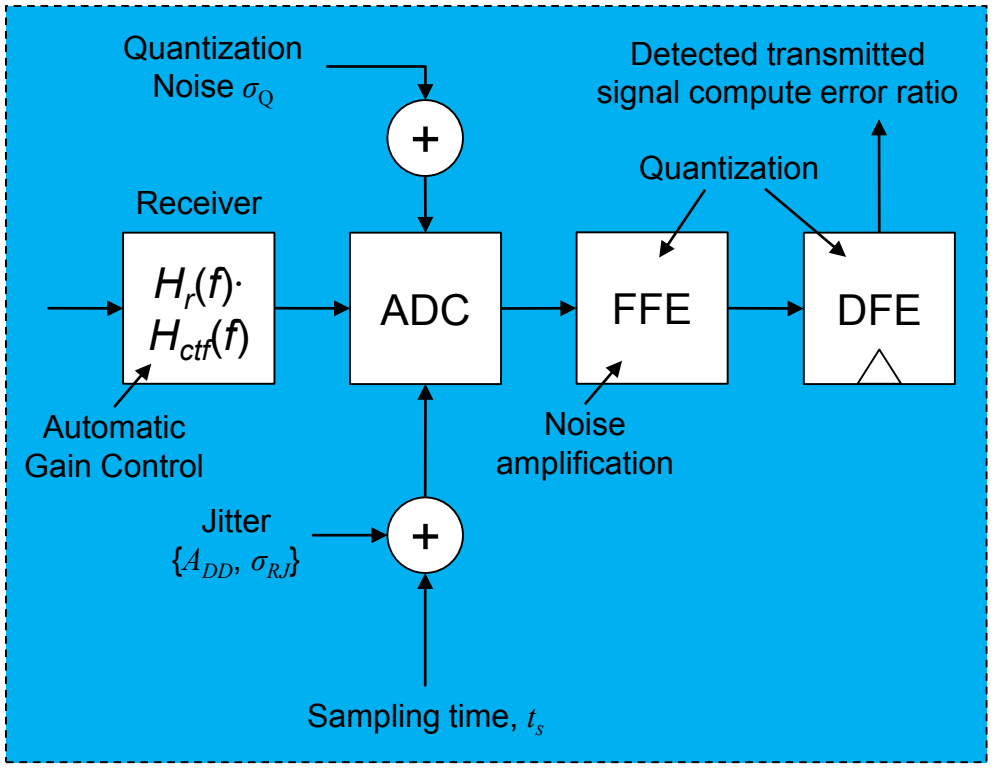


- AGC is considered to keep the signal to quantization noise proportional.
- ADC quantization noise is introduced at ADC.
- Jitter is added at the ADC instead of DFE.
- Noise amplification of FFE is considered in time domain.
- Quantized FFE and DFE models are considered both in signal and weight values.

What's New: Differences and New Parameters



Mix-Signal Receiver Model



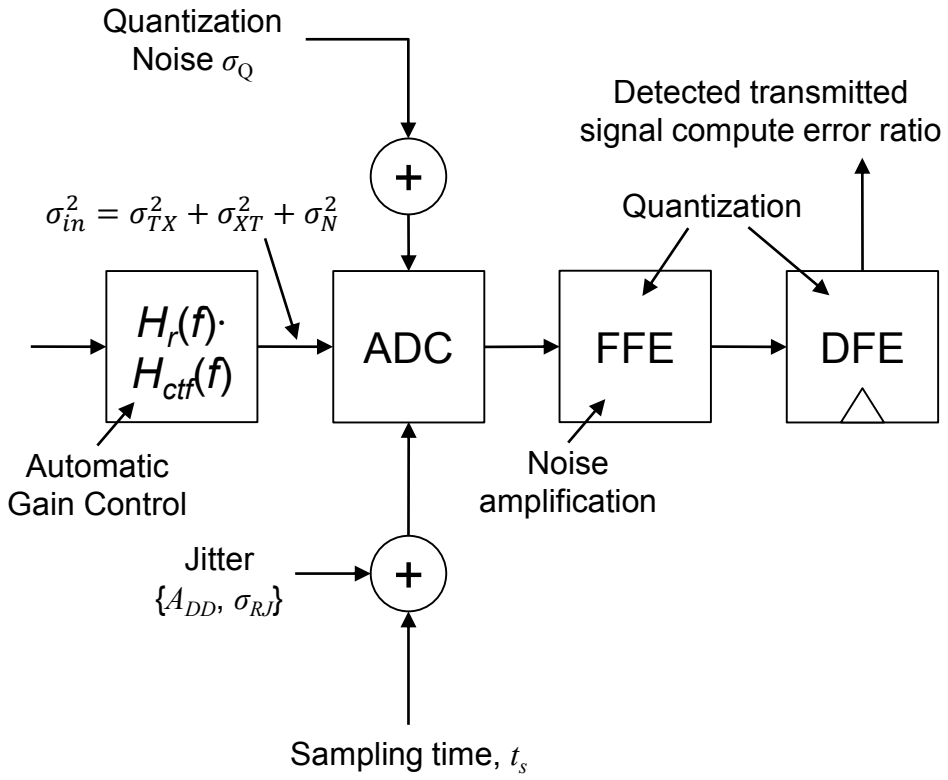
ADC-DSP Receiver Model

Parameter	Symbol	Units
ADC input amplitude.	A_{adc}	mV
ADC resolution	N_{adc}	bit
FFE weight bit number	N_{ffe}	bit
DFE weight bit number	N_{dfe}	bit
FFE Tap Number	N_f	--
FFE Pre Tap Number	$N_{pre-ffe}$	--
DFE Tap Number	N_b	--

- "Equalize then Slice" vs. "Equalize, Sample, Equalize then Slice".
- "DFE only" vs. "FFE&DFE interaction".
- "No quantization issues" vs. "ADC, FFE, DFE need quantized model."

- ADC input amplitude will impact the AGC gain.
- ADC input amplitude and resolution determine the quantization noise.
- FFE&DFE weight bit # will determine the residual ISI induced by the quantization.

ADC-DSP Reference Receiver Model: Revised Formulas



$$h_J(n) = \frac{h(t_s+(n+1/M)T_b)-h(t_s+(n-1/M)T_b)}{2/M}$$

$$\sigma_X^2 = \frac{L^2-1}{3(L-1)^2}$$

$\sigma_{in}^2 = \sigma_{TX}^2 + \sigma_{XT}^2 + \sigma_N^2$, scaled by the AGC gain.

$$\sigma_{TX}^2 = \left[h^{(0)}(t_s)\right]^2 \cdot 10^{-SNR_{TX}/10}$$

$$\sigma_Q^2 = \frac{1}{3}\left(\frac{A_{\text{adc}}}{2^{N_{\text{adc}}-1}}\right)^2$$

$$\sigma_{ISI}^2 = \sigma_X^2 \cdot \sum_i h_{ISI}^2(i)\,,$$

$$\sigma_J^2 = \left(A_{DD}^2 + \sigma_{RJ}^2\right) \cdot \sigma_X^2 \cdot \sum_n h_J^2(n)$$

$$[\sigma_m^k]^2 = \sigma_X^2 \sum_n \left[h^{(k)}\left((m/M+n)T_b\right)\right]^2$$

$$\sigma_{XT}^2 = \sum_{k=1}^{K-1}\left[\sigma_i^k\right]^2$$

$$\alpha_{\text{FFE}} = \sqrt{\sum_i \text{ffeWeight}_i^2}$$

$$\sigma_N^2 = \eta_0 \int_0^\infty \left|H_r(f)\cdot H_{ctf}(f)\right|^2 df$$

$$A_{ni}^2 = \alpha_{\text{FFE}}^2 \cdot \left(\sigma_{\text{in}}^2 + \sigma_Q^2 + \sigma_J^2\right) + \sigma_{ISI}^2$$

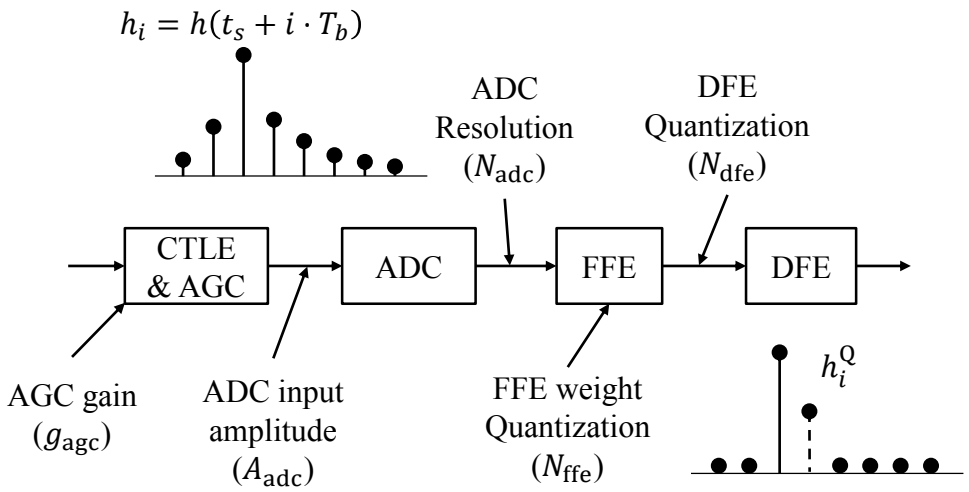
$$FOM = 20 \cdot \log_{10}\left(\frac{A_s}{A_{ni}}\right)$$

ADC resolution	5	6	7	8
σ_Q in mV @A_{adc}=200mV	3.72	1.83	**0.91**	0.45

Upper bound of σ_N:
$\sqrt{8.2\times10^{-9}\text{V}^2/\text{GHz} * 56\text{GHz}} \times 10^3 = 0.6776\text{mV}$

Quantization noise cannot be neglected

Quantized Model



AGC model:

$g_{\text{agc}} = \frac{A_{\text{adc}}}{\sum|h_i|}$, h_i is the sampled pulse response at ADC input. $H_{ctf}(f) = g_{\text{agc}} \cdot H_{ctf}^{\text{before AGC}}(f)$.

ADC model:

$$f_{\text{ADC}}(x) = \text{round}\left[x \cdot \left(\frac{2^{N_{\text{adc}}-1}}{2 \cdot A_{\text{adc}}}\right)\right] \cdot \left(\frac{2 \cdot A_{\text{adc}}}{2^{N_{\text{adc}}-1}}\right)$$

$$\sigma_{\text{Q}}^2 = \frac{1}{3}\left(\frac{A_{\text{adc}}}{2^{N_{\text{adc}}-1}}\right)^2$$

x is ADC input signal.

Quantized FFE Model:

$$f_{\text{FFE}}(x, i) = \sum_j \text{ffeWeight}_j \cdot x_{i-j}$$

$$\text{ffeWeight} = \text{round}\left[\frac{\text{ffeWeight}}{\max_i(\text{ffeWeight}_i)} \cdot 2^{N_{\text{ffe}}-1}\right] \cdot \frac{1}{2^{N_{\text{ffe}}-1}}$$

Compute the DFE weight in digital domain then do the reverse conversion.

Quantized DFE model:

$$h_Q(i) = \text{floor}\left[\frac{\sum_j\left(\text{ffeWeight}_j \cdot 2^{N_{\text{ffe}}-1}\right) \cdot \left(f_{\text{ADC}}(h(i-j)) \cdot \frac{2^{N_{\text{adc}}}-1}{2 \cdot A_{\text{adc}}}\right)}{2^{(N_{\text{adc}}+N_{\text{ffe}}-1)-N_{\text{dfe}}}}\right]$$

$$A_s^{\text{Q}} = \max\left(h_Q(i)\right),\ \text{dfeWeight}^{\text{Q}} = h_Q(idx+1 \sim idx+N_b)$$

idx is the location of A_s^{Q} in $h_Q(i)$.

$$\text{dfeWeight} = \text{dfeWeight}^{\text{Q}} \cdot \frac{2^{(N_{\text{adc}}+N_{\text{ffe}}-1)-N_{\text{dfe}}}}{2^{N_{\text{ffe}}-1}} \cdot \left(\frac{2 \cdot A_{\text{adc}}}{2^{N_{\text{adc}}-1}}\right)$$

Sampled Pulse Responses:

$$h_{FFE}(i) = \sum_j \text{ffeWeight}_j \cdot f_{\text{ADC}}\left(h(i-j)\right)$$

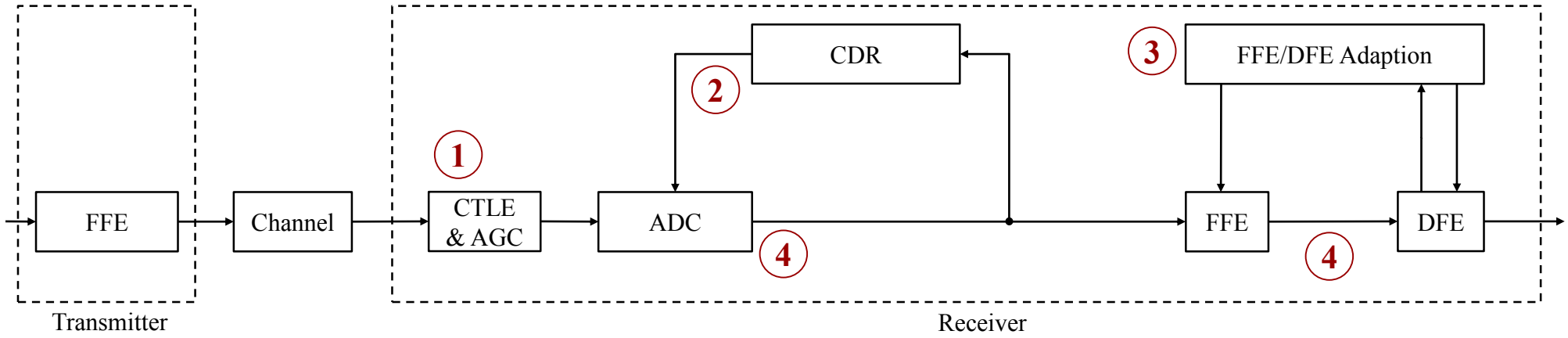
$$h_{DFE}(i) = \begin{cases} h_{FFE}(i), & i \text{ is not DFE tap} \\ h_{FFE}(i) - \text{dfeWeight}_i, & i \text{ is DFE tap} \end{cases}$$

Signal Amplitude and Residual ISI:

$A_s = \max(h_{DFE}(i))/(L-1)$, Eye height, align with Annex 93A

$$h_{ISI}(i) = \begin{cases} 0, & i \text{ is main tap} \\ h_{DFE}(i), & i \text{ is not main tap} \end{cases}$$

Further Considerations



① CTLE bandwidth. The peak frequency of 802.3cd CTLE is ~32GHz@53.125GBd.
- Introduce a scaling factor (<=1) of f_b in CTLE formula?

② CDR locking phase.
- Pulse response peak [@ADC input/CTLE output] or MM-PD locking phase or Multiple locking phase?

③ FFE&DFE adaption, Interaction of FFE and DFE.
- The choice of Pos1 to Main ratio (i.e. b_{max}). Fixed or Adaptive?

④ Quantization issues
- ADC input amplitude (Automatic gain control, AGC) & resolution
- Quantized FFE & DFE model.

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