P802.3ck D1.4
Open technical issues and concerns

Matt Brown, Huawei, 802.3ck Chief Editor

Introduction

- In order to gain approval to move to Working Group ballot at the March Plenary meeting, Draft 1.5 must have no remaining technical issues.
- We must address the following in Draft 1.4
  - Provide a value for any TBD relating to a normative parameter.
  - Provide updated content for any normative method that is incomplete or broken.
  - Remove any editor's notes implying incomplete specifications.
- Open technical issues are listed on subsequent slides.
- Please point out any unlisted open technical issues.

Legend

Subclause/Page/Line	Description
subclause/page/line	Issues that are highlighted in red are ones that must be addressed to ensure technical completeness.
subclause/page/line	Issues that are highlighted in orange are ones that could remain, but should be addressed if possible to reduce concerns during WG approval.
subclause/page/line	Issues that are highlighted in yellow are ones relating to placeholders with missing content, but are not essential to any normative specifications.

Clause 162 and Annexes 162B/C

Subclause/Page/Line	Description
162.9.3/152/30	TBD: Common-Mode to Differential Mode Return Loss (TX at TP2) Table 162-10 and PICS (162.14.4.3/175/43)
162.9.4/158/16	TBD: Differential to Common-Mode Return Loss (RX at TP3) Table 162-13 and PICS (162.14.4.4/176/17)
162.11/163/17	TBD: Cable Assembly ERL, Table 162-16 and PICS (162.14.4.5/176/45)
162B.1.3.1/262/36	TBD: Mated test fixture FOM_ILD
162B.1.3.1/262/43	TBD: Mated test Fixture ERL, also PICS (162B.2.4/269/22)
162C.2.2/275/12	Missing receptacle/plug graphic in Figures 162C-3/4. *Not essential for technical completeness.*

Clause 163, Annex 163B

Subclause/Page/Line	Description
163.9.3/187/41	TBD: RX differential to common-mode return loss, Table 163-8
163.10.4/192/44	TBD: Channel differential to common-mode conversion loss
163B.2/291/18	TBD (informative): Example test fixture: TX steady-state voltage, Vf *Not essential for technical completeness.*
163B.2/291/20	TBD (informative): Example test fixture: TX linear fit pulse peak, Vpeak *Not essential for technical completeness.*

Annex 120F

Subclause/Page/Line	Description
120F.3.1.2/214/34	Editor's note: confirmation of TX c(-3) tap
120F.3.1.2/218/44	Editor's note: confirmation of insertion loss for stressed input test 2 (high loss) Related to channel IL below
120F.4.2/222/4	Editor's note: confirmation of channel insertion loss Related to test 2 IL above
120F.4.3/223/5	TBD: Channel ERL, also PICS table (120F.5.4.3/227/29)

Annex 120G

Subclause/Page/Line	Description
120G.3.1/231/33	Editor's note: Confirmation of host output AC CM noise, PP voltage, RLCC
120G.3.1.5/233/17	TBD: Host output EH/VEC crosstalk parameters (4x)
120G.3.2/234/17	TBD: Module output ERL, Table 120G-3
120G.3.2/234/41	Editor's note: Confirmation of module output AC CM noise
120G.3.2.2/235/33	TBD: Module output EH/VEC crosstalk parameters (2x)
120G.3.3.2.1/238/54	TBD: Host stressed input, crosstalk parameters (2x)
120G.3.4/240/17	TBD: Module input ERL, Table 120G-9
120G.3.4.1.1/242/2	TBD: Module stressed input, crosstalk parameters (2x)
120G.5.2/246/38	Editor's note: Confirmation of EH/VEC value due to revised methodology

Thanks!