C2M Measurement Methodology

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Overview

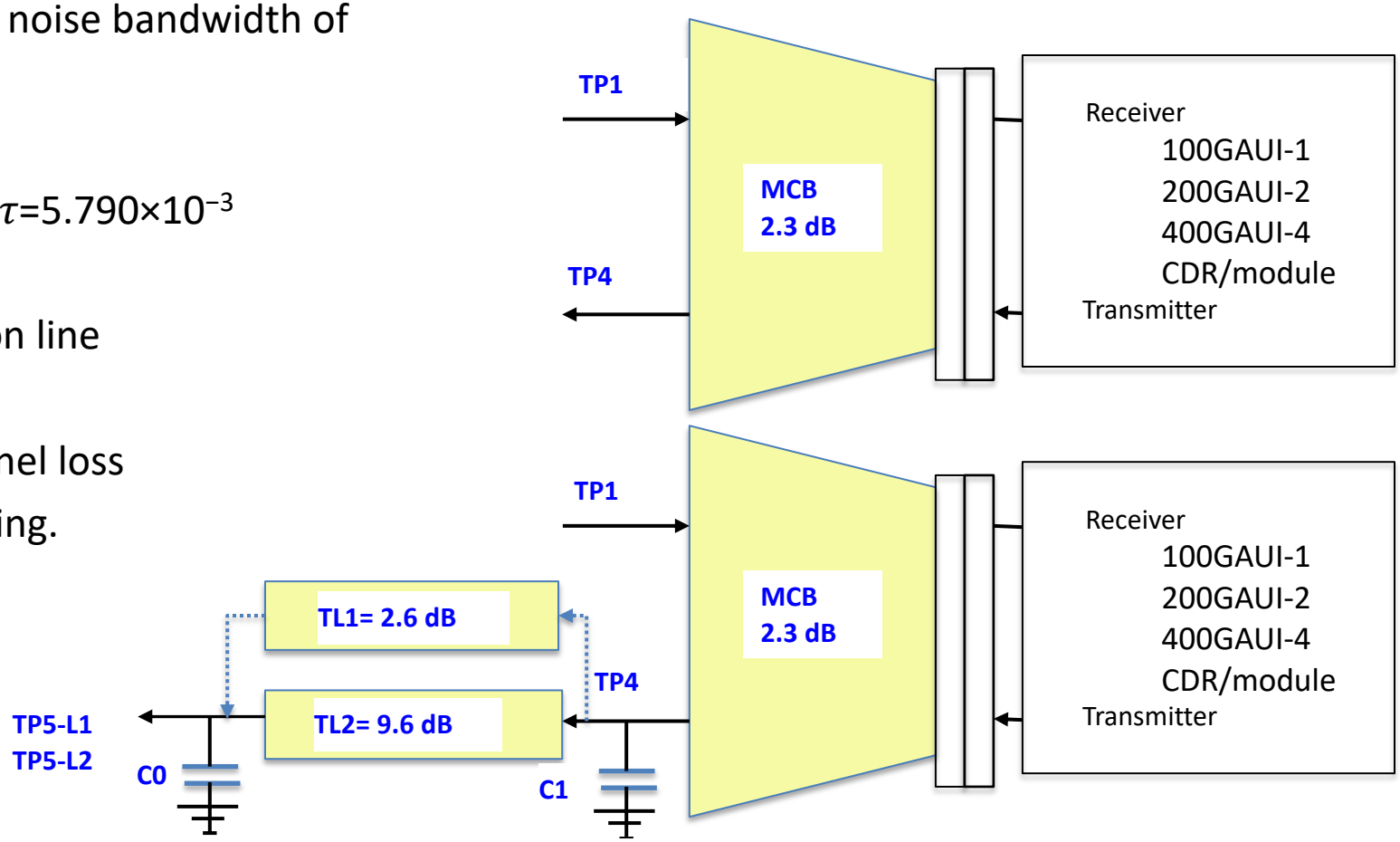
- **Some of the material presented here originally presented in following presentations**
  - Results included are for several equalizer types and before we voted for 4T DFE during Nov. 2019 plenary meeting
  - http://www.ieee802.org/3/ck/public/19_11/ghiasi_3ck_01a_1119.pdf
  - http://www.ieee802.org/3/ck/public/19_11/ghiasi_3ck_03_1119.pdf
- **Module to ASIC test methodology**
  - Purpose to use CR (C0, C1) to add some impairment to the MCB accounting for long barrel vias
- **Module output measurement test points**
  - Is TP4 and TP5 sufficient
- **COM analysis at TP4, TP5x**
  - Penalty associated from fixed module TX FIR
- **Summary.**

Module to ASIC Test Methodology

- **Unlike ASIC-Module the Module-ASIC output at TP4 and TP5 measured with compliance board and reference trace typically has COM >6 dB dB with 4T DFE receiver**
  - If one replaces module compliance board with realistic host with long barrel via and a short stub then COM can drop by ~ 2 dB
  - COM can drop to 2-3 dB for realistic channel if one include the ASIC package
- **Instead of just measuring TP5 with bare reference trace and getting a very optimistic COM, it is recommended to use benartsi_3ck_01a_0719 method initially purposed for CR end to end links with (C0, C1)= (29, 19 fF) for C2M TP5 measurements**
- **Given that there is no way to add (C0, C1) to TP4 unless one create single lumped element it is purposed to expand TP5 test point into**
  - TP5-L1 (long 68 mm) add ~ 3 dB to the MCB
  - TP5-L2 (short 215 mm) max loss 16 dB
- **There will be total of 3 test conditions module output**
  - TP4, TP5-L1, TP5-L2 for eye measurement
  - TP4 for ERL measurement.

TP1, TP4 and TP5 Test Points

- **TP4/TP5 measurements are with addition of 0.577 nV^2/GHz (TBD) noise to account for BGA crosstalk**
  - The equivalent 0.577 mV RMS noise is for noise bandwidth of 53.125*0.75 = 39.84 GHz
- **Transmission line parameters**
  - $\gamma 0=0$, $a1 =3.8206\times10^{-4}$, $a2 =9.5909\times10^{-5}$, $\tau=5.790\times10^{-3}$
  - TP4 is MCB output measurement
  - TP5-L1 measured with 68 mm transmission line
    - TP5-L1 is used to set module TX FIR
  - TP5-L2 measured with 244 mm max channel loss
    - TP5-L2 must pass with TP5-L1 TX setting.



COM 2.70 Module to Host (CDR PKG 2-8 mm)

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5]	Ohm
C_d	[1e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12 0]	nF	[TX RX]		Port Order	[2 4 1 3]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[2 8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[2 8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	215	mm
z_p (RX)	[0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	215	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	215	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 50]	Ohm	[TX RX]		Include PCB	1	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.7	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	0	UI			N_bx	4	UI				
b_max(1)	0.75				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	4	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.15										
ffe_backoff	1										

COM 2.75 Module to Host (CDR PKG 2-8 mm) with addition of C0/C1

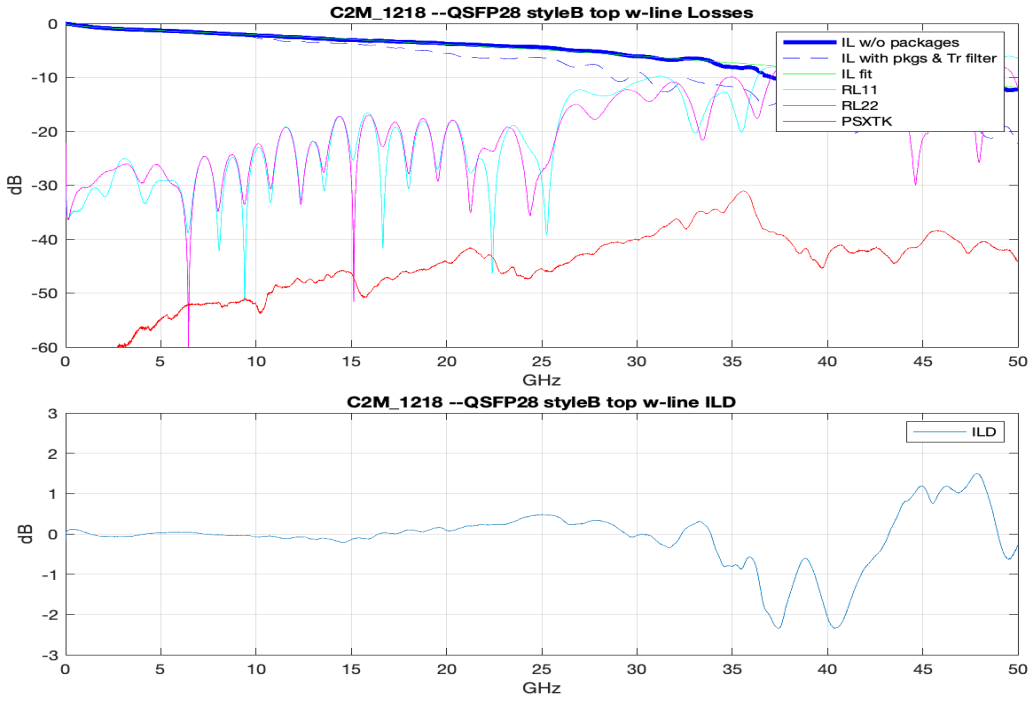
Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5]	Ohm
C_d	[1e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12 0]	nF	[TX RX]		Port Order	[2 4 1 3]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[2 8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[2 8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	68	mm
z_p (RX)	[0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	68	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	68	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 50]	Ohm	[TX RX]						C_0	[0.29e-4]	nF
A_v	0.41	V			TDR and ERL options				C_1	[0.19e-4]	nF
A_fe	0.41	V			TDR	1	logical		Include PCB	1	logical
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.7	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	0	UI			N_bx	4	UI				
b_max(1)	0.75				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.37E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	32.5	dB				
ffe_post_tap_len	4	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.15										
ffe_backoff	1										

COM 2.70 Module to Host at Slicer T-Coil Model (CDR PKG 2-8 mm)

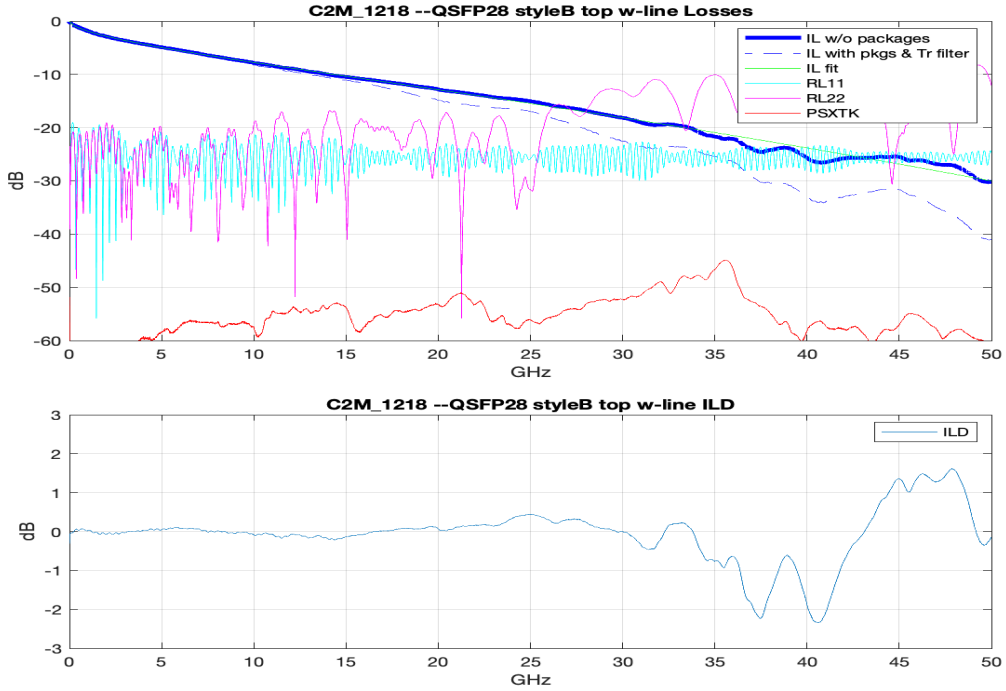
Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5; 92.5 92.5]	Ohm
C_d	[1e-4 1.2e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.1 0.12]	nF	[TX RX]		Port Order	[2 4 1 3]			Table 92–12 parameters		
C_b	[0 0.3e-4]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[2 8; 0.01 0.01]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 8; 0.01 0.01]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[2 8; 0.01 0.01]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	215	mm
z_p (RX)	[13 29; 1.8 1.8]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	215	mm
C_p	[0.65e-4 0.87e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	215	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 45]	Ohm	[TX RX]		Include PCB	1	logical				
A_v	0.41	V			TDR and ERL options						
A_fe	0.41	V			TDR	1	logical				
A_ne	0.6	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb		0.8	TDR_Butterworth	1	logical				
c(0)	0.65		min		beta_x	2.53E+09					
c(-1)	[-0.2:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.02:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	4	UI			N_bx	4	UI				
b_max(1)	0.75				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-14:0.5:-4]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	18.55345912	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	28.2	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-3:0.5:-1]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	1.3275	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	0	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.2										
ffe_backoff	1										

TP4/TP5 Analysis with Yamaichi QSFP-56 Mated Boards

Mated board IL = 5.2 dB
Total IL with 8 mm PKG=8.0 dB



Mated board + 220 mm trace IL = 16.1 dB
Total IL with 8 mm PKG=18.6 dB



Yamaichi QSFP56 Mated Board Near End and Far End Results

- **Mated board COM with addition of PCB trace and C0/C1***
  - Near end results with addition of 68 mm trace improves COM ~0.7 dB but after adding C0/C1 degrades COM by 0.5 dB
  - Far end TP5 results degrades by 0.5 dB with addition of C0/C1.

Channel	Equalizer	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO Case I	VEO Case II	VEC Case I	VEC Case II	COM Case I	COM Case II
Yamaichi QSFP56 FOM ILD = 0.18 ICN = 5.2 mV ERL11=14.6 dB ERL22=10.7 dB TP4/Nearend	5T FFE	5.2	8.0	53.2	53	6.2	6.1	5.8	6.0
	4 DFE COM	5.2	8.0	55.1	53	6.9	6.7	5.2	5.4
	5T FFE + 68 mm	8.6	11.1	42.8	35.9	5.3	5.4	6.8	6.7
	4DFE + 68 mm	8.6	11.1	44.2	42.7	5.7	5.6	6.4	6.4
	5T FFE+68 mm+C0/C1	8.6	11.6	35.9	39.2	6.2	6.7	5.9	5.4
	4T DFE+68 mm+C0/C1	8.6	11.6	39.3	35.7	6.4	7.2	5.6	5.0
Yamaichi QSFP56 FOM ILD = 0.17 ICN = 1.6 mV ERL11=14.6 dB ERL22=10.7 dB TP5	5T FFE+215mm	15.8	18.6	21.0	18.0	5.3	5.7	6.8	6.3
	4T DFE+215mm	15.8	18.6	28.2	25.8	5.2	5.6	6.9	6.5
	5T FFE+215mm+C0/C1	15.8	19.2	16.9	16.3	6.5	6.3	5.6	5.8
	4T DFE+215mm+C0/C1	15.8	19.2	25.4	22.9	5.8	6.4	6.2	5.7

* Using CR COM reduced TX SNR and increased eta_0.

Yamaichi QSFP56 Mated Board at Slicer

- **Mated board COM with addition of PCB trace and C0/C1***
  - With addition of C0/C1 COM decreases by about 1.5 dB
  - The Slicer behavior with addition of C0/C1 is now more similar to Lim channels which include vias and BGA footorint
    - But Lim 2” channel still 0.7 dB worse even with addition of C0/C1.

Channel	Equalizer	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO Case I	VEO Case II	VEC Case I	VEC Case II	COM Case I	COM Case II
Yamaichi QSFP56 FOM ILD = 0.18 ICN = 5.2 mV ERL11=14.6 dB ERL22=10.7 dB At Slicer	5T FFE	5.2	12.8	36.3	27.9	8.6	6.7	4.0	5.3
	4 DFE COM	5.2	12.8	27.7	22.5	8.2	6.2	4.3	5.8
	5T FFE + 68 mm	8.6	15.5	36.3	27.9	8.6	6.7	4.0	5.3
	4DFE + 68 mm	8.6	15.5	35.3	38.0	8.8	6.7	3.9	5.4
	5T FFE+68 mm+C0/C1	8.6	16.4	16.3	16.5	12.1	8.7	2.5	4.0
	4T DFE+68 mm+C0/C1	8.6	16.4	20.8	22.7	10.5	8.1	3.1	4.4
Yamaichi QSFP56 FOM ILD = 0.17 ICN = 1.6 mV ERL11=14.6 dB ERL22=10.7 dB At Slicer	5T FFE+215mm	15.8	23.2	12.7	11.1	6.9	7.9	5.2	4.5
	4T DFE+215mm	15.8	23.2	15.7	13.0	6.5	6.7	5.6	5.4
	5T FFE+215mm+C0/C1	15.8	24.3	7.5	7.7	11.3	9.2	2.7	3.7
	4T DFE+215mm+C0/C1	15.8	24.3	14.3	10.6	9.0	7.8	3.8	4.6

* Using CR COM reduced TX SNR and increased eta_0.

Min/Max Channel Loss at Slicer with Yamaichi QSFP-56 Mated Boards

- **COM at slicer for min loss 5.2 dB channel and max loss 16 dB channel are about the same!**
  - The optimum TX FIR for 5T FFE and 4T DFE for Yamaichi mated board with 68 mm and C0/C1 were [0.04, -0.2, 0.76, 0]
  - The follow on simulations TX FIR was set to [0.04, -0.18, 0.72, -0.04].

Channel	Equalizer	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO Case I	VEO Case II	VEC Case I	VEC Case II	COM Case I	COM Case II
Yamaichi QSFP56 At TP5 FOM ILD = 0.18 ICN = 5.2 mV ERL11=14.6 dB ERL22=10.7 dB Optimum TX FIR	5T FFE	5.2	12.8	36.3	27.9	8.6	6.7	4.0	5.3
	4 DFE COM	5.2	12.8	27.7	22.5	8.2	6.2	4.3	5.8
	5T FFE + 68 mm	8.6	15.5	36.3	27.9	8.6	6.7	4.0	5.3
	4DFE + 68 mm	8.6	15.5	35.3	38.0	8.8	6.7	3.9	5.4
	5T FFE+68 mm+C0/C1	8.6	16.4	16.3	16.5	12.1	8.7	2.5	4.0
	4T DFE+68 mm+C0/C1	8.6	16.4	20.8	22.7	10.5	8.1	3.1	4.4
Yamaichi QSFP56 At Slicer FOM ILD = 0.17 ICN = 1.6 mV ERL11=14.6 dB ERL22=10.7 dB Optimum TX FIR	5T FFE+215mm	15.8	23.2	12.7	11.1	6.9	7.9	5.2	4.5
	4T DFE+215mm	15.8	23.2	15.7	13.0	6.5	6.7	5.6	5.4
	5T FFE+215mm+C0/C1	15.8	24.3	7.5	7.7	11.3	9.2	2.7	3.7
	4T DFE+215mm+C0/C1	15.8	24.3	14.3	10.6	9.0	7.8	3.8	4.6

COM Analysis on Lim Channel 1 and 4 – Module to ASIC

- **Lim 2” or 9” host PCB with QSFP-dd connector, mid-depth via, and ASIC foot printed included**
  - Optimum TX FIR is the setting for Yamaichi mated board + 68 mm with CR C0/C1 included
  - Sub-optimum TX FIR has about 0.5 dB penalty on 5T FFE and 4T DFE at TP5!

Channel	Equalizer	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO Case I	VEO Case II	VEC Case I	VEC Case II	COM Case I	COM Case II
Lim Channel 2” at TP5 FOM ILD = 0.16 ICN = 3.7 mV ERL11=12.3 dB, ERL22=9.3 dB Optimum TX FIR	5T FFE	5.9	8.6	49.7	47.5	6.6	6.4	5.5	6.0
	5T FFE + 1DFE	5.9	8.6	51.6	50.7	7.1	6.7	5.0	5.3
	4T DFE	5.9	8.6	51.1	50.7	7.1	6.8	5.0	5.8
	10T FFE	5.9	8.6	51.4	45.2	6.3	5.9	5.7	6.1
Lim Channel 2” at TP5 FOM ILD = 0.16 ICN = 3.7 mV ERL11=12.3 dB , ERL22=9.3 dB TX FIR=[0.04, -0.18, 0.74, -0.04]	5T FFE	5.9	8.6	43.7	40.5	7.1	7.0	5.0	5.2
	5T FFE + 1DFE	5.9	8.6	38.1	37.1	8.3	8.0	4.2	4.4
	4T DFE	5.9	8.6	37.8	38.1	8.4	8.0	4.2	4.4
	10T FFE	5.9	8.6	44.9	42.1	6.9	6.6	5.2	5.5
Lim Channel 9” at TP5 FOM ILD = 0.13 ICN = 1.44 mV ERL11=11.8 dB, ERL22=14.8 dB Optimum TX FIR	5T FFE	14.8	16.8	20.8	22.4	6.2	6.5	5.8	5.5
	5T FFE + 1DFE	14.8	16.8	30.2	26.0	5.7	6.1	6.3	5.9
	4T DFE	14.8	16.8	28.2	24.7	5.8	6.1	6.2	5.9
	10T FFE	14.8	16.8	21.1	19.5	5.9	5.8	6.1	6.2
Lim Channel 9” at TP5 FOM ILD = 0.13 ICN = 1.44 mV ERL11=11.8 dB, ERL22=14.8 dB TX FIR=[0.04, -0.18, 0.74, -0.04]	5T FFE	14.8	16.8	23.3	19.2	6.4	6.6	5.6	5.5
	5T FFE + 1DFE	14.8	16.8	25.3	24.8	6.2	6.2	5.9	5.8
	4T DFE	14.8	16.8	24.5	25.0	6.2	6.1	5.8	5.9
	10T FFE	14.8	16.8	24.1	24.5	6.2	6.1	5.8	5.9

COM Analysis on Lim Channel 1 and 4 – Module to ASIC

- **Lim 2” or 9” host PCB with QSFP-dd connector, mid-depth via, and ASIC foot printed included**
  - Non-optimum TX FIR is the optimum setting for Yamaichi mated board + 68 mm with CR C0/C1 included
  - The 5T FFE has negligible penalty for sub-optimum TX FIR but the 4T DFE has about 0.5 dB penalty at the slicer!

Channel	Equalizer	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO Case I	VEO Case II	VEC Case I	VEC Case II	COM Case I	COM Case II
Lim Channel 2” At Slicer FOM ILD = 0.16 ICN = 3.7 mV ERL11=11.3 dB, ERL22=10.5 dB TX FIR Optimum	5T FFE	5.9	14.3	12.8	26.5	14.4	7.2	1.8	4.5
	5T FFE + 1DFE	5.9	14.3	16.4	32.2	14.9	7.1	1.7	5.7
	4T DFE	5.9	14.3	16.4	32.2	14.9	7.1	1.7	5.1
	10T FFE	5.9	14.3	18.0	23.1	11.1	6.7	2.8	5.3
Lim Channel 2” At Slicer FOM ILD = 0.16 ICN = 3.7 mV ERL11=11.3 dB, ERL22=10.5 dB TX FIR=[0.04, -0.18, 0.74, -0.04]	5T FFE	5.9	14.3	12.1	26.8	14.5	7.4	1.8	4.9
	5T FFE + 1DFE	5.9	14.3	11.8	29.0	16.6	7.4	1.4	4.8
	4T DFE	5.9	14.3	11.9	29.0	16.6	7.4	1.4	4.8
	10T FFE	5.9	14.3	18.9	23.8	11.1	7.0	2.8	5.2
Lim Channel 9” at Slicer FOM ILD = 0.13 ICN = 1.44 mV ERL11=11.8 dB, ERL22=14.8 dB TX FIR Optimum	5T FFE	14.8	23.0	8.0	12.7	11.9	7.0	2.5	5.1
	5T FFE + 1DFE	14.8	23.0	18.6	17.1	7.6	6.3	4.5	5.8
	4T DFE	14.8	23.0	16.9	14.1	8.5	6.5	4.1	5.6
	10T FFE	14.8	23.0	8.2	12.5	10.3	6.5	3.2	5.6
Lim Channel 9” At Slicer FOM ILD = 0.13 ICN = 1.44 mV ERL11=11.8 dB, ERL22=15.1 dB TX FIR=[0.04, -0.18, 0.74, -0.04]	5T FFE	14.8	23.0	10.4	12.9	12.2	7.1	2.4	5.1
	5T FFE + 1DFE	14.8	23.0	14.8	17.4	9.2	6.3	3.7	5.7
	4T DFE	14.8	23.0	14.0	13.9	9.7	6.5	3.5	5.5
	10T FFE	14.8	23.0	8.9	11.7	10.4	6.5	3.1	5.6

Summary

- **Propose to measure module output per CR method with addition of capacitors (C0, C1)**
  - TP4 measured directly
  - TP5-L1 measured with addition of (C0, C1) + 68 mm trace
  - TP5-L2 measured with addition of (C0, C1) + 215 mm trace
- **Module TX FIR is set based on TP5-L1 setting**
  - TP4 and TP5 eye measurement must pass with module TX FIR setting optimized for TP5-L1
  - For Lim C2M channel there is about 0.3 dB of penalty if the module TX FIR is optimized for TP5-L1
- **For Lim and Yamaichi MCB/HCB one constructs module-ASIC link the COM at slicer can be as low as 1.7 dB with 4T DFE due to short package reflection, which is similar to what has been observed on the ASIC-Module direction**
  - If the ASIC SerDes only has 4T DFE would need to operate with < 3 dB COM or alternatively may have additional enhancements.