Update COM Analysis with Rectangular Window

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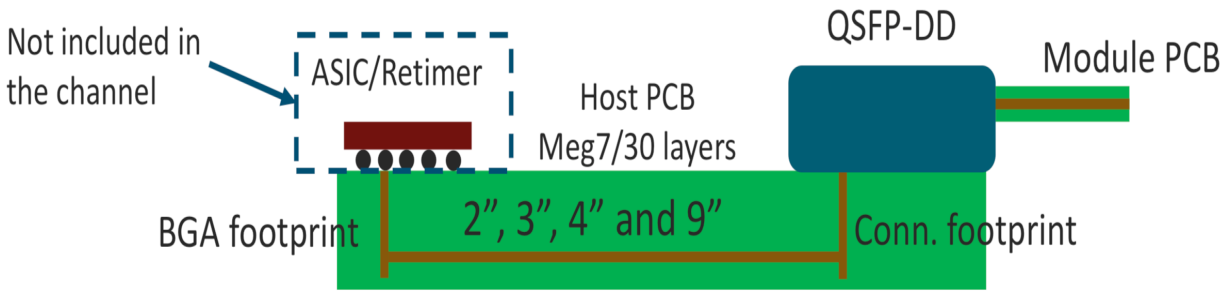
Overview

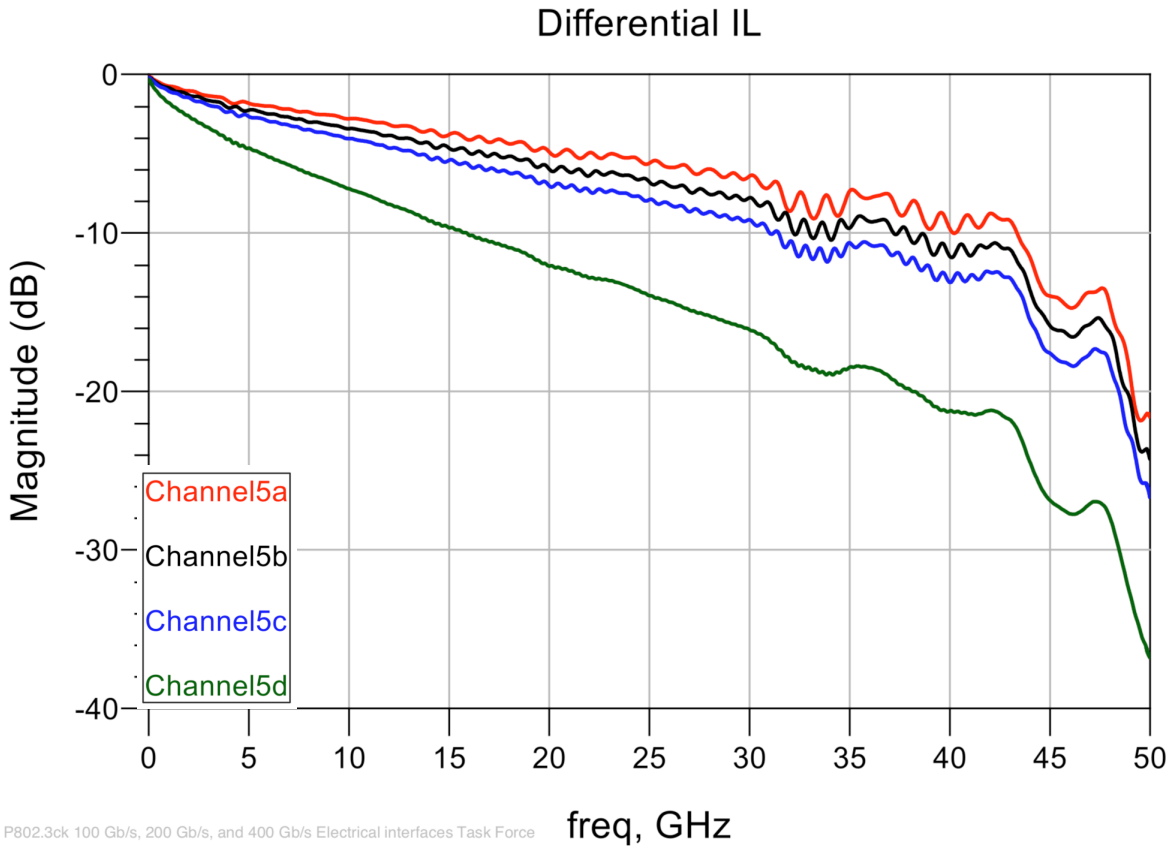
- **Updated analysis is with COM 3.1.0**
  - The updated TP1a analysis uses lim_3ck_adhoc_02_073119 channels
  - The updated TP4 analysis uses lim_3ck_02_0719 channels
- **COM analysis investigates impact of 50 mUI rectangular window**
  - The intent of this analysis is not to change TP1a/TP4 baseline line specifications
  - The updated results intended to only adjust the TP1a/TP4 limits due to 50 mUI rectangular window
  - The intention of new limits for VEO/VEC is to avoid relaxing or tightening the specification just adjust for rectangular window impact on VEO/VEC
- **D1.4 defines AUI-S/AUI-L, propose to align AUI-S/AUI-L with TP4 nearend and TP4 farend.**

C2M TP1a Channels for Updated Analysis

- **Channel based on lim_3ck_adhoc_02_073119 as shown**
  - 16 pairs (8 Tx, 8 Rx) QSFP-DD SMT Connector with host PCB footprint
  - PCB stackup is 30 layers, 150 mils thick, based on Meg7 material
  - PCB via stub length is modeled as 10 mils
  - Diff pair trace width/spacing is 4.5 mils /8.5 mils
  - ASIC and retimer footprint are simulated with actual BGA ball-out using the same PCB stackup.

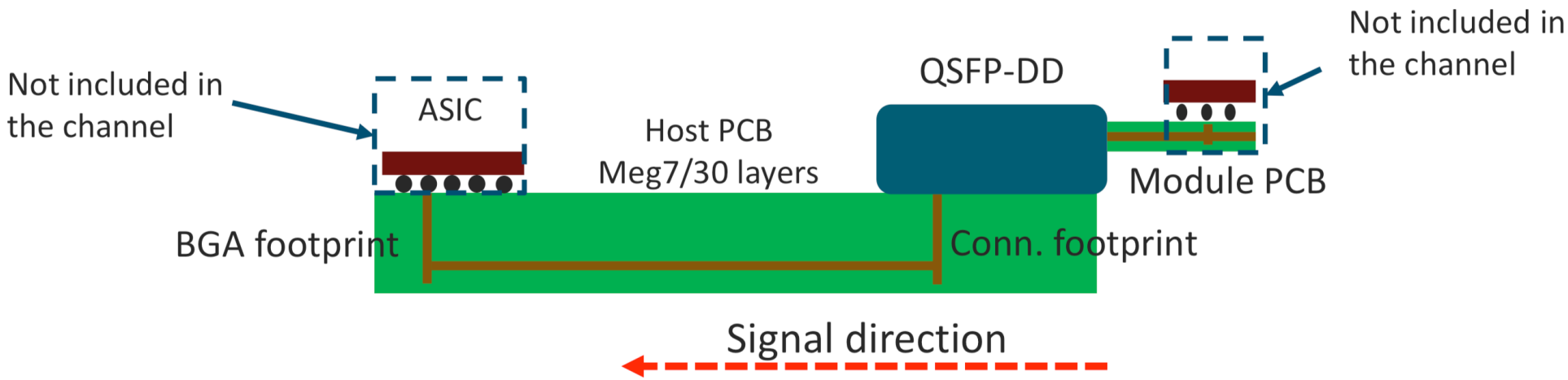


- **This analysis uses min loss channel 5a and max loss channel 5d.**



C2M TP4 Channels for Updated Analysis

- **Channel based on lim_3ck_02_0719 shown**
  - 16 pairs (8 Tx, 8 Rx) QSFP-DD SMT Connector and host PCB footprint are solved as one piece in HFSS
  - PCB stackup is 30 layers, 150mil thick, with Meg7 material
  - PCB via stub length is modelled as 10mil
  - Diff pair trace width/spacing is 4.5mil/8.5mil, 2 different trace lengths are used (2" & 9")
  - ASIC footprint are simulated with actual BGA ball-out using the same PCB stackup
  - Module CDR footprint is not included in the. Channel.



COM Code 3.1.0 Host-Module TP1a

❑ Test case I/II (13, 31 mm) ASIC packages.

Table 93A-1 parameters				
Parameter	**Setting**	**Units**	**Information**	
f_b	53.125	GBd		
f_min	0.05	GHz		
Delta_f	0.01	GHz		
C_d	[1.2e-4 0]	nF	[TX RX]	
L_s	[0.12 0]	nH	[TX RX]	
C_b	[0.3e-4 0]	nF	[TX RX]	
z_p select	[1 2]		[test cases to run]	
z_p (TX)	[13 31; 1.8 1.8]	mm	[test cases]	
z_p (NEXT)	[0 0 ; 0 0]	mm	[test cases]	
z_p (FEXT)	[13 31; 1.8 1.8]	mm	[test cases]	
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]	
C_p	[0.87e-4 0]	nF	[TX RX]	
R_0	50	Ohm		
R_d	[50 50]	Ohm	[TX RX]	
A_v	0.415	V	vp/vf=.694	
A_fe	0.415	V	vp/vf=.694	
A_ne	0.608	V		
L	4			
M	32	Samp/UI		
samples_for_C2M	100	Samp/UI		
T_O	50	mUI		
AC_CM_RMS	[0.0235 0.0256]	V	[test cases]	[0.0235 0.0256]
filter and Eq				[0.015, 0.015]
f_r	0.75	*fb		[0, 0]
c(0)	0.54		min	
c(-1)	[-0.2:0.02:0]		[min:step:max]	
c(-2)	[0:0.02:0.1]		[min:step:max]	
c(-3)	[0]		[min:step:max]	
c(1)	[-0.1:0.02:0]		[min:step:max]	
N_b	4	UI		
b_max(1)	0.4		As/dffe1	
b_max(2..N_b)	[0.15 0.15 0.1]		As/dfe2..N_b	
b_min(1)	0.1		As/dffe1	
b_min(2..N_b)	[-0.15 -0.15 -0.05]		As/dfe2..N_b	
g_DC	[-13:1:-3]	dB	[min:step:max]	
f_z	12.58	GHz		
f_p1	20	GHz		
f_p2	28	GHz		
g_DC_HP	[-3:0.5:1]		[min:step:max]	
f_HP_PZ	1.328125	GHz		
G_Qual	[-2 -9 ;-2 -12; -4 -12;-6 -13]	dB	ranges	
G2_Qual	[0 -1 -2 -3]	dB	ranges	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_C2M_host_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_eval_	
COM_CONTRIBUTION	0	logical
Local Search	2	
Operational		
VEC Pass threshold	9	db
EH_min	15	mV
ERL Pass threshold	7.3	dB
DER_0	0.00001	
T_r	0.0075	ns
FORCE_TR	1	5
PMD_type	C2M	
BREAD_CRUMBS	0	logical
SAVE_CONFIG2MAT	1	logical
PLOT_CM	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	800	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0.2e-9]	[port1 port2]
TDR_W_TXPKG	1	
N_bx	0	UI
Tukey_Window	1	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	4.10E-08	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
ICN & FOM_ILD parameters		
f_v	0.594	*Fb
f_f	0.594	GHz f_r specified in first column
f_n	0.594	GHz
f_2	40	GHz
A_ft	0.600	V
A_nt	0.600	V

new
upodated for D1.4

Floating Tap Control		
N_bg	0	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	40	I span for floating taps
bmaxg	0.2	DFE value for floating taps

for TP4-->	[1.2e-4 0]	nF	[TX RX]
	[0.12 0]	nH	[TX RX]
	[0.3e-4 0]	nF	[TX RX]
	[1 2 3]		[test cases to run]
	[2 7 8]	mm	[test cases]
	[0 0 0]	mm	[test cases]
	[2 7 8]	mm	[test cases]
	[0 0 0]	mm	[test cases]
	[0 0.87e-4]	nF	[TX RX]

Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	0.00579	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	407	mm
z_bp (NEXT)	407	mm
z_bp (FEXT)	407	mm
z_bp (RX)	407	mm
C_0	0	nF
C_1	0	nF
Include PCB	0	logical

COM Code 3.1.0 Module to Host TP4

- **Test case I/II (4, 7 mm) CDR packages.**

Table 93A-1 parameters					I/O control			Table 93A–3 parameters			Floating Tap Control			
Parameter	**Setting**	**Units**	**Information**		DIAGNOSTICS	1	logical	**Parameter**	**Setting**	**Units**	N_bg	0	0 1 2 or 3 groups	
f_b	53.125	GBd			DISPLAY_WINDOW	1	logical	package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]		N_bf	3	taps per group	
f_min	0.05	GHz			CSV_REPORT	1	logical	package_tl_tau	6.141E-03	ns/mm	N_f	40	l span for floating taps	
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_C2M_host_{date}\		package_Z_c	[87.5 87.5; 92.5 92.5]	Ohm	bmaxg	0.2	DFE value for floating taps	
C_d	[1.0e-4 0]	nF	[TX RX]		SAVE_FIGURES	0	logical	**ICN & FOM_ILD parameters**						
L_s	[0.12 0]	nH	[TX RX]		Port Order	[2 4 1 3]		f_v	0.594	*Fb	for TP4-->	[1.2e-4 0]	nF	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	C2M_eval_		f_f	0.594	GHz f_r specified in first column		[0.12 0]	nH	[TX RX]
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical	f_n	0.594	GHz		[0.3e-4 0]	nF	[TX RX]
z_p (TX)	[4 7; 0 0]	mm	[test cases]		Local Search	2		f_2	40	GHz		[1 2 3]		[test cases to run]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]		**Operational**			A_ft	0.600	V		[2 7 8]	mm	[test cases]
z_p (FEXT)	[4 7; 0 0]	mm	[test cases]		VEC Pass threshold	9	db	A_nt	0.600	V		[0 0 0]	mm	[test cases]
z_p (RX)	[0 0; 0 0]	mm	[test cases]		EH_min	15	mV	**Table 92–12 parameters**				[2 7 8]	mm	[test cases]
C_p	[0.65e-4 0]	nF	[TX RX]		ERL Pass threshold	7.3	dB	**Parameter**	**Setting**			[0 0 0]	mm	[test cases]
R_0	50	Ohm			DER_0	0.00001		board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*			[0 0.87e-4]	nF	[TX RX]
R_d	[50 50]	Ohm	[TX RX]		T_r	0.0075	ns	board_tl_tau	*5.790E-03*	ns/mm				
A_v	0.415	V	vp/vf=.694		FORCE_TR	1	5	board_Z_c	100	Ohm				
A_fe	0.415	V	vp/vf=.694		PMD_type	C2M		z_bp (TX)	*200*	mm				
A_ne	0.608	V			BREAD_CRUMBS	0	logical	z_bp (NEXT)	*200*	mm				
L	4				SAVE_CONFIG2MAT	1	logical	z_bp (FEXT)	*200*	mm				
M	32	Samp/UI			PLOT_CM	1	logical	z_bp (RX)	*0*	mm				
samples_for_C2M	100	Samp/UI			**TDR and ERL options**			**Include PCB**	**0**	**logical**				
T_O	50	mUI			TDR	1	logical							
AC_CM_RMS	[0, 0]	V	[test cases]	[0.0235 0.0256]	ERL	1	logical							
filter and Eq				[0.015, 0.015]	ERL_ONLY	0	logical							
f_r	0.75	*fb		[0, 0]	TR_TDR	0.01	ns							
c(0)	0.72		min		N	800		new						
c(-1)	-0.18		[min:step:max]		beta_x	0		upodated for D1.4						
c(-2)	0.04		[min:step:max]		rho_x	0.618								
c(-3)	[0]		[min:step:max]		fixture delay time	[0 0.2e-9]	[port1 port2]							
c(1)	0		[min:step:max]		TDR_W_TXPKG	1								
N_b	4	UI			N_bx	0	UI							
b_max(1)	**0.4**		**As/dffe1**		Tukey_Window	1								
b_max(2..N_b)	**[0.15 0.15 0.1]**		**As/dfe2..N_b**		**Receiver testing**									
b_min(1)	**0.1**		**As/dffe1**		RX_CALIBRATION	0	logical							
b_min(2..N_b)	**[-0.15 -0.15 -0.05]**		**As/dfe2..N_b**		Sigma BBN step	5.00E-03	V							
g_DC	[-13:1:-1]	dB	[min:step:max]		**Noise, jitter**									
f_z	12.58	GHz			sigma_RJ	0.01	UI							
f_p1	20	GHz			A_DD	0.02	UI							
f_p2	28	GHz			eta_0	4.10E-08	V^2/GHz							
g_DC_HP	[-3:0.5:1]		[min:step:max]		SNR_TX	32.5	dB							
f_HP_PZ	1.328125	GHz			R_LM	0.95								
G_Qual	[0 -4 -12; -4 -12; -5 -13]	dB	ranges											
G2_Qual	[0 -1 -2 -3]	dB	ranges											

COM Analysis on Lim Channel 1 and 4 – ASIC to Module

- **Results with COM 2.76 from March 2020 presentation was one of supporting presentation in choosing VEO=15 mV and VEC=9 dB**
  - As can be be seen the VEC/VEC value substantially exceed case II (31 mm PKG) but fail pathological case I (13 mm PKG)!

Channel	Equalizer	Fitted IL@26.56 GHz	IL wPKG@26.55 GHz	VEO Case I/II	VEC Case I/II	EW Case I/II	COM Case I/II
Lim Channel 2" at TP1a FOM ILD = 0.16 ICN = 3.7 mV ERL11=12.3 dB ERL22=9.3 dB	5T FFE	5.9 dB	12.5 dB	21.4/31.3	11.5/6.0	0.156/0.219	2.7/6.0
	4T DFE	5.9 dB	12.5 dB	27.4/38.8	11.4/6.5	0.063/0.187	2.7/5.5
	2T+2T 12UI DFE	5.9 dB	12.5 dB	43.7/39.9	7.5/6.5	0.125/0./187	4.8/5.6
	12T FFE	5.9 dB	12.5 dB	48.4/32.3	5.4/5.8	0.219/0.219	6.6/6.3
Lim Channel 2" At Slicer FOM ILD = 0.16 ICN = 3.7 mV ERL11=12.3 dB ERL22=9.3 dB	5T FFE	5.9 dB	14.5 dB	11.0/28.8	15.7/8.1	0.125/0.188	1.6/4.3
	4T DFE	5.9 dB	14.5 dB	18.7/27.5	14.2/8.9	0.062/0.156	1.9/3.9
	2T+2T 12UI DFE	5.9 dB	14.5 dB	30.3/29.3	10.0/8.4	0.094/0.156	3.3/4.2
	12T FFE	5.9 dB	14.5 dB	28.4/23.7	7.7/7.8	0.188/0.188	4.6/4.5
Lim Channel 9" at TP1a FOM ILD = 0.13 ICN = 1.44 mV ERL11=16 dB ERL22=11.3 dB	5T FFE	14.8	21.4	11.3/13.9	10.8/6.5	0.125/0.187	3.0/5.5
	4T DFE	14.8	21.4	18.2/18.9	8.2/6.4	0.125/0.187	4.3/5.7
	2T+2T 12UI DFE	14.8	21.4	23.7/18.9	6.1/6.4	0.156/0.187	6.0/5.7
	12T FFE	14.8	21.4	19.1/13.2	5.3/6.2	0.219/0.187	6.8/5.8
Lim Channel 9" At Slicer FOM ILD = 0.13 ICN = 1.44 mV ERL11=16.0 dB ERL22=11.3 dB	5T FFE	14.8	23.2	7.2/10.9	12.3/7.3	0.094/0.188	2.4/4.9
	4T DFE	14.8	23.2	16.9/15.6	8.6/7.2	0.125/0.156	4.0/5.0
	2T+2T 12UI DFE	14.8	23.2	21.5/17.0	6.9/6.9	0.125/0.156	5.3/5.2
	12T FFE	14.8	23.2	14.9/12.7	6.3/6.8	0.188/0.188	5.8/5.3

COM Analysis on Lim Channel 1 and 4 – ASIC to Module

- **Lim channels include BGA footprint, via, host stripline, via, QSFP-dd connector and module module PCB**
  - Results for test case I=13 mm is pathological and consistent with prior results
  - VEO results with 50 mUI window are reduced by ~half and VEC increases by 6+ dB
- **Follow prior approach to determine new limits for VEO/VEC where case II passes with high margin but case I fails**
  - Recommended TP1a VEO=9.5 mV and VEC=14 dB
  - 15 mV RMS common mode at TP0 has negligible effect at TP1a.

Channel	VCM	Fitted IL@26.56 GHz	IL wPKG@26.55 GHz	VEO Case I/II	VEC Case I/II	EW Case I/II	COM Case I/II**
Lim Channel 2" at TP1a ILD = 0.16, ICN = 4.9 mV ERL[11,22]= [9.1, 9.1] dB	[0, 0]	5.9 dB	11.3 dB	10.6/25.7	19.4/9.9	0.125/0.20	1.0/3.34
	[0.024, 0.026]* V	5.9 dB	11.3 dB	10.7/25.6	19.4/9.9	0.12/0.2	1.0/3.3
Lim Channel 2" at Slicer ILD = 0.16, ICN = 4.9 mV ERL[11,22]= [9.1, 9.1] dB	[0, 0]	5.9 dB	14.5 dB	6.3/16.9	23.2/12.8	0.11/0.17	0.6/2.3
	[0.024, 0.026]* V	5.9 dB	14.5 dB	6.3/16.9	23.2/12.8	0.11/0.17	0.623/2.26
Lim Channel 9" at TP1a ILD = 0.09, ICN = 2.0 mV ERL[11,22]=[11.4,11.4] dB	[0, 0]	14.7 dB	20.3 dB	8.5/10.6	13.9/10.8	0.16/0.19	1.9/3.0
	[0.024, 0.026]* V	14.7 dB	20.3 dB	8.5/10.5	14/10.8	0.16/0.19	1.9/3.0
Lim Channel 9" at Slicer ILD = 0.09, ICN = 2.0 mV ERL[11,22]=[11.4,11.4] dB	[0, 0]	14.7 dB	22.1 dB	5.9/7.7	16.4/12.8	0.14/0.17	1.4/2.3
	[0.024, 0.026]* V	14.7 dB	22.1 dB	5.9/7.6	16.4/12.8	0.14/0.17	1.4/2.3

*** Equivalent of 15 mV RMS at TP0 for test case I and II**

**** COM values are for reference as it include reduction due to 50 mUI window, per classic COM definition COM is reported with no window and for those result please see page 7.**

TP4 Short and Long

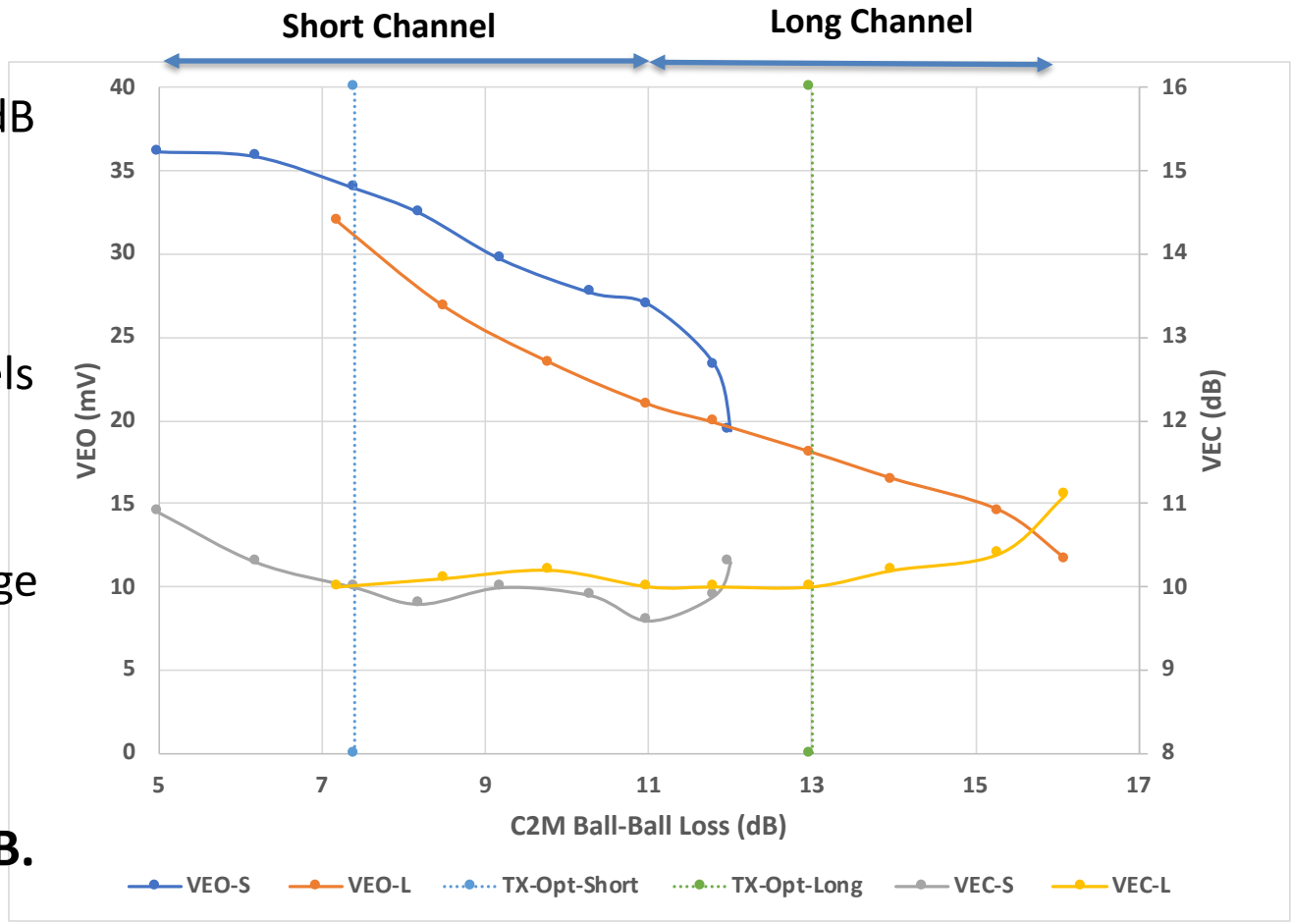
- **D1.4 draft defines TP4 short and long**
  - The next step is to define the ranges for short and long C2M channels
  - Otherwise short/long setting will not be very useful!

Table 120G–4—Module state mapping

IEEE Interface Type	tx_eq_state	Application Name
100GAUI-1 C2M	0	100GAUI-1-S C2M
100GAUI-1 C2M	1	100GAUI-1-L C2M
200GAUI-2 C2M	0	200GAUI-2-S C2M
200GAUI-2 C2M	1	200GAUI-2-L C2M
400GAUI-4 C2M	0	400GAUI-4-S C2M
400GAUI-4 C2M	1	400GAUI-4-L C2M

M2C Short and Long Channels

- **Measurement configurations**
  - The MCB/HCB loss is 5 dB
  - Based on the data short channel can be up to 10 dB and long channel from 10 dB to 16 dB
    - But to align with CR host it would be better to increase short channel loss to 11 dB
  - Optimum TX FIR setting for short and long channels
    - TX FIR short [0.02, -0.16, 0.82, 0]
    - TX FIR long [0.04, -0.18, 0.78, 0]
  - VEO/VEC results reported are for the worst package combinations
- **Result indicate ~10 dB as optimum transition from short to long but considering alignment with CR host the recommended loss is 10.975 dB.**



COM Analysis on Lim Module to Chip Channels

- **Lim 1a/2a are TP4 near end like channels and Lim 1b/2b are TP4 far end like channels**
  - Results are with optimum setting as determined for mated board for short and long channels
    - TX FIR optimum setting for short channel is based on 7.4 dB loss and for long channel is based on 13 dB loss
  - Recommended TP4-S VEO=20 mV and VEC=14.5 dB (also include impact of sub-optimum TX FFE)
  - Recommended TP4-L VEO=11 mV and VEC=12.5 dB (also include impact of sub-optimum TX FFE).

Channel	ILD, ICN, ERL	Fitted IL at 26.56 GHz (dB)	Total IL w PKG at 26.55 GHz (dB)	VEO mV Case I/II	EW UI Case I/II	VEC dB Case I/II	COM dB Case I/ II
Lim Channel 1a * TP4 near end	ILD = 0.1, ICN = 2.8 mV ERL11=10.9 dB, ERL22=10.7 dB	5.4	6.0	30/27	0.25/0.23	12.3/13	2.4/2.3
Lim Channel 2a * TP4 near end	ILD = 0.11, ICN = 4.9 mV ERL11=11.3 dB, ERL22=11.1 dB	5.9	6.7	24/21.6	0.19/0.20	13.7/14.6	2.0/1.8
Lim Channel 1a ** +200 mm TP4 far end	ILD = 0.1, ICN = 2.8 mV ERL11=10.9 dB, ERL22=10.7 dB	15.5	16.1	18.2/15.3	0.23/0.21	8.2/9.5	4.3/3.5
Lim Channel 2a ** +200 mm TP4 far end	ILD = 0.11, ICN = 4.9 mV ERL11=11.3 dB, ERL22=11.1 dB	16.1	16.8	16.2/13.8	0.22/0.22	8.9/10.1	3.9/3.2
Lim Channel 1b ** TP4 far end	ILD = 0.1, ICN = 2.1 mV ERL11=10.6 dB, ERL22=11.7 dB	14.8	15.8	16.0/11.1	0.21/0.18	9.5/12.8	3.5/2.3
Lim Channel 2b ** TP4 Far end	ILD = 0.12, ICN = 0.70 mV ERL11=11.7 dB, ERL22=10.3 dB	15.0	16.0	17.8/11.6	0.22/0.18	8.9/12.3	3.9/2.4

*** TX FIR for short channel [0.02 -0.16 0.82 0]**

**** TX FIR for long channel [0.04 -0.18 0.78 0]**

Summary

- **Summary of results at TP1a with COM 3.1.0 with 50 mUI rectangular window based on analysis on reference Lim ASIC to module channels**
  - Recommend to adjust TP1a VEO=9.5 mV and VEC=14 dB
  - 15 mV RMS common mode at TP0 has negligible impact at TP1a
- **At TP4 Need to align AUI-S (short) and AUI-L (long) with TP4 near end and TP4 far end**
  - Propose to define AUI-S loss range to align with CR host with loss up to 10.975 dB
  - Propose to define AUI-L loss range to be >10.975 dB and <16 dB
  - Propose align and replacing TP4 nearend and farend with TP4-S and TP4-L to align with AUI-S and AUI-L
- **Summary of results at TP4 with COM 3.1.0 with 50 mUI rectangular window based on analysis on reference Lim module to host channels**
  - Recommended TP4-S VEO=20 mV and VEC=14.5 dB (also include impact of sub-optimum TX FFE)
  - Recommended TP4-L VEO=11 mV and VEC=12.5 dB (also include impact of sub-optimum TX FFE)
  - Proposed above limits also include sub-optimum TX FIR over the range of short or long channels.