Editorial Consensus Discussion

Matt Brown
Huawei Technologies Canada
P802.3ck Chief Editor

Topic #1: Annex 120G C2M ESMW and EW parameters

- The specified values for eye width (EW) and eye symmetry mask width (ESMW) are currently TBD.
- Comment 173 (see next slide) proposes to remove ESMW parameter specifications in Annex 120G.
- Comment 231 (see next slide) proposes to remove EW parameter specifications and replace with jitter specifications in Annex 120G.
- A number of comments propose values for the TBD for EW and ESMW.
  - However, according to comments 173 and 231, EW and ESMW are not meaningful without fully specifying the DFE feedback in the reference receiver.
  - Many comments proposing values for these parameters have been withdrawn.
- It seems there has been a paradigm shift from previous generations given introduction of the DFE into the reference receiver.

Comments part 1

Cl 120G *SC* 120G.3.1 *P* 221 *L* 17 # 173

Ran, Adee Intel

Comment Type T *Comment Status* X

Addressing EMSW which is TBD.

EMSW is not a meaningful measure for a receiver with DFE, since the eye's shape depends on the delay and the transfer function of DFE's feedback path. A DFE mathematical model can have arbitrary delay and transfer function so the value of EMSW (or any eye width parameter) is not well defined.

Furthermore, the DFE typically optimizes the eye height, but not necessarily the eye width (whihc requires equalizing the transitions). Trying to optimize for both EW and EH with a single DFE has been done in early versions of PCI express, it can be a futile exercise, and it is not what a real receiver will do anyway.

As the experience with COM has shown, for lossy channels and DFE receivers the equalized EH is a good enough figure of merit. Real receivers do not care about asymmetry caused by the DFE.

It is suggested to remove EMSW, at least until evidence of the need for it and a robust measurement method is presented.

SuggestedRemedy

Remove the EMSW specification in this subclause, and also in 120G.3.2 and Table 120G–5 and Table 120G–8.

Proposed Response *Response Status* O

Jitter specifications in 120F.3.1 (Table 120F-1)

Output jitter			
J_{RMS} (max)	120D.3.1.8	0.023	UI
J4u (max)	120D.3.1.8	0.118	UI
Even-odd jitter (max)	120D.3.1.8	0.019	UI

Cl 120G *SC* 120G.5.2 *P* 236 *L* 9 # 231

Ran, Adee Intel

Comment Type T *Comment Status* X

This subclause specifies measurement of "eye opening parameters eye height, eye width, and vertical eye closure".

Item e here:
"e) Compute the receiver input signal yrx(k) by applying the effect of the DFE to y2(k) using the
sampling phase ts"

May cause ambiguity in the resulting eye diagram, which can yield different EW and ESMW results.

The reason is that it does not fully specify how the sampling phase ts is used. To create a "nice" eye diagram, the DFE feedback is typicallly applied after some delay relative to ts. The time when the DFE feedback is applied will affect the eye shape, width and ESMW (though not the eye height at ts, which is maximized by the DFE coefficients).

Note that this delay is not necessarily what a real receiver will have, and the eye may not correspond to the performance of real receivers.

In another comment I suggest to remove the ESMW specification. Following the statements above, The EW specification may also be worth removing. EH (which does not depend on the DFE feedback timing) should be enough.

Without EW, jitter measurement and calibration should be done using other means. Jitter injected in host stressed input test is already calibrated using C2C methods. Jitter for host and module outputs can be specified using C2C methods too.

SuggestedRemedy

Remove all EW specifications and change the text in this subclause to omit EW.

(Alternatively. if ESMW and/or EW are retained, then the application of the DFE feedback should be specified explicitly. I would suggest specifying that the DFE feedback effect starts 1/2 UI after ts.)

Add jitter specifications J4U, JRMS, and EOJ, for host output and module output, using references to 120F.3.1 (same values as in Table 120F–1).

Proposed Response *Response Status* O

Comments part 2

Cl 120G *SC* 120G.3.1 *P* 221 *L* 17 # 32

Wu, Mau-Lin Mediatek

Comment Type T *Comment Status* X

The ESMW (eye symmetry mask width) value in Table 120G-1 is still TBD

SuggestedRemedy

Change 'TBD' value to '0.1'

Proposed Response *Response Status* O

Cl 120G *SC* 120G.5.2 *P* 236 *L* 20 # 246

Dawe, Piers Nvidia

Comment Type T *Comment Status* X

This criterion "The values of eye height, eye width, and vertical eye closure are the values obtained with the combination of gDC and gDC2 that produces the minimum value of vertical eye closure where eye height also meets the target value" would fail a signal that passes all 3 criteria on a different Rx setting but fails ESMW at the setting for best VEC.
We learnt in previous C2M projects that best vertical and best horizontal opening weren't at the same setting.
Editorial: the idea is not to meet a target, it is to meet or exceed a limit.

SuggestedRemedy

Change to:
The values of eye height, eye width, and vertical eye closure are the values obtained with the combination of gDC and gDC2 that produces the minimum value of vertical eye closure where eye height and ESMW also comply with the limits in the appropriate table.
Editorial: ESMW isn't really a measurement, it's a mask. Maybe define ESW as the measurement?

Proposed Response *Response Status* O

Withdrawn comments not shown

Specifications

- TP1a host output
  - ESMW value (Table 120G-1)
- TP4 module output
  - near-end ESMW value (Table 120G-3)
  - far-end ESMW value (Table 120G-3)
- TP4a host input stressed eye
  - far-end ESMW value (Table 120G-5)
  - far-end EW value (Table 120G-5)
- TP4 module input stressed eye
  - ESWM value (Table 120G-8)
  - EW value (Table 120G-8)
  - Module stressed eye setup specifies optimizing on best EH and EW (120G.3.4.1.1)
- Test methodology in 120G.5.2 includes determination of eye width

Options

- Option #1
  - Leave as is and specify values for EW and ESMW.
- Option #2
  - Retain EW and ESMW
  - Specify the RR DFE appropriately (no proposals so far)
  - Specify values for EW and ESMW.
- Option #3
  - remove the EW and ESMW
  - specify jitter at host output and module output

Proposed Straw Poll for ad hoc

For Annex 120G, I would support the following direction to deal with EW and ESMW:

A: retain EW and ESMW as currently defined

B: retain EW and ESMW and respecify RR DFE

C: remove EW and ESMW, add jitter specification at TP1a and TP4

D: other approach not listed above

Chicago rules

Thanks