Following Up on Representing Discontinuities for CR Host Board

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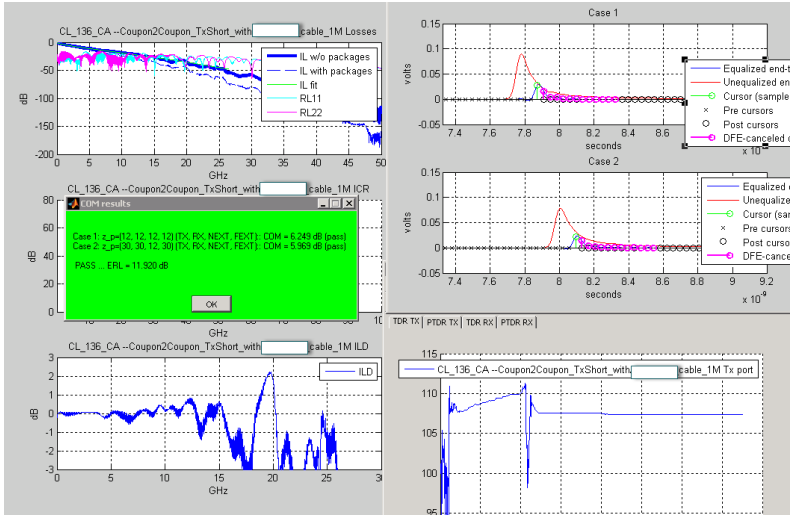
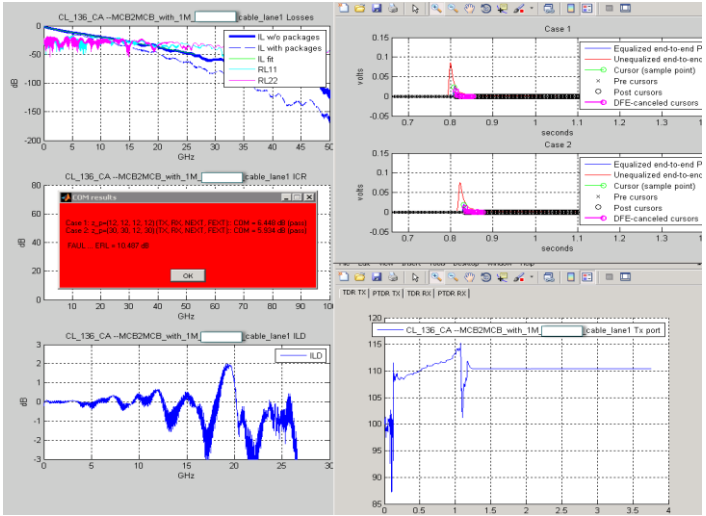
Challenge Definition – Presented During May Interim

- Basic Assumptions
  - Cable assembly MCB is optimized to best match the cable assembly and is as close as the connector can be to a seamless transition
  - µvias, or other high cost structures are acceptable
  - Impedance variance to be kept to a minimum for these test structures
  - Actual connector area to contain higher reflection via structures and higher production impedance variance.
  - Currently the “include PCB” section in COM does not account for the above discrepancies between MCB and actual PCB
- Challenge
  Update the “include PCB” section accordingly and include discontinuities, Xtalk and potentially other relevant phenomena

50Gbps “Include PCB” is Somewhat Smooth & Ideal…

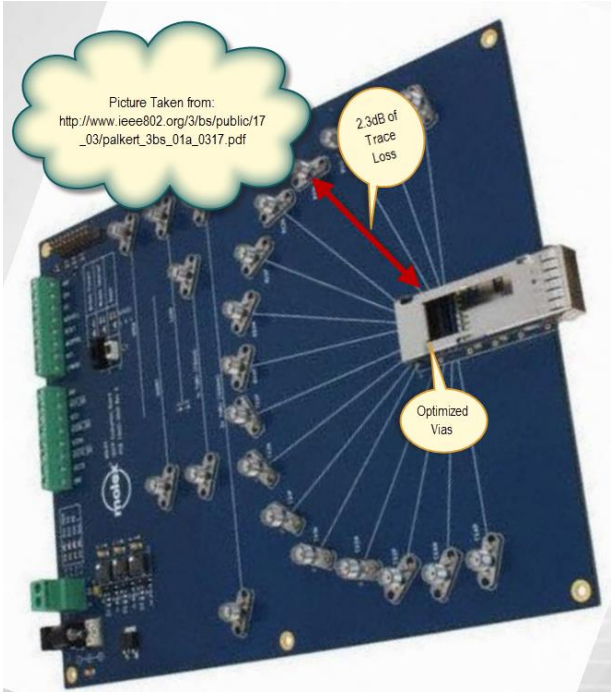
- Host “include PCB” is smooth and under accounts for reflections
- Two different MCBs + same 1 meter cable - with passing vs. failing ERLs result with the same COM ≈5.95





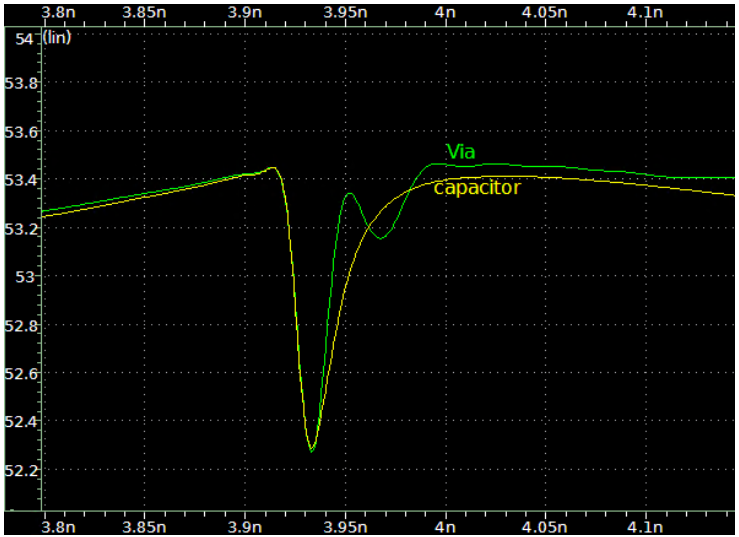
MCB Construction and Measurement Implications

- Cable assembly measurements include optimized structures and ~2.3dB of trace loss matched as best as possible to the cable
- In an actual host board the connector will be linked with through-hole via structures with minimal stubs
- Need as simple a representation as possible to the actual host board vias located at the connector area
- The representation needs to mimic the way actual host board vias would have looked from ~2.3dB away



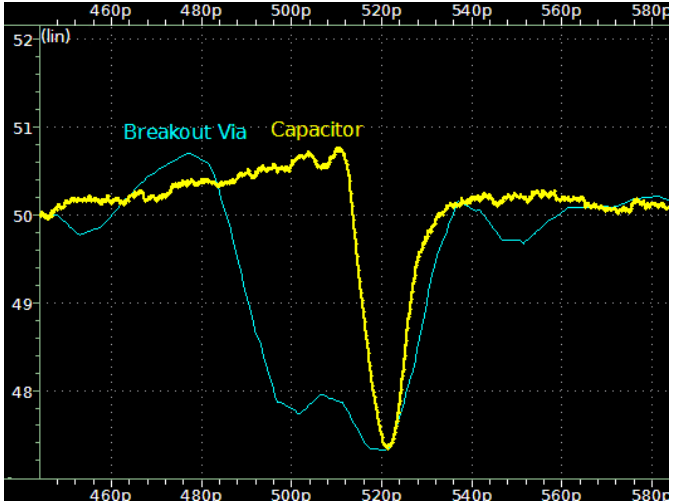
Correlating Extracted Optimized Via (May Interim)

- An optimized via structure placed at the connector of a host board was correlated to a capacitor discontinuity placed 2.3dB closer to the TDR
- The vias had 9 mil drill, 10 mil stub and optimized structure enabling them to be placed within the SMT connector area and a total length of ~2.7mm
- Excessive capacitance value was correlated to 19fF to be located @ the concatenation point to a measured MCB+cable assembly+MCB



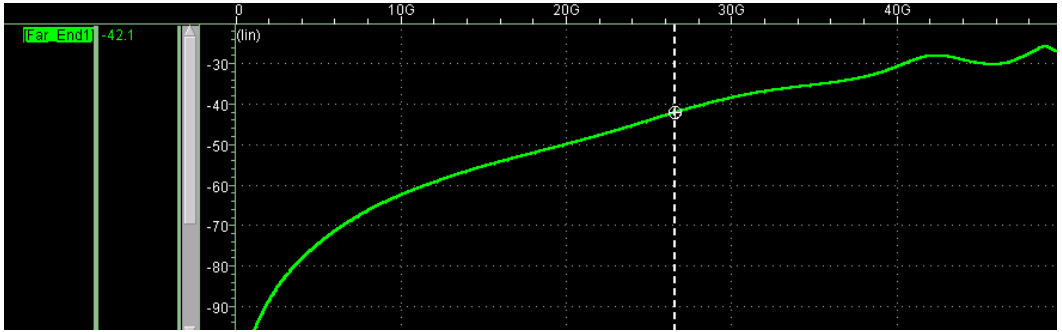
Chip Break-Out Area Phenomena

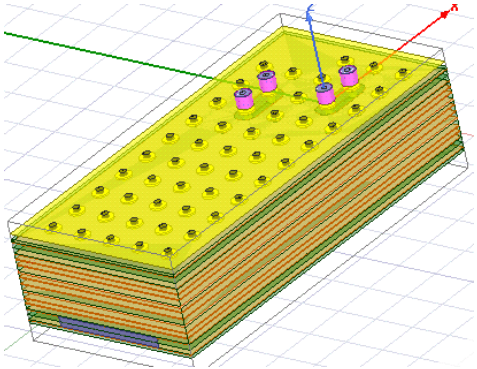
- The Chip Break-out area is characterized by via discontinuity & break-out traces cross-talk
- Further optimization of break-out Via and correlating the impedance fall to an excessive capacitance resulted in a value of 29fF



Chip Break-Out Area Phenomena – XTalk.

- @ 50Gbps BO Xtalk was low enough to ignore… @100G?!
- Analyzed via pattern surrounded by GND (as was defined by a group of 802.3ck participants during discussions prior to this work done) and break-out traces Xtalk from ONE aggressor ➔ -40dB ICR (Via + trace loss ~2dB)

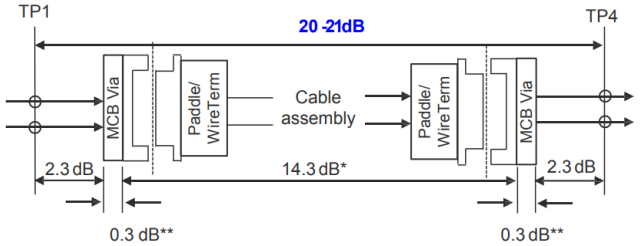


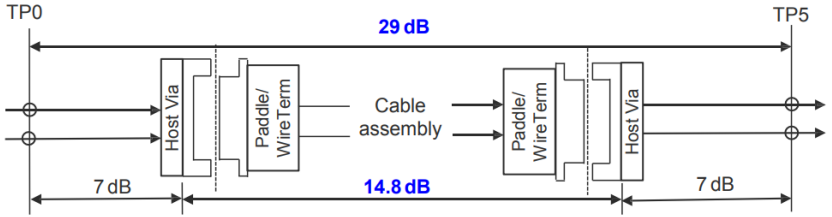


- Tx side: SNDR @ TP0 is -33dB – How would it look @ TP0a? Lower SNDR to account for Xtalk?!
- Rx side: should account for two aggressors Xtalk➔-34dB – Lower Tx SNDR for this?
  - if yes; one side accounted for; SNDR = -27.5dB !

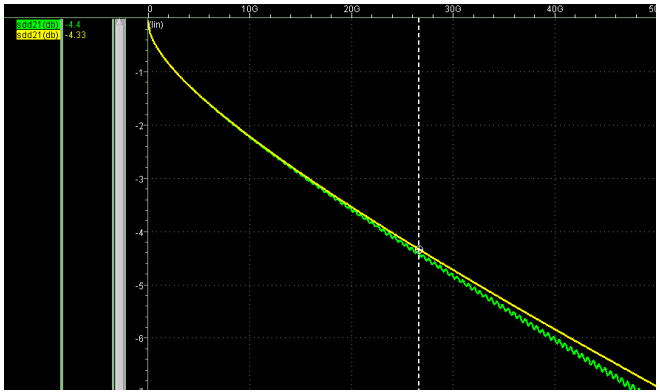
“Include PCB” Trace Loss

- As suggested in http://www.ieee802.org/3/ck/public/19_05/palkert_3ck_01b_0519.pdf
- TP0-TP1 Loss should follow ≈ 7dB-2.3dB-0.3dB = 4.4dB

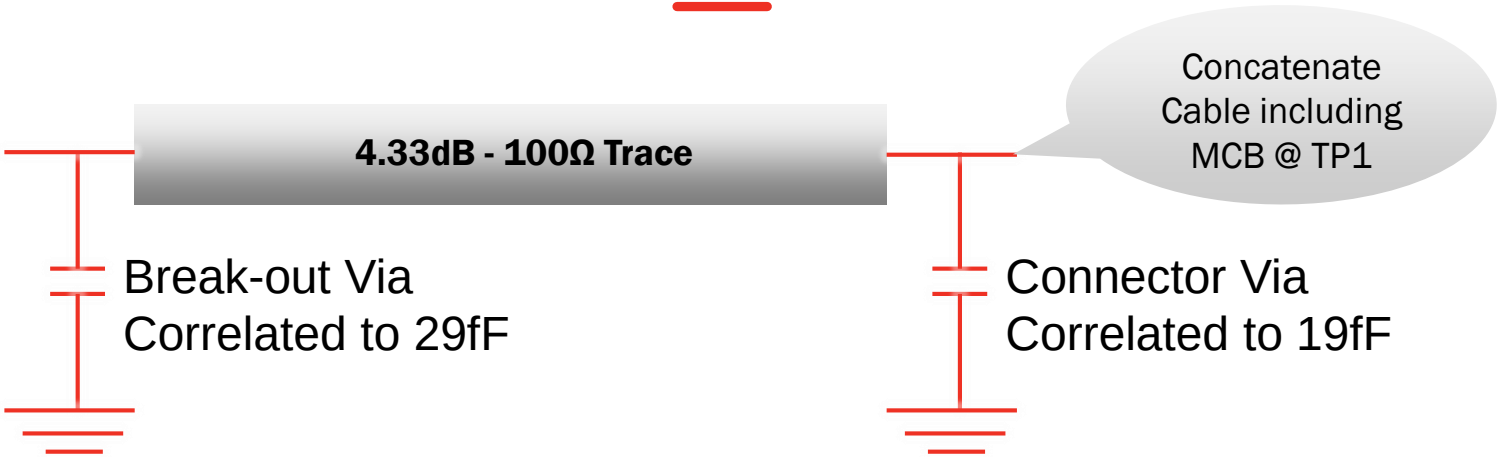




- Given Correlated capacitance, pure trace loss = 4.33dB ➔ 4.4dB by capacitance ripple



Current Model to be Inserted as “Include PCB”



“Include PBC” Status & Next Phases

- Vias were correlated to simple capacitance values 29fF & 19fF
- A simple trace representation suggested to be added to accommodate the end to end target loss including the MCB loss
  - Fit 4.33dB – 100Ω “Meg7 like” trace for parameters

  Two phase examination:
  - Integrate suggestion into a “test” COM version and examine impact
  - Decide how to account for Xtalk (SNDR?!) and examine impact

Thank You