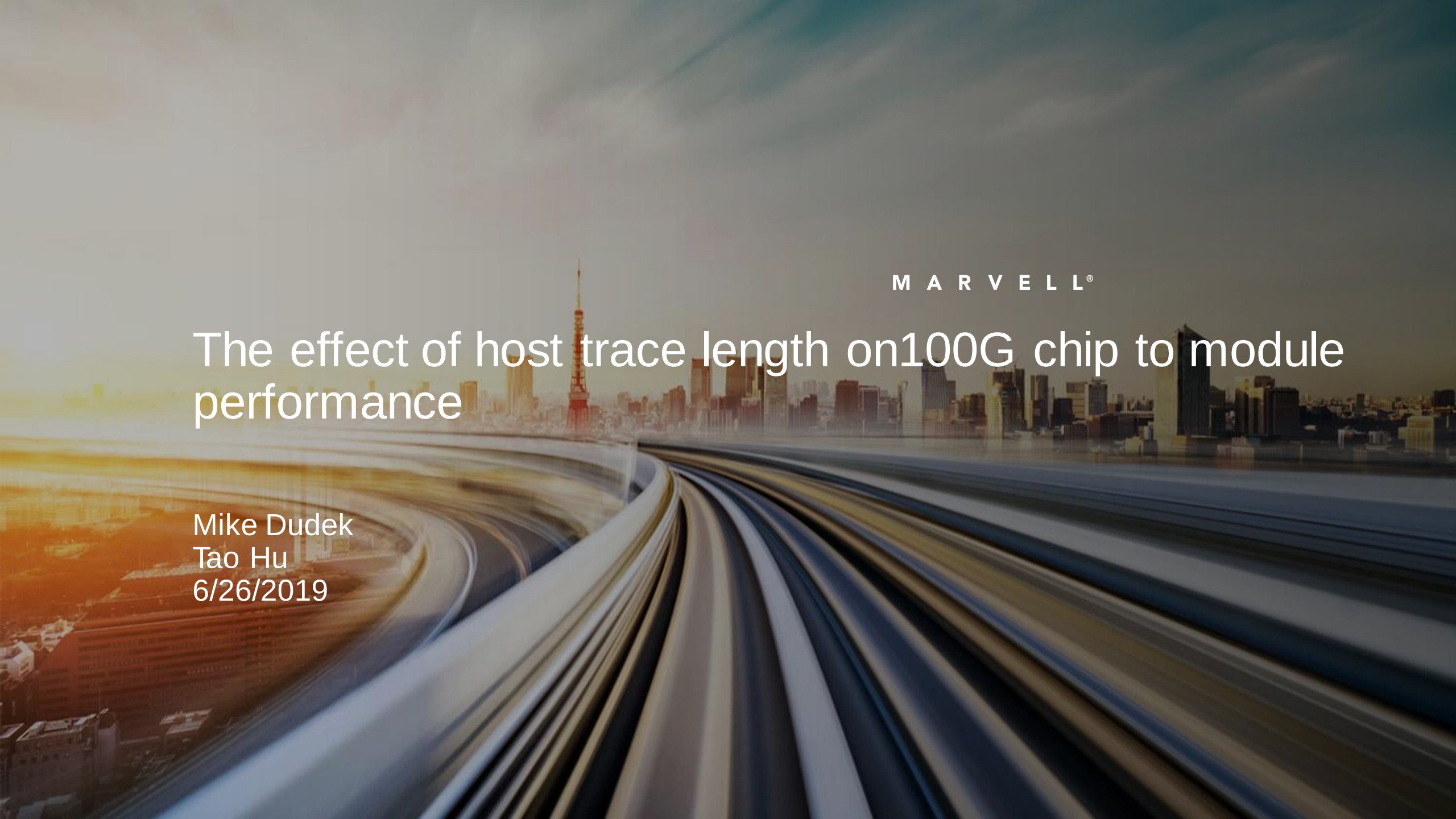

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The effect of host trace length on100G chip to module performance

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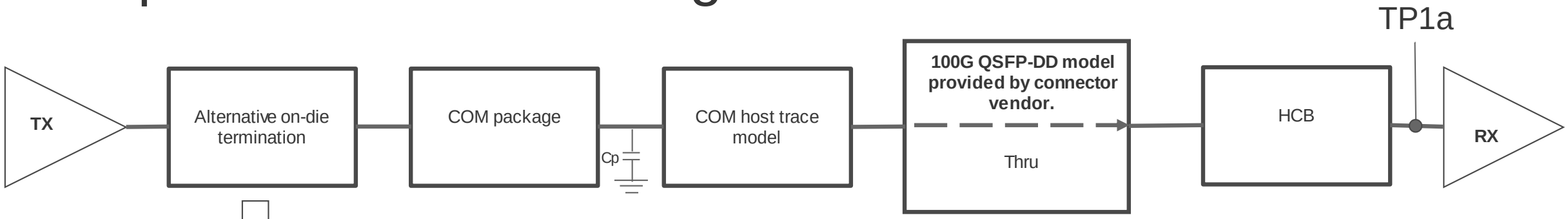
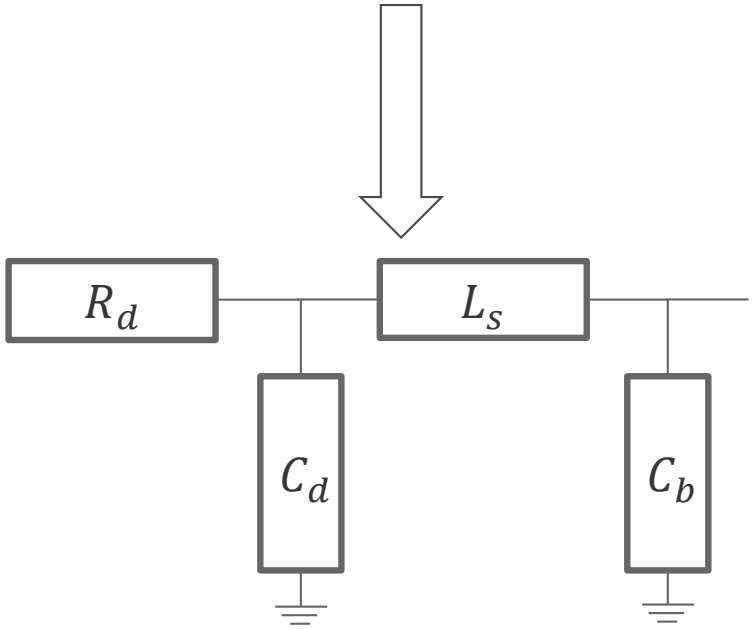
6/26/2019

Introduction

- This presentation explores the effect of host trace length on the performance of the chip to module link to the Tx test point TP1a
- The effects of different die models, package lengths, some host impairments and connector crosstalk is also included.
- No conclusions are made as to what should be included in the baseline proposal as further investigations are still needed.

Chip to module block diagram for COM





Alternative on-die termination

- HCB trace: 100ohm 63.8mm (2.5dB loss) (from COM model)
- TX/RX termination Rd: 50ohm
- Package trace length: 15mm/30mm
- Sweep host trace length
- Host trace impedance: 80/90/100/110ohm
- Av: 0.415V A_ne: 0.608V A_fe: 0.415V
- Crosstalk is not included unless specifically stated
- Lane 3 Is used for the simulations if not stated otherwise.
- 4 tap DFE is used unless stated otherwise
- Performance is simulated using COM 2.70
- The complete COM table is in the back-up

filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.1]		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	4	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-14:1:-3]	dB	[min:step:max]
f_z	12.58	GHz	
f_p1	20	GHz	
f_p2	28	GHz	
g_DC_HP	[-3:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	0	UI	
Include PCB	1	logical	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	0		

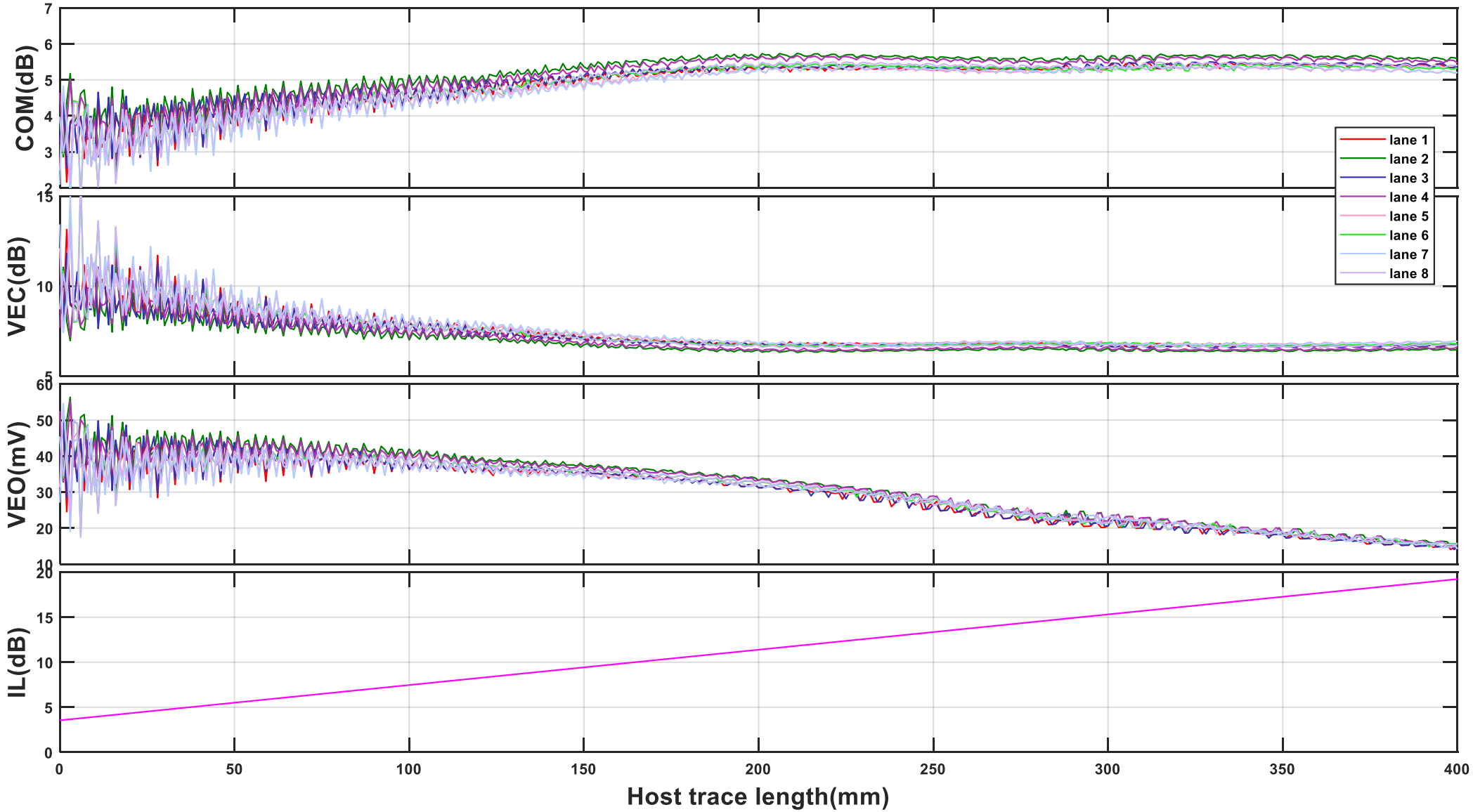
4-tap DFE RX

COM PCB and package loss information

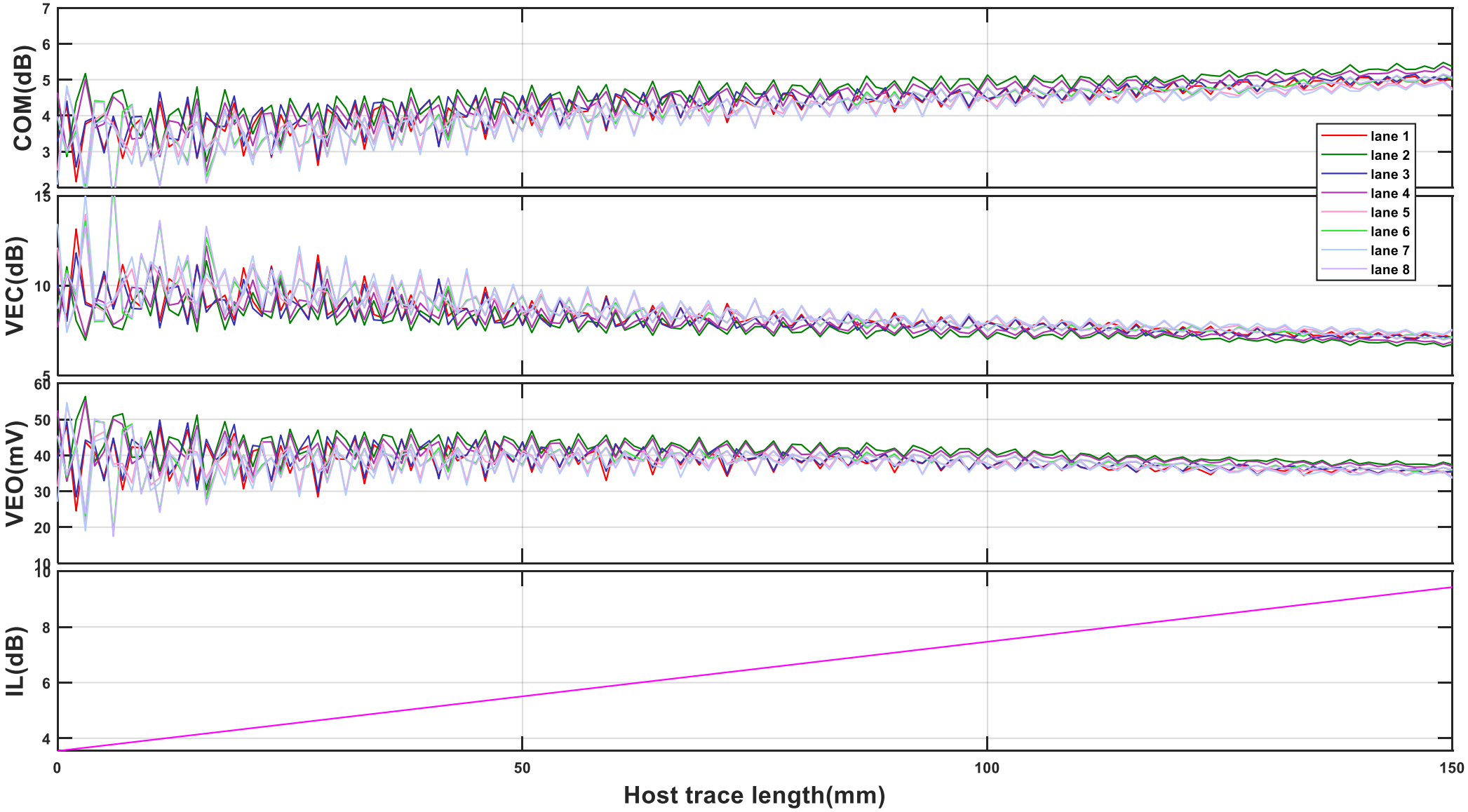
- PCB loss at 26.56GHz: ~0.04dB/mm, ~1dB/in. (58mm is equivalent to the 2.3dB MCB loss being proposed in the cable small group).
- Package loss at 26.56GHz: 0.1dB/mm
- Insertion loss plotted in this report includes host, module and connector, but not package.

Effect of channel length, and connector lane

Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host



Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host

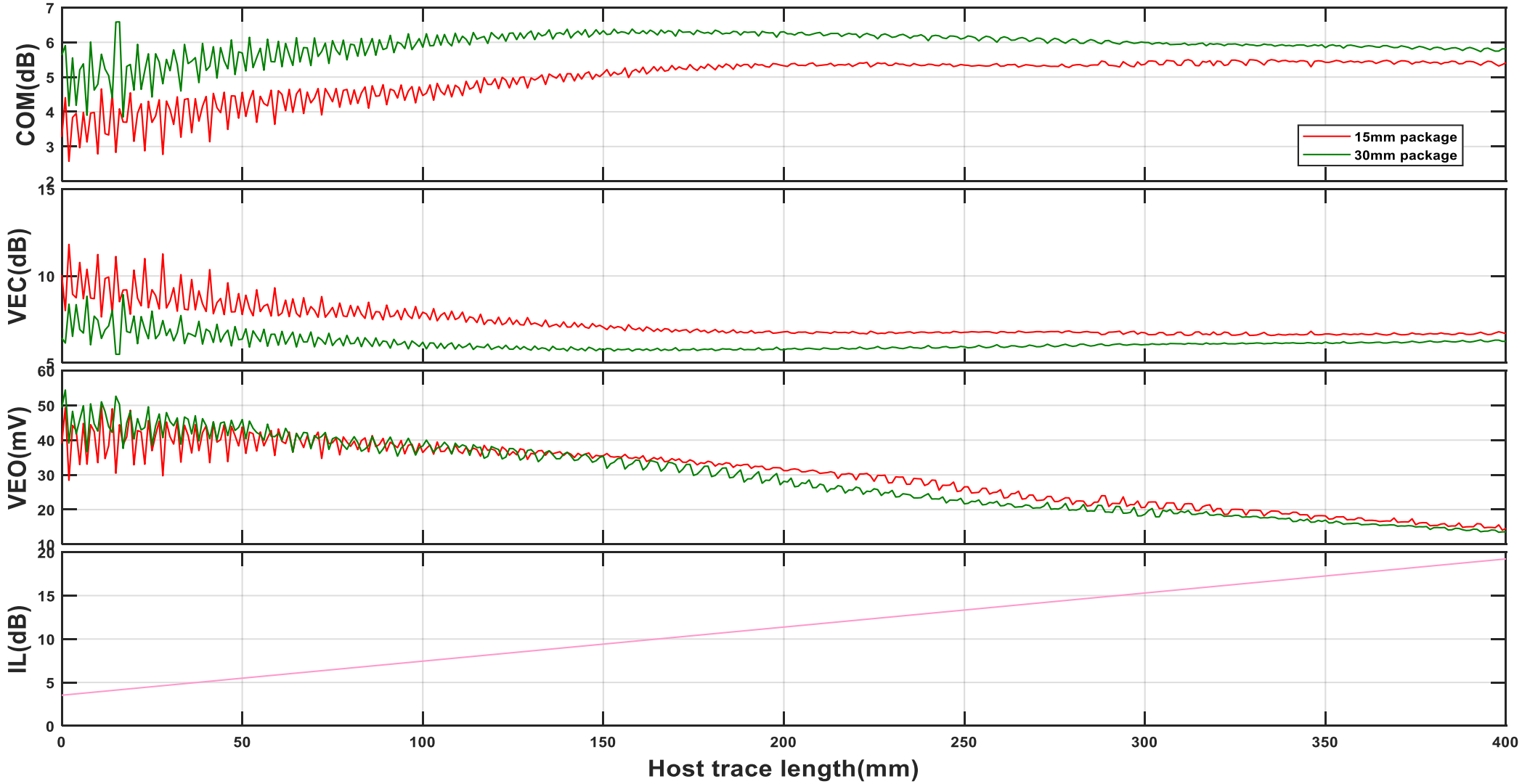


Conclusions.

- Longer host traces (higher loss) degrade VEO but significantly improve COM and VEC.
- This implies that the COM performance is dominated by reflections.
- For short traces the exact length of the host trace matters, but the good lengths vary depending on the connector lane making it necessary to assume worst length.
- With the 4 tap DFE even with no additional impairments the COM for short traces is marginal. Impairments that will occur in a real chip to module link are listed below. Some of these and some potential improvements are investigated in the following slides.
  - Effect of package length
  - Effect of connector crosstalk
  - Effect of vias and impedance discontinuities in the host traces
  - Effect of better die model
  - Effect of other equalizers
  - Effect of having additional reflections in a real module rather than the perfect HCB.
  - Effect of having a real connector on the output of the HCB.

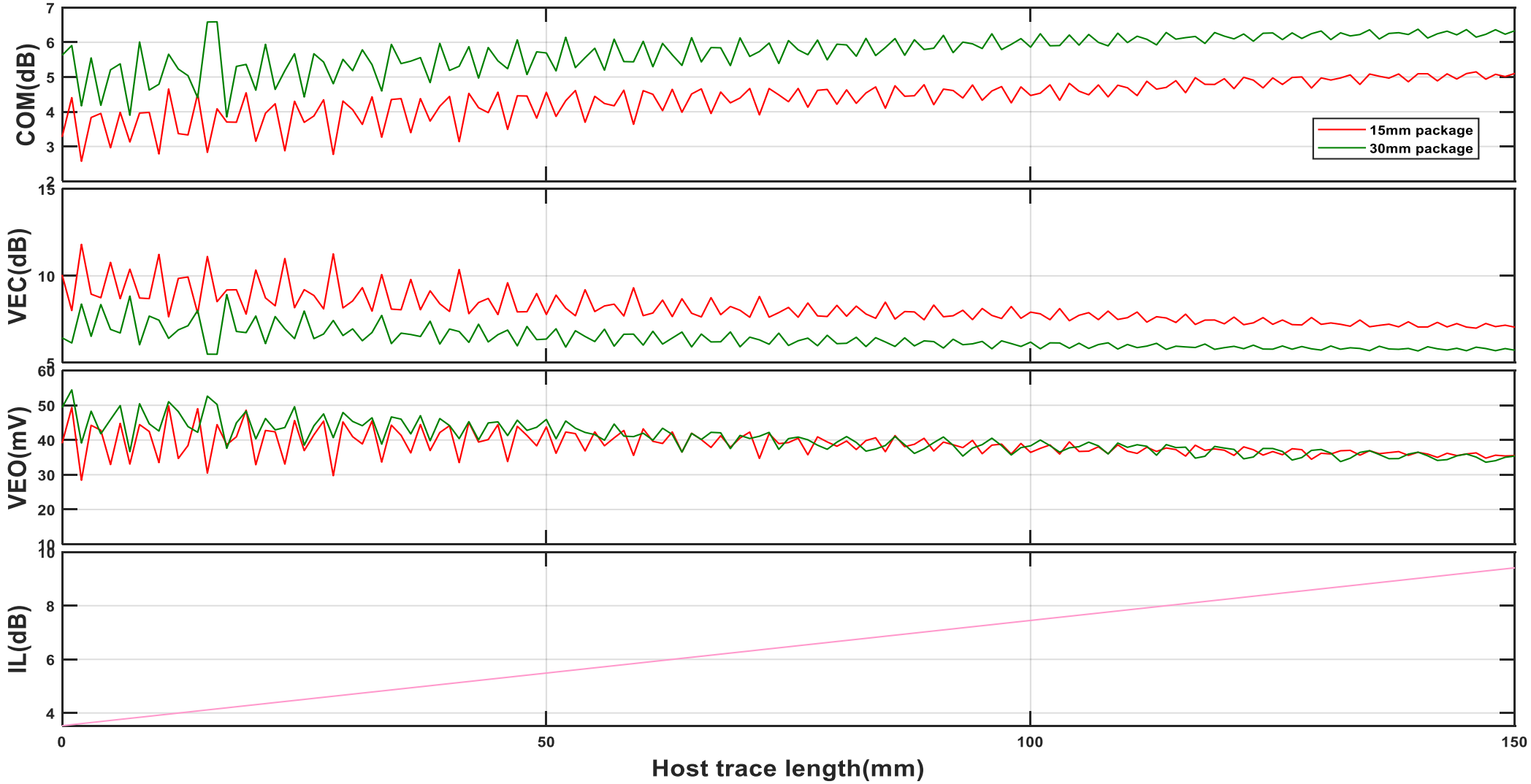
Effect of package length

Cd 0.11pF Ls 0pH Cb 0pF 100ohm host



Longer package trace (more loss) is better for COM and VEC although slightly worse for VEO

Cd 0.11pF Ls 0pH Cb 0pF 100ohm host

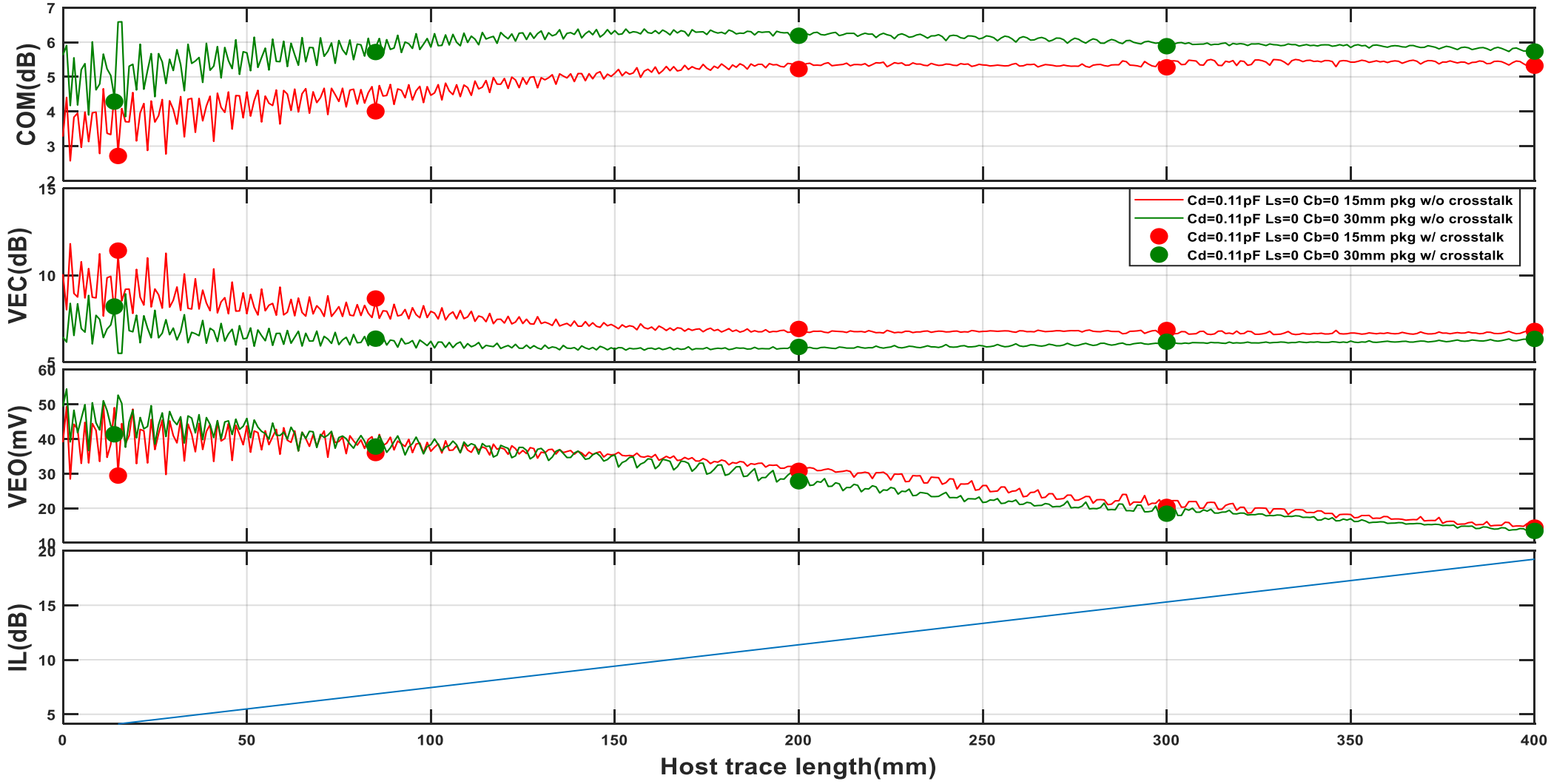


The “good” host trace lengths are different for different package lengths.

Effect of crosstalk

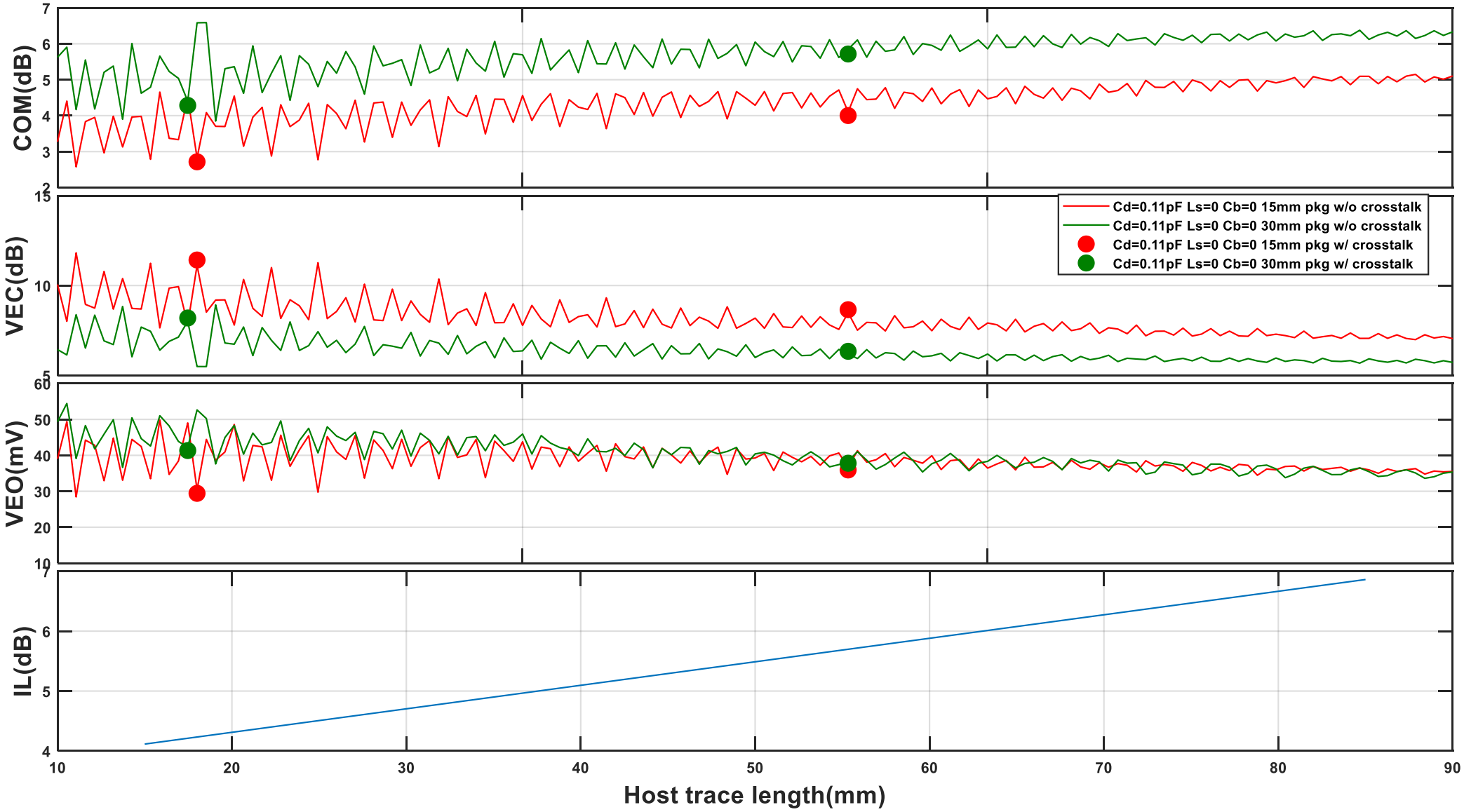
Performance was simulated just at some host lengths with connector crosstalk added

100ohm host impedance



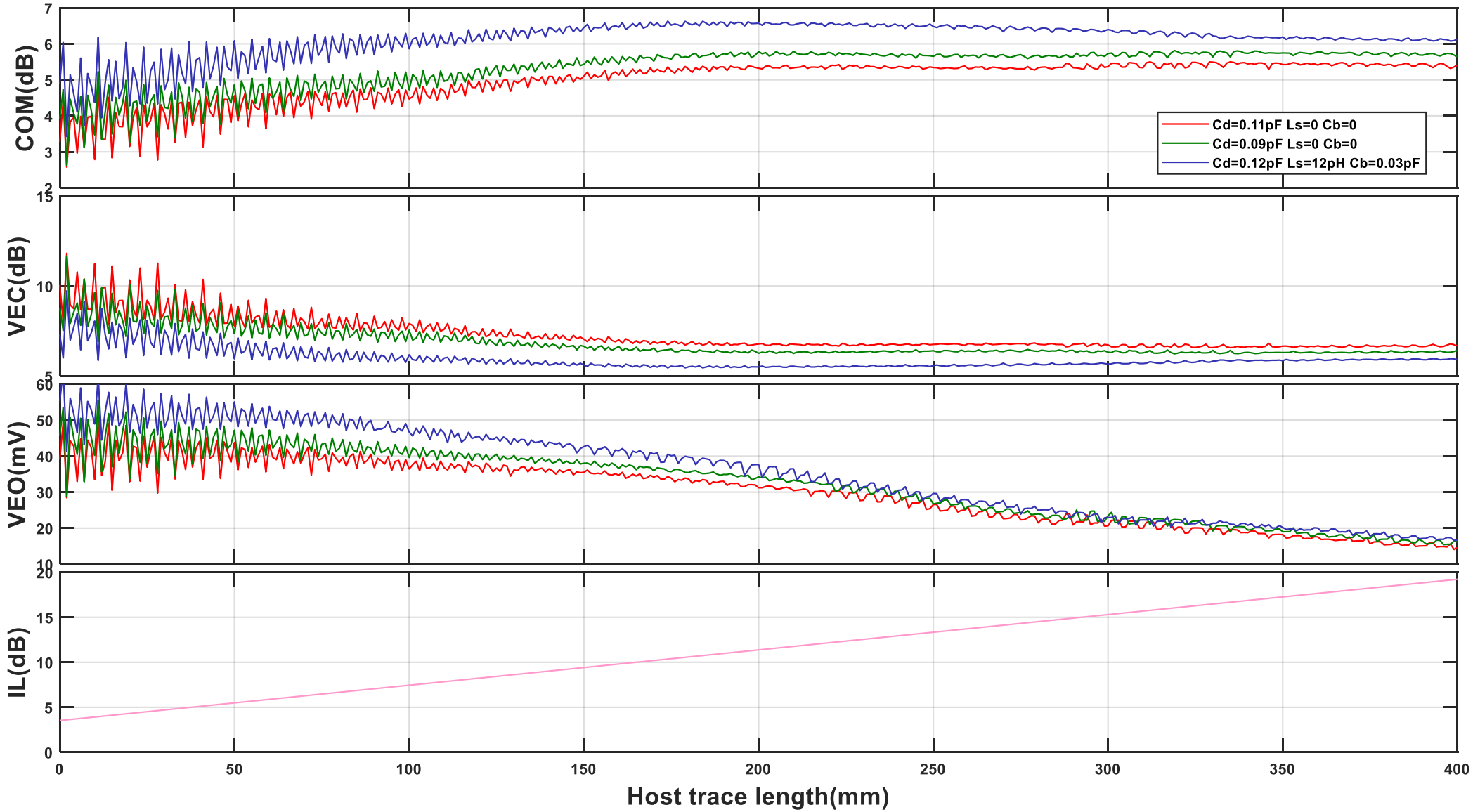
Crosstalk is not a significant degradation for this connector with these trace lengths.

100ohm host impedance

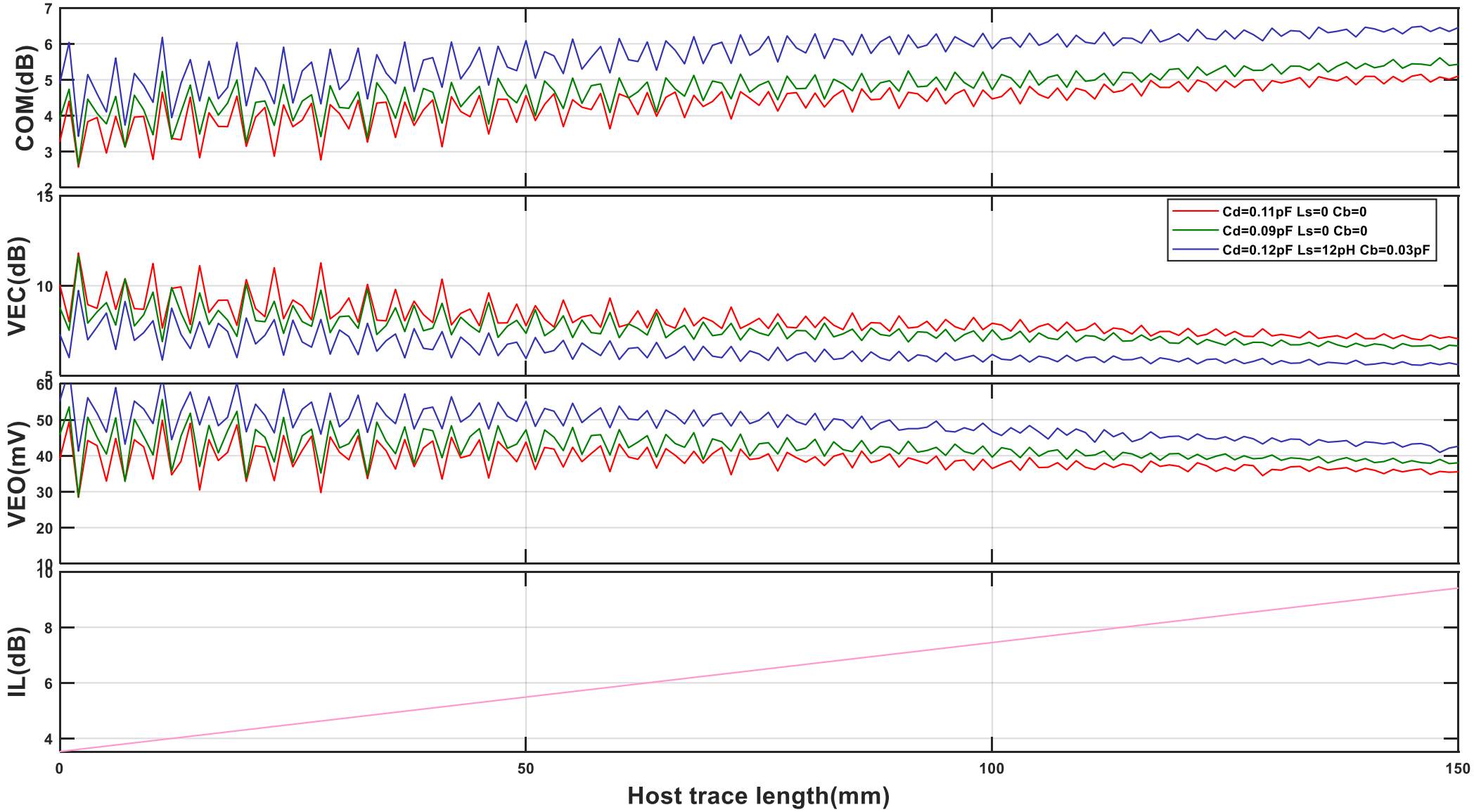


Effect of die model

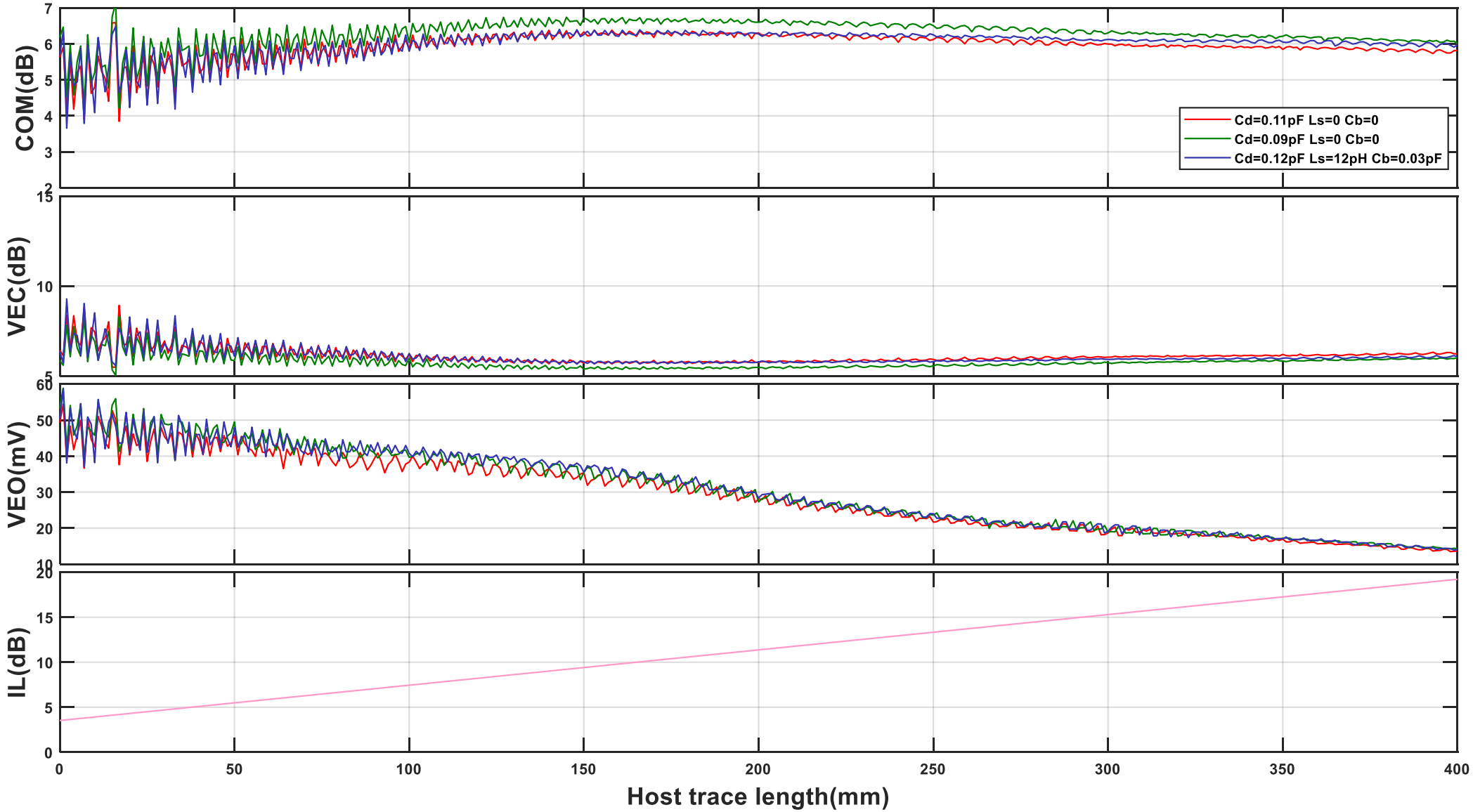
15mm pkg 100ohm host



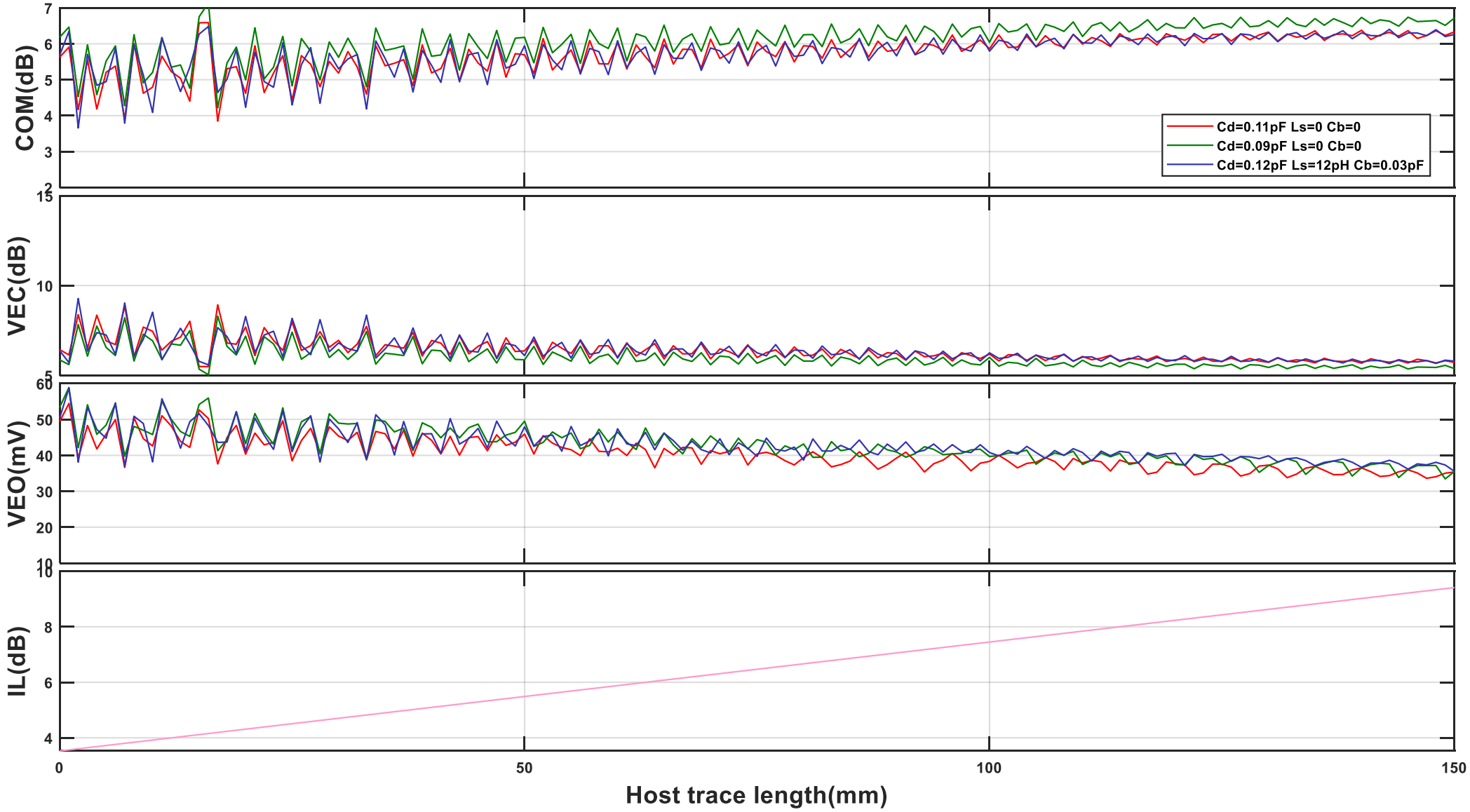
15mm pkg 100ohm host



30mm pkg 100ohm host



30mm pkg 100ohm host

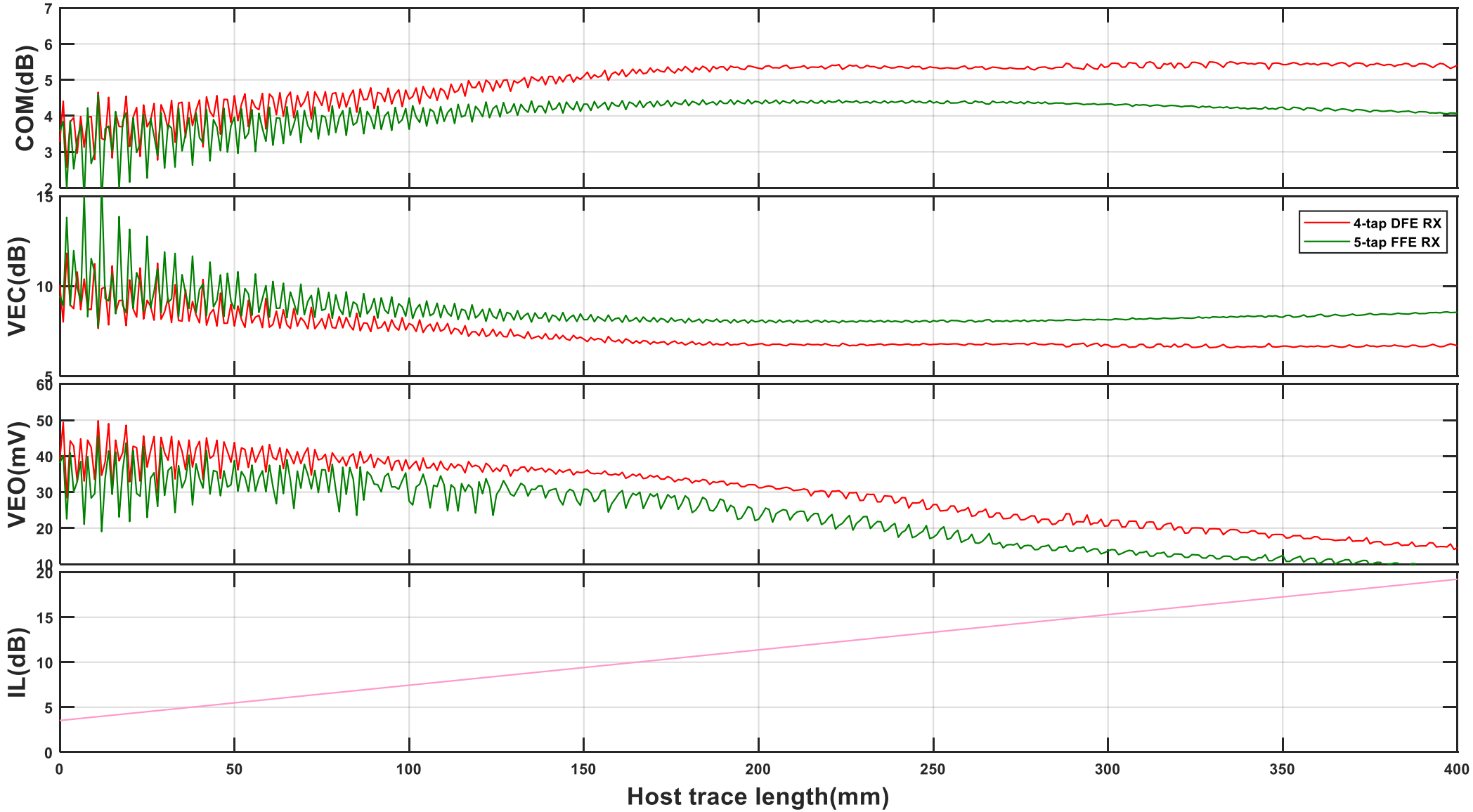


Conclusions on die model.

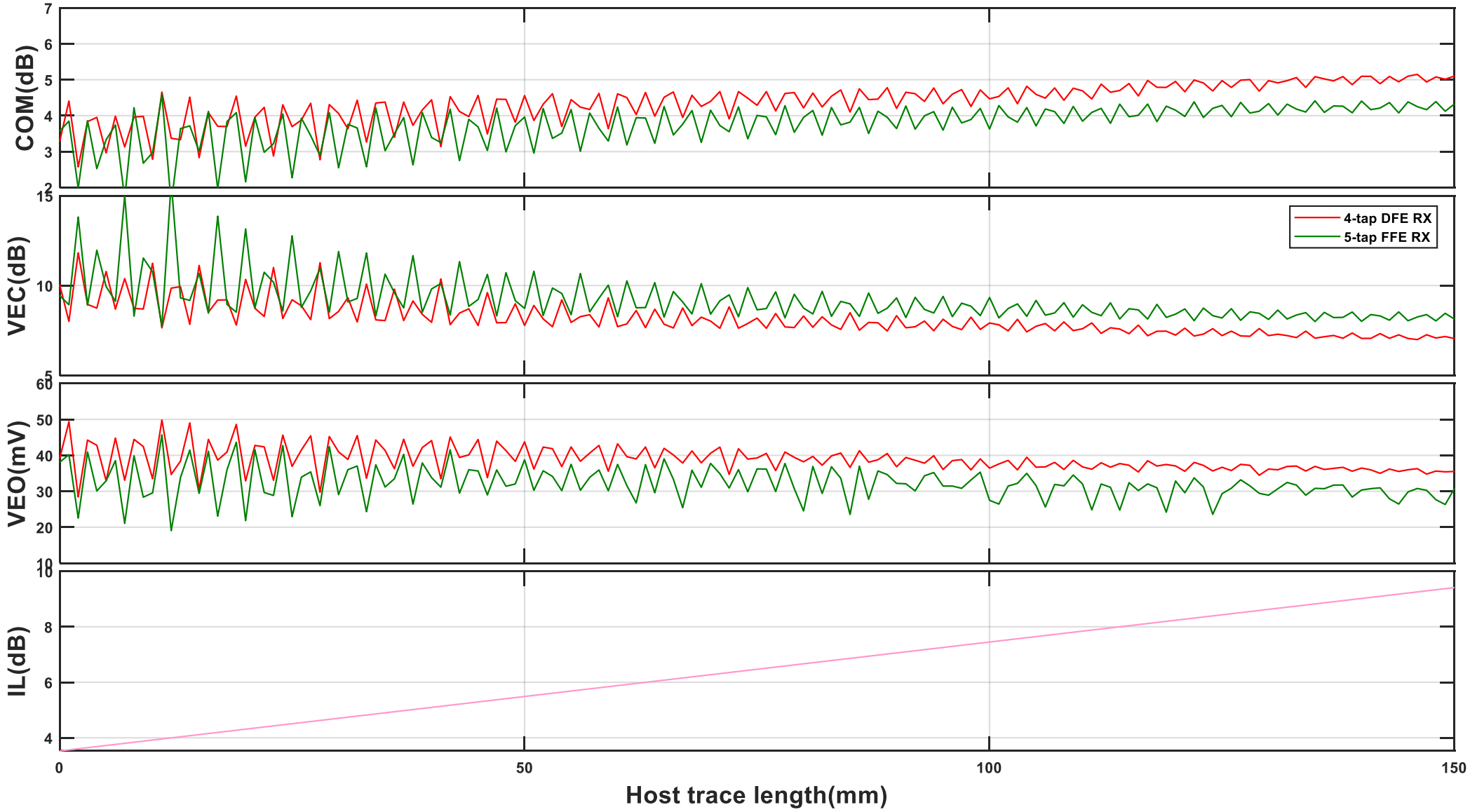
- The new die model including the inductor provides significant improvement for the shorter package trace even over changing C_d to 90pF. This is not apparent for the longer package trace.

Effect of equalization

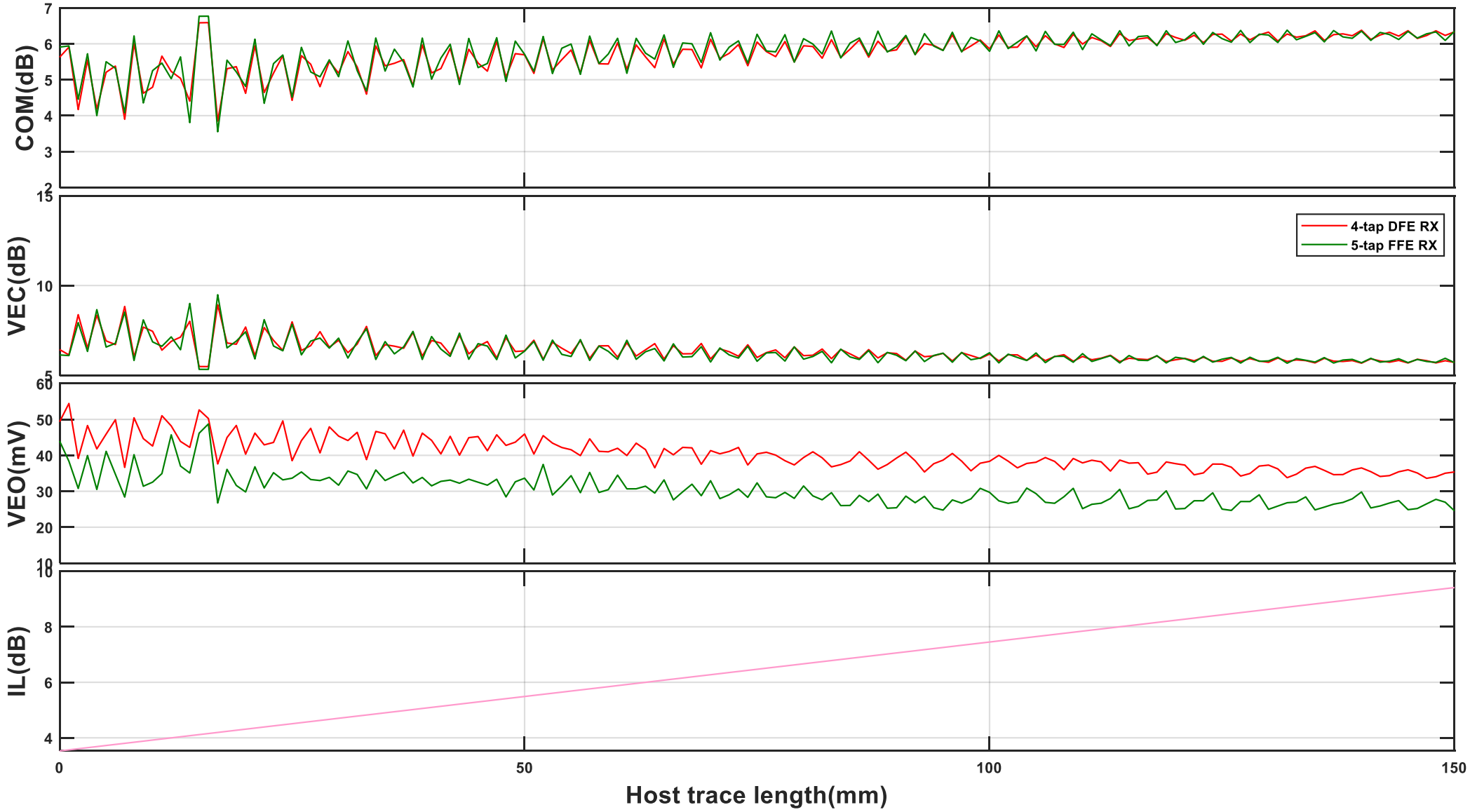
Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host



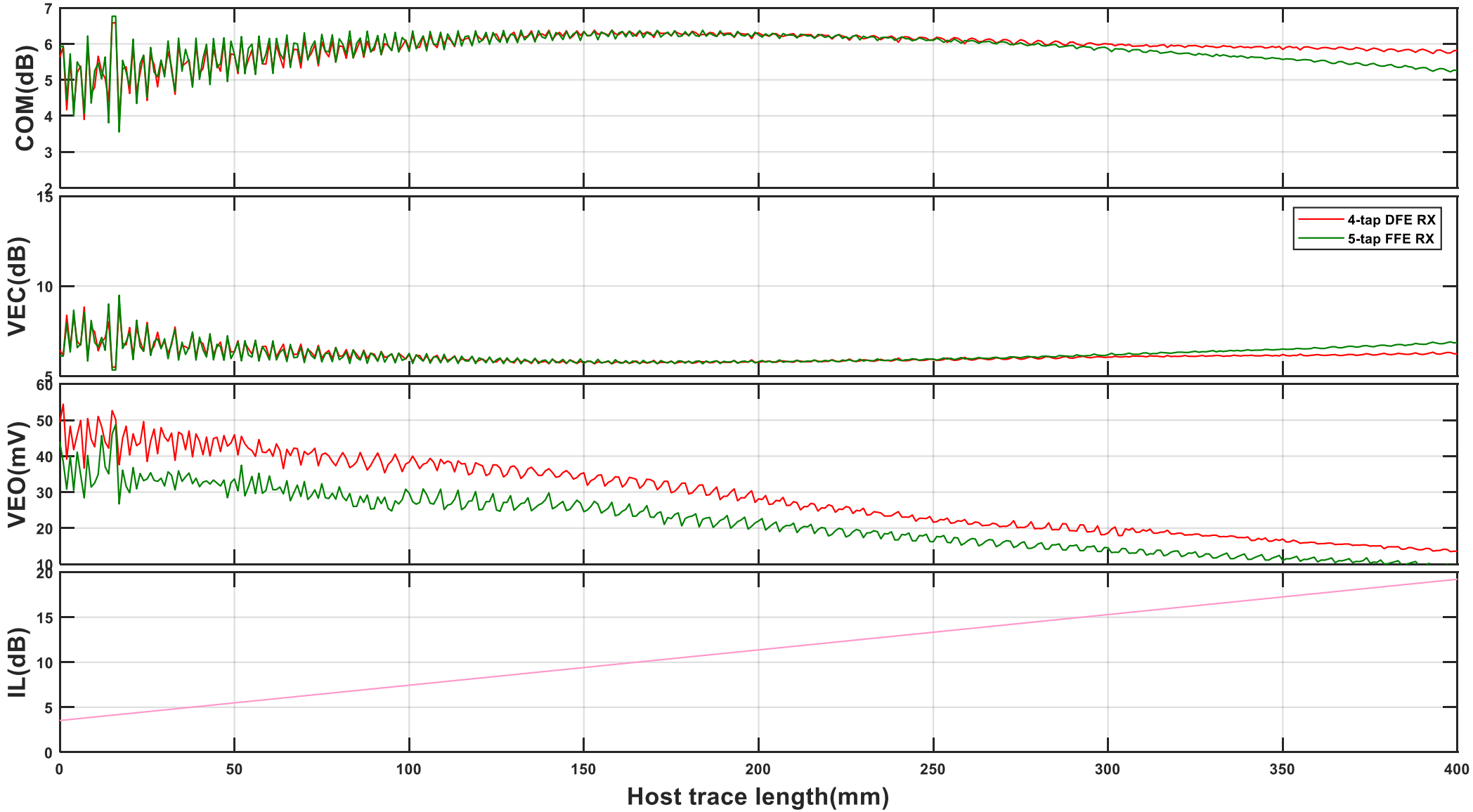
Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host



Cd 0.11pF Ls 0pH Cb 0pF 30mm pkg 100ohm host



Cd 0.11pF Ls 0pH Cb 0pF 30mm pkg 100ohm host

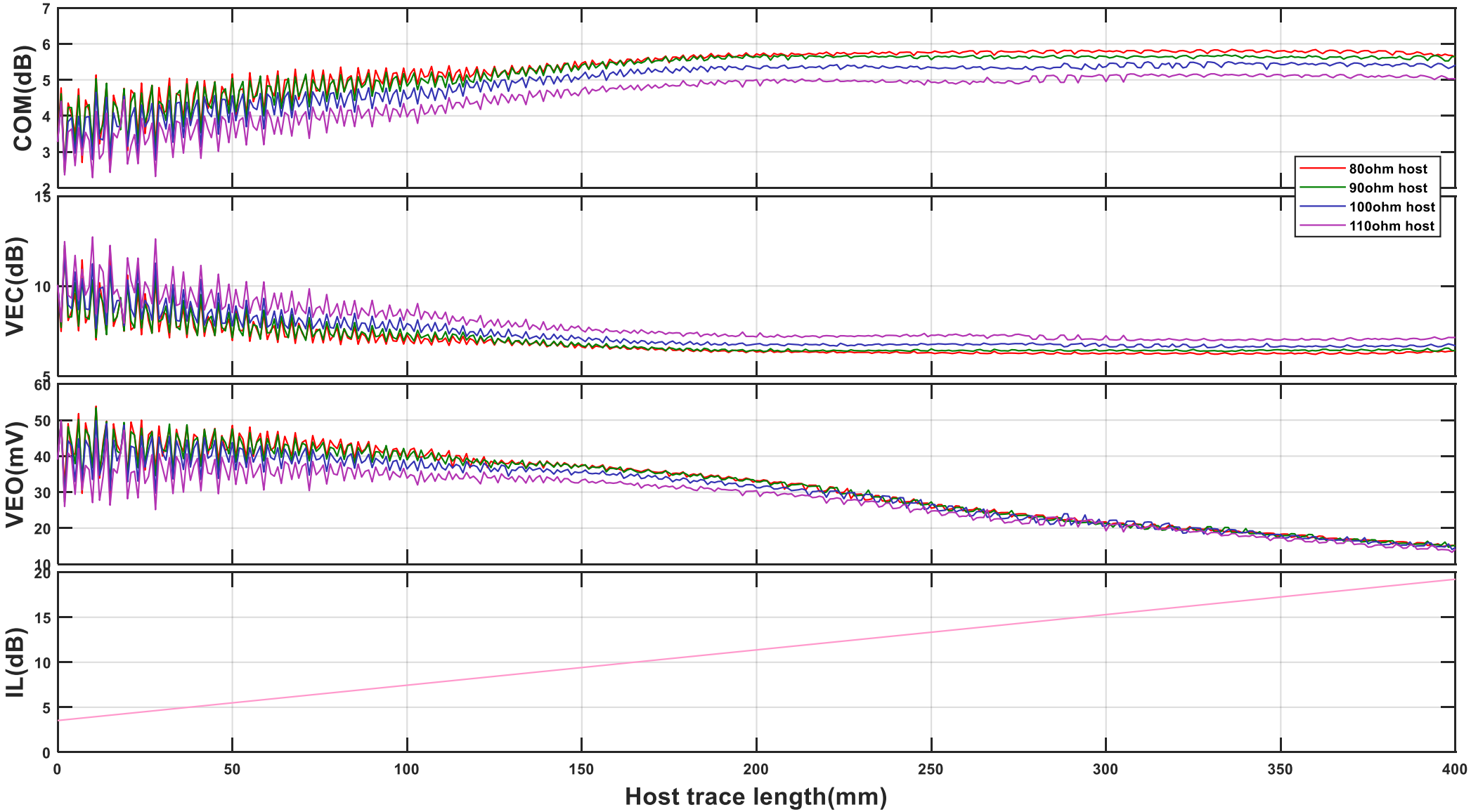


Conclusions on Equalization.

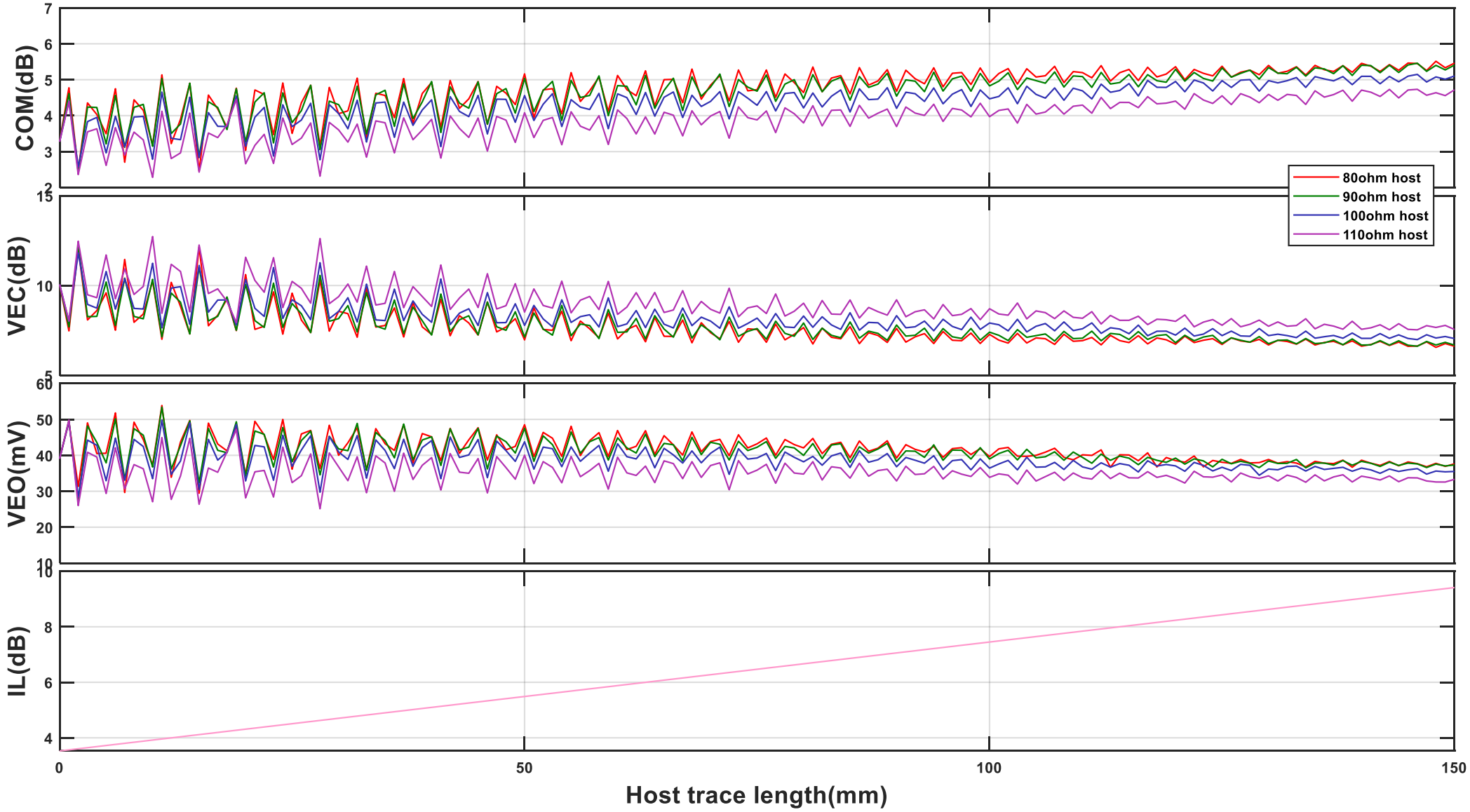
- Using the 5 tap FFE instead of the 4 tap DFE does not make a lot of difference to COM and VEC for the 30mm package but significantly degrades the performance with the 15mm package.
- Using the 5 tap FFE instead of the 4 tap DFE always degrades VEO.

Effect of host trace impedance

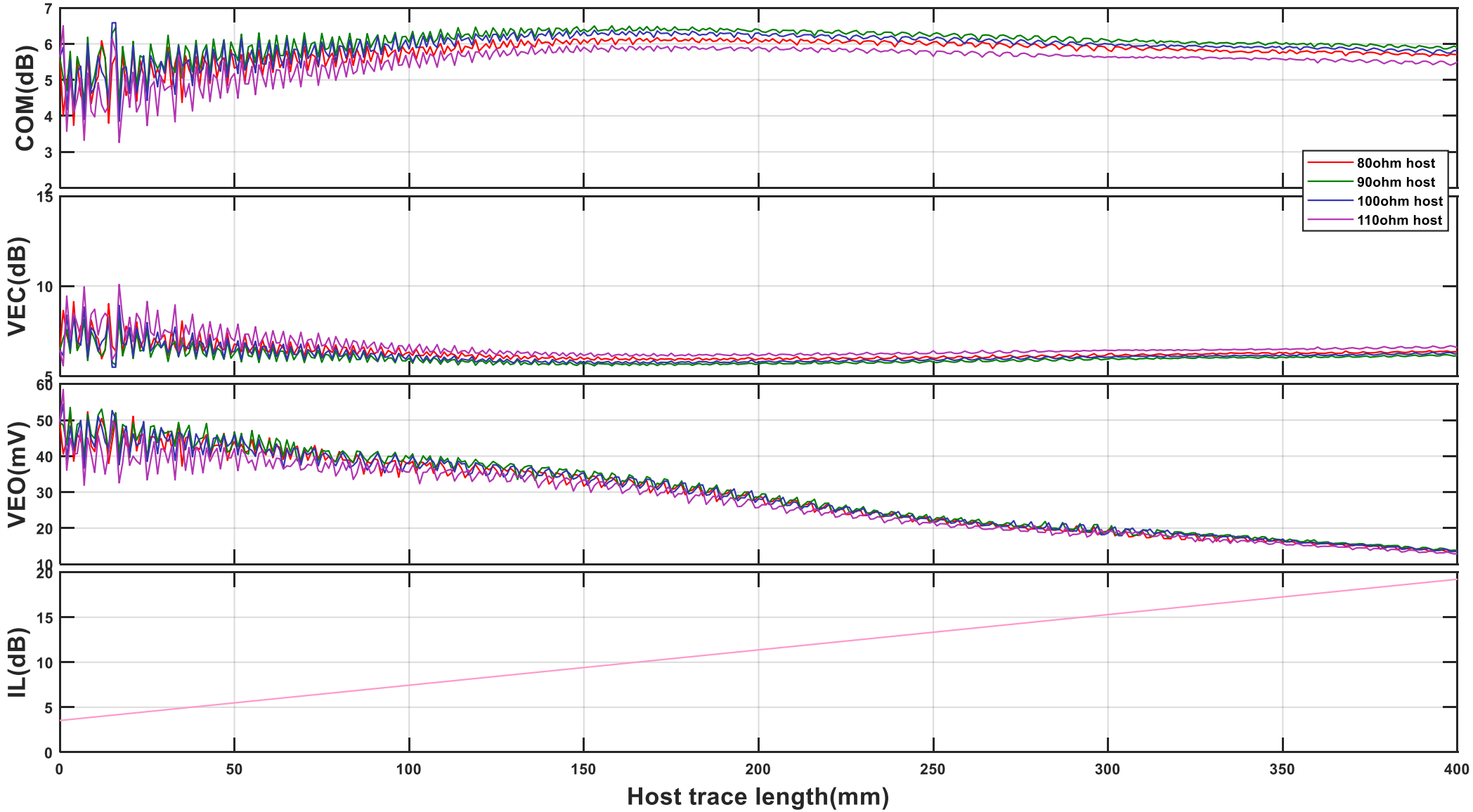
Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg



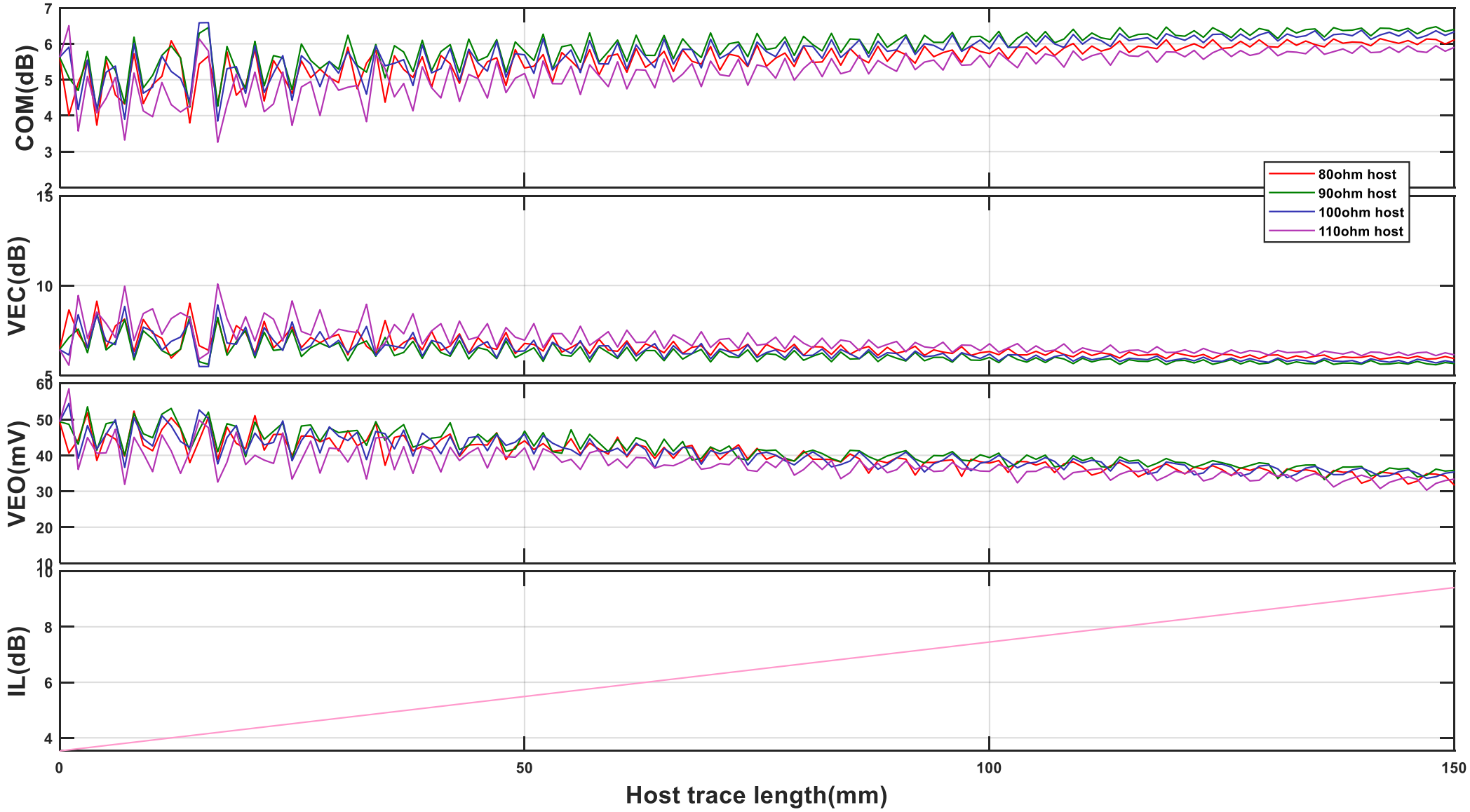
Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg



Cd 0.11pF Ls 0pH Cb 0pF 30mm pkg -contd



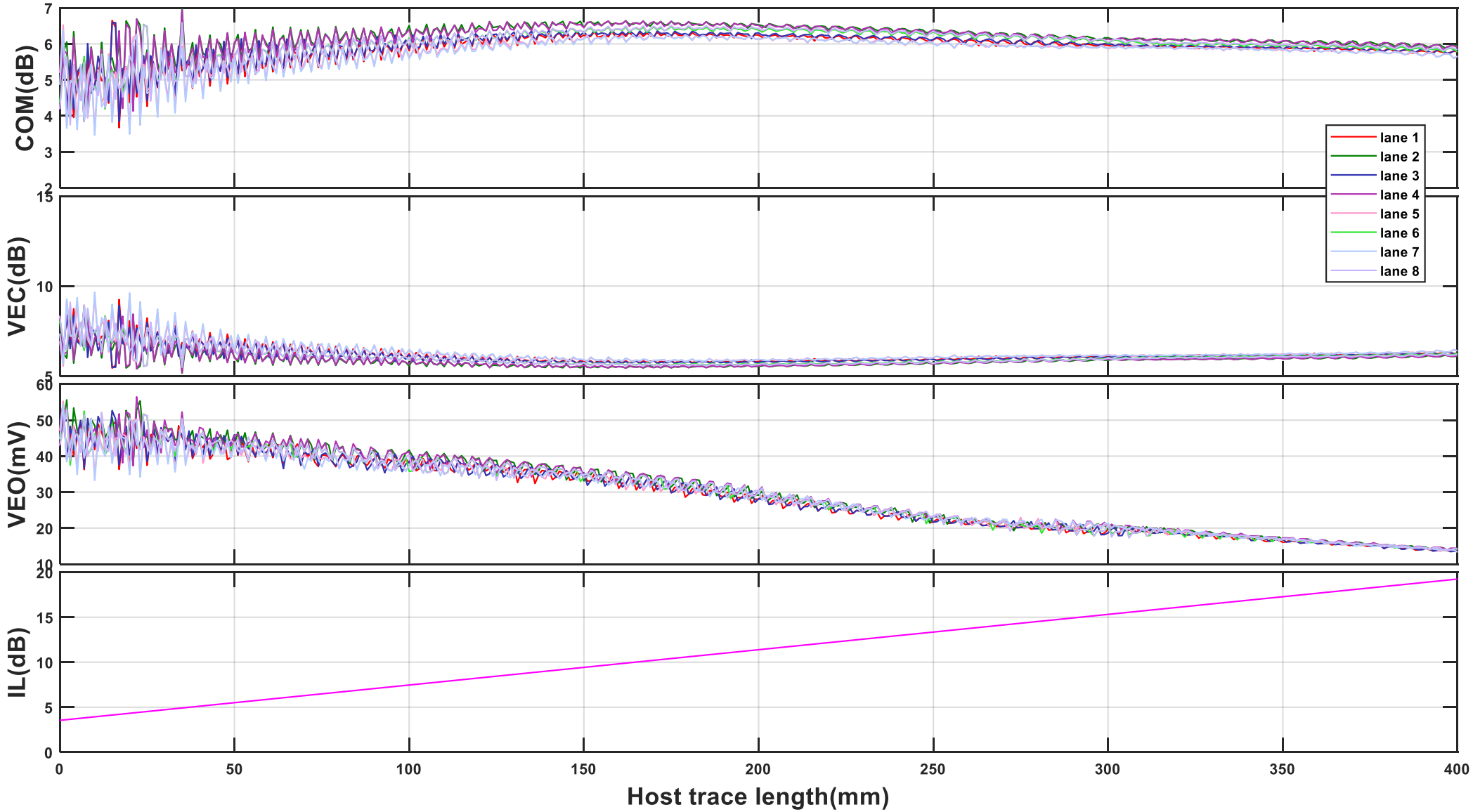
Cd 0.11pF Ls 0pH Cb 0pF 30mm pkg



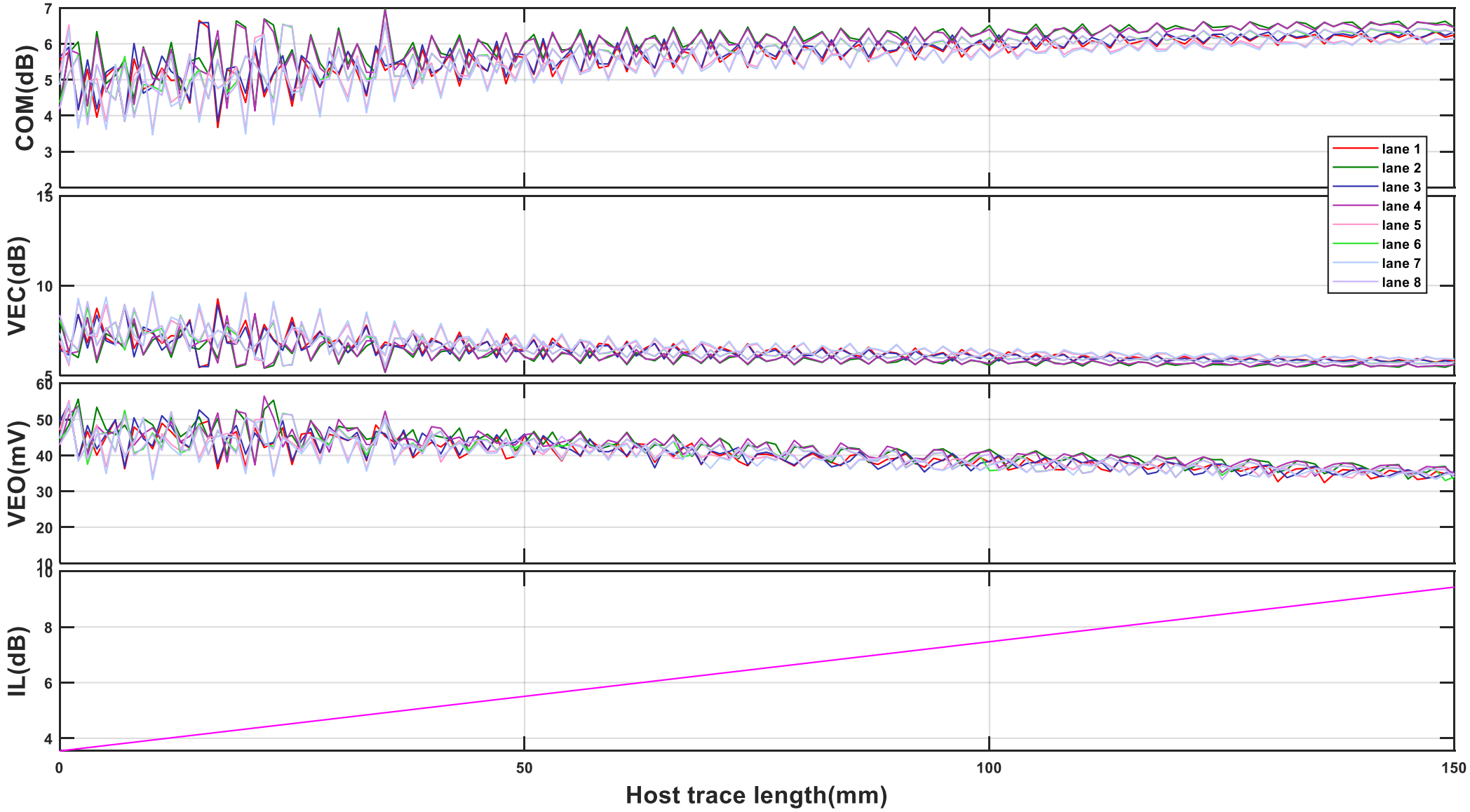
Back-up

Effect of channel length, and connector lane on 30mm package

Cd 0.11pF Ls 0pH Cb 0pF 30mm pkg 100ohm host -contd



Cd 0.11pF Ls 0pH Cb 0pF 30mm pkg 100ohm host



COM spreadsheet for 4-tap DFE RX

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 0]	nF	[TX RX]
L_s	[0.12, 0]	nH	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	[15 15; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[15 15; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0; 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.415	V	
A_fe	0.415	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.1]		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	4	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-14:1:-3]	dB	[min:step:max]
f_z	12.58	GHz	
f_p1	20	GHz	
f_p2	28	GHz	
g_DC_HP	[-3:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
ffe_pre_tap_len	**0**	UI	
ffe_post_tap_len	0	UI	
Include PCB	1	logical	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	0		

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	esults\100GEL_WG_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_1218	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	0	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	300	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	**0.3**	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	
TDR_W_TXPKG	1	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92–12 parameters			
Parameter	**Setting**		
board_tl_gamma0_a1_a2	*[0 3.8206e-04 9.5909e-05]*		
board_tl_tau	*5.790E-03*	ns/mm	
board_Z_c	[100 100]	Ohm	TX RX
z_bp (TX)	*7*	mm	
z_bp (NEXT)	*0*	mm	
z_bp (FEXT)	*0*	mm	
z_bp (RX)	*7*	mm	

COM spreadsheet for 5-tap FFE RX

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 0]	nF	[TX RX]
L_s	[0.12, 0]	nH	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	[15 15; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[15 15; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0; 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.415	V	
A_fe	0.415	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.1]		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	0	UI	
b_max(1)	0		
b_max(2..N_b)	0		
g_DC	[-14:1:-3]	dB	[min:step:max]
f_z	18.88	GHz	
f_p1	28	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-3:1:0]		[min:step:max]
f_HP_PZ	0.00025	GHz	
ffe_pre_tap_len	**0**	UI	
ffe_post_tap_len	4	UI	
Include PCB	1	logical	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	0		

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	'esults\100GEL_WG_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_1218	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	0	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	300	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	**0.3**	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	
TDR_W_TXPKG	1	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 3.8206e-04 9.5909e-05]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	[100 100]	Ohm
z_bp (TX)	*7*	mm
z_bp (NEXT)	*0*	mm
z_bp (FEXT)	*0*	mm
z_bp (RX)	*7*	mm

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