How to Proceed on C2C Application

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Straw Polls Results

- **C2C-L had 71% support and No might be as some view it too close to KR**
- **C2C-S has stronger support possibly because it fill a void given that it can operate with end-end FEC.**

Straw Poll #10:

I support the task force effort to define a C2C-L AUI similar to ghiasi_3ck_02_0519.

Yes: 20 No: 8 Abstain: 12

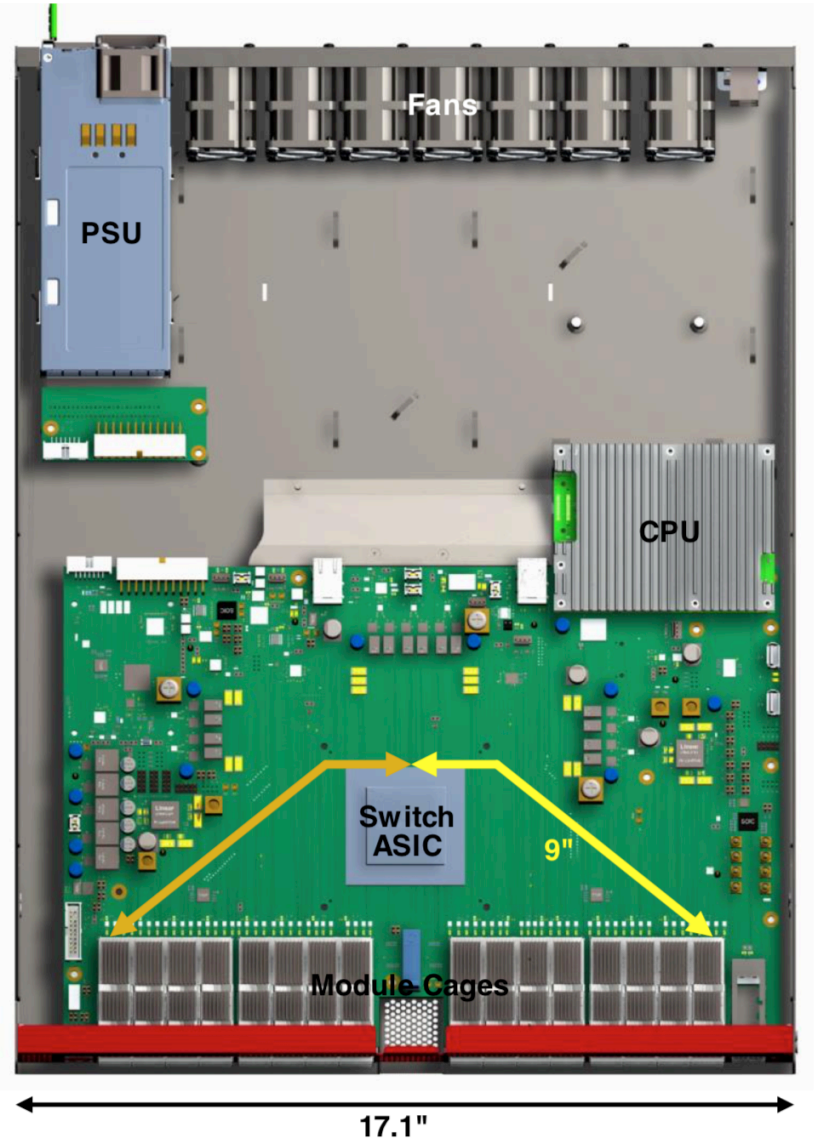
Straw Poll #11:

I support the task force effort to define a C2C-S AUI similar to ghiasi_3ck_02_0519 with loss TBD.

Yes: 30 No: 0 Abstain: 9

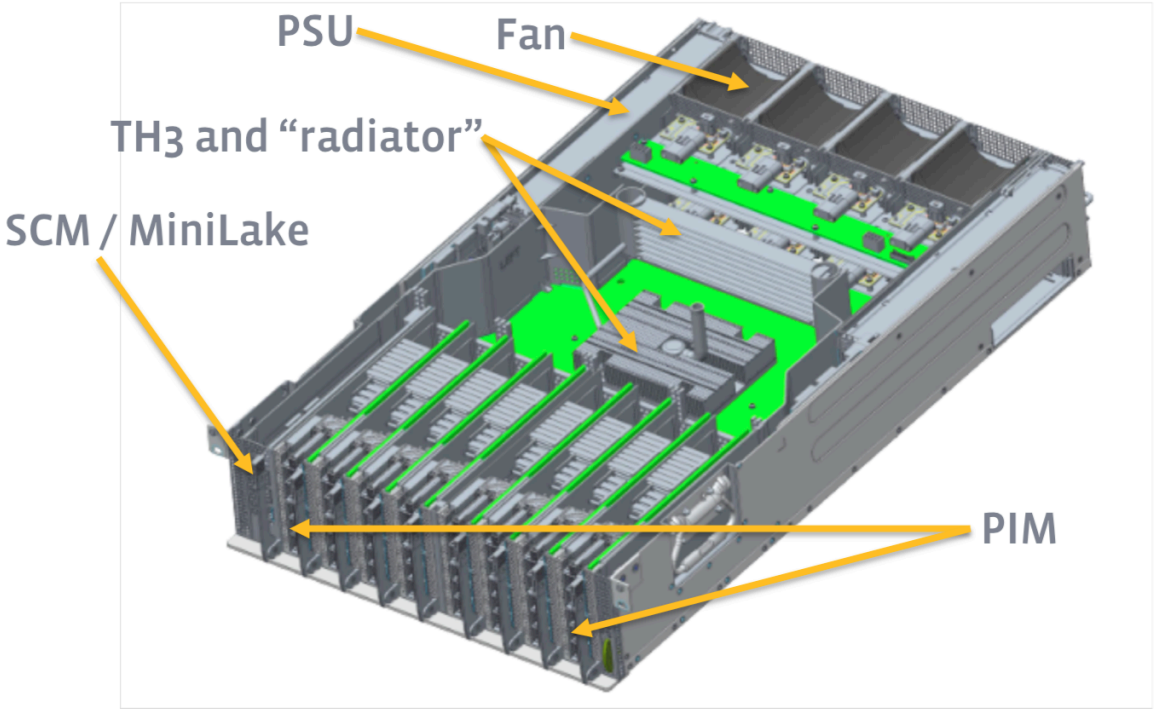
TOR Trace Length

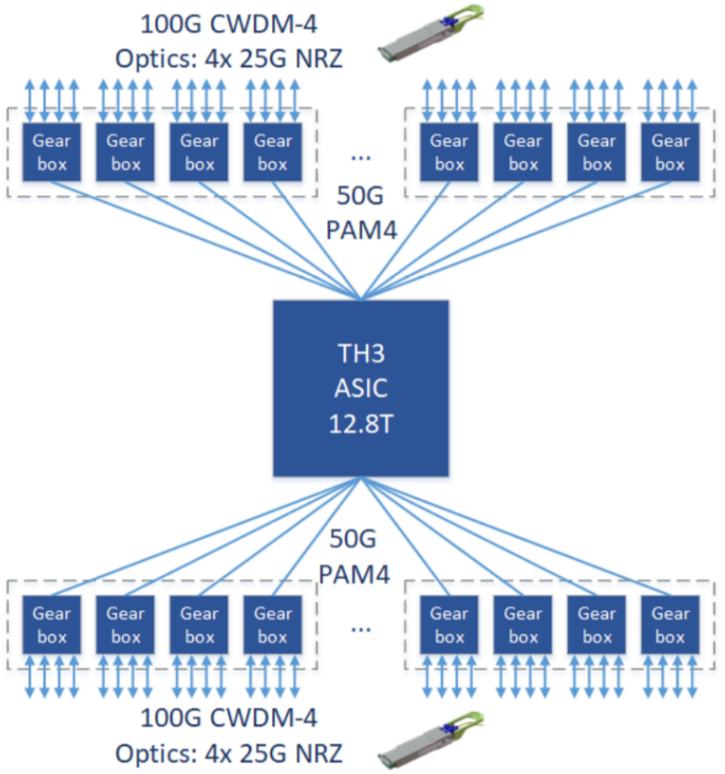
- **Max trace for TOR switches according Rob Stone a well design system may have 9” long traces**
  - Assuming 1.25 dB/in and 1 dB for 2 vias a 9” host trace loss will be 12.5 dB
  - http://www.ieee802.org/3/100GEL/public/18_03/stone_100GEL_01_0318.pdf
- **To achieve 9” long traces it require rotating ASIC by 45 degree otherwise traces could be ~11”**
  - Assuming 1.25 dB/in and 1 dB for 2 vias a 11” host trace loss will be 14.75 dB
- **Potentially ~1/3 of the optical ports will require retimer**
- **Potentially ~2/3 of the Cu/optical ports will require retimer**
- **Need a low power-cost C2C-C2M CDR solution!**



Facebook Minipack

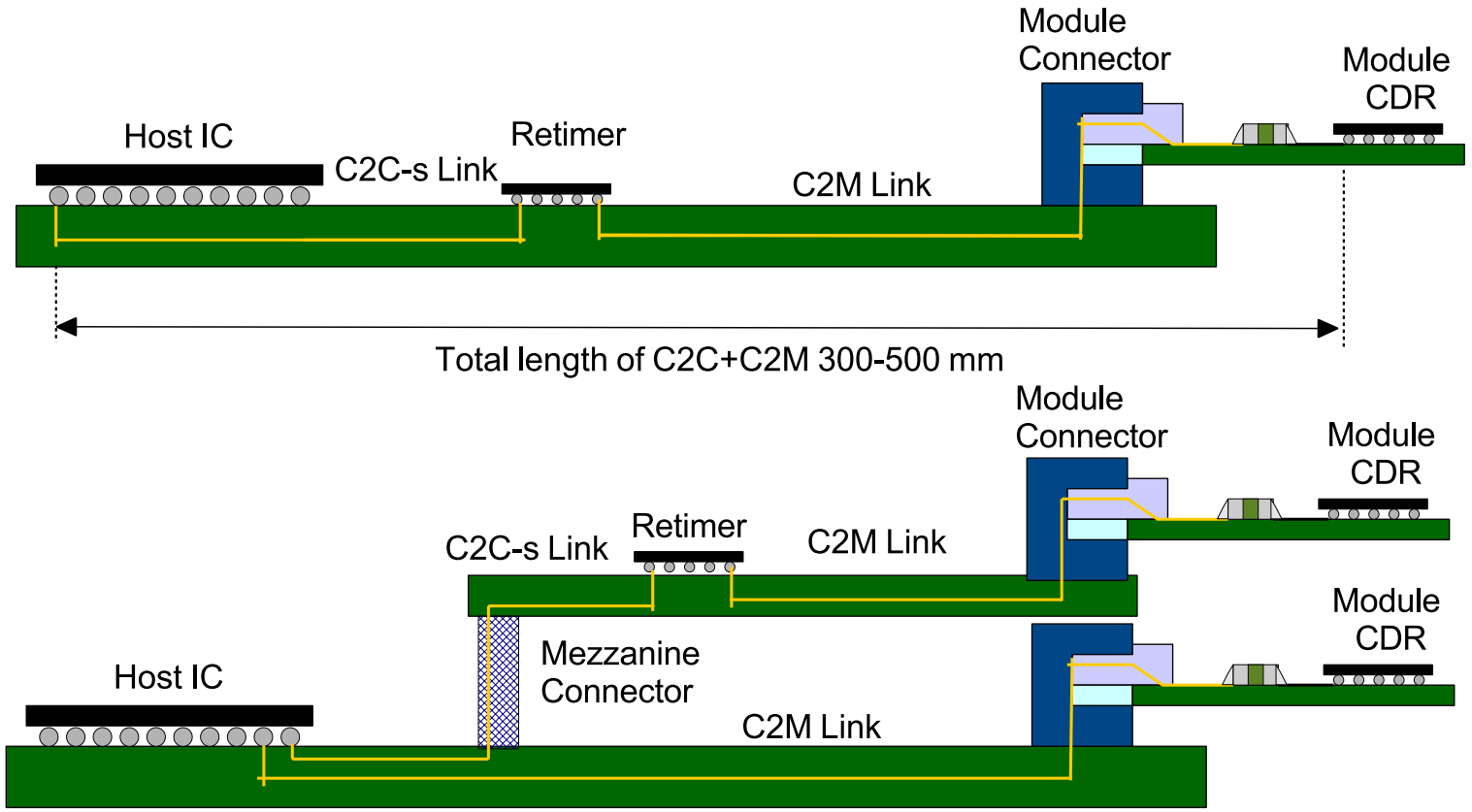
- **4 RU design with Tomahawk III and inverse-mux to 128 QSFP28**
  - The trace length for this system is about 16” (Meg 7 1.25 dB/in) total for main board plus the daughter card
  - The estimated total loss will be 20 dB for PCB, 2 dB for connector, and 2 dB for 4 vias for total loss of 24 dB
  - Minipack will be more in line with C2C-L as 20 dB C2C not sufficient.





Two Common C2C-S Applications

- **These two common C2C-S applications can satisfied with ~300 mm trace and by repurposing 16 dB C2M budget**
  - Connecting to far-side of the ASIC IO may require retimer
  - Modules mounted on mezzanine card.



Overview of C2C-S and C2C-L Attributes

- **C2C-S will leverage C2M equalizer and operate with end-end FEC**
- **Can we safely increase C2C-S to 20 dB and still operate with end-end FEC?**

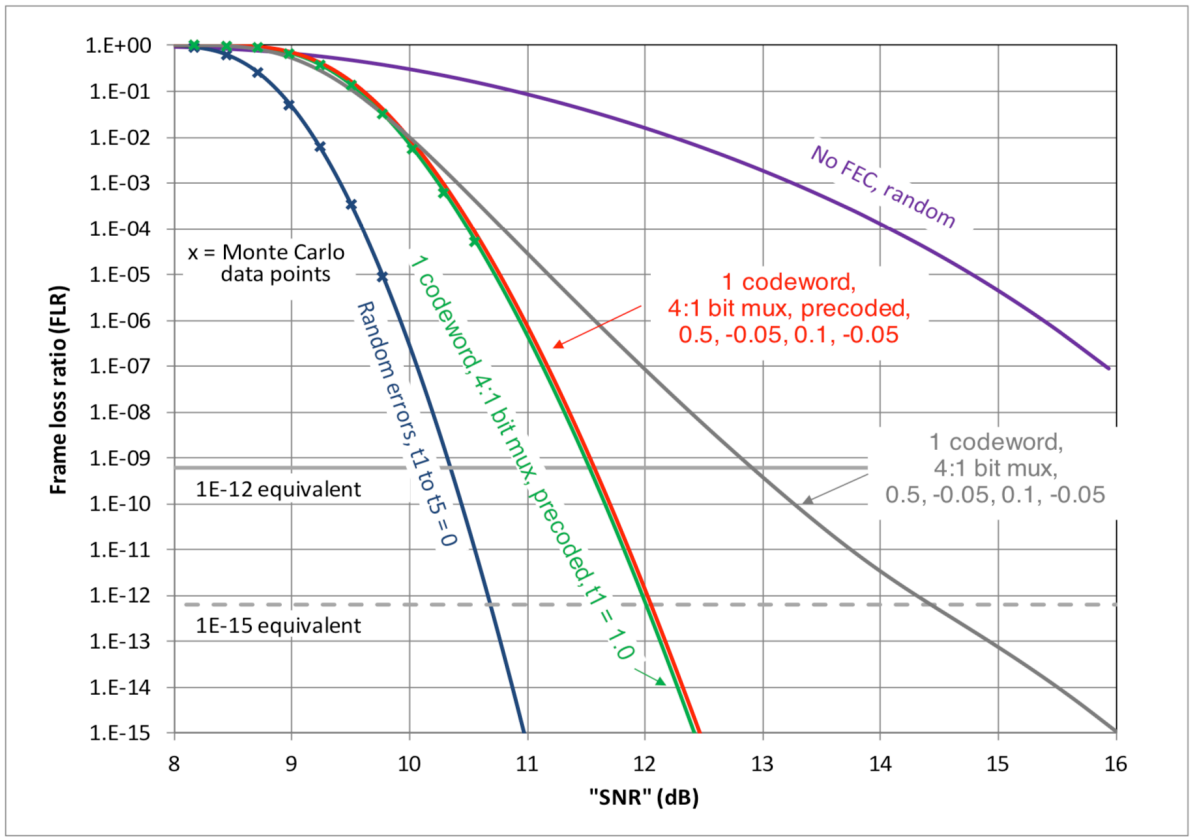
Parameters	C2M	C2C-S	C2C(MR)	KR	C2C-L
Chip configuration	ASIC to CDR	ASIC to CDR	ASIC to ASIC	ASIC to ASIC	ASIC to ASIC
Link configuration	One Connector	One Connector	One Connector	2 Connectors	One Connector
Host PCB Reach (mm)	~225	~280	~360	~500	~500
FEC operation	Pass Through	Pass Through	?	Terminated	Terminated
FEC Interleave/Non-Interleave	NA	Same as C2M	Same as C2M	TBD for 100G	Same as KR
Back Channel Link Training	NA	NA	Optional	Required	Optional
[ASIC, CDR] Trace Lengths (mm)	[30, 8]	[30,15]	[30,30]	[30,30]	[30,30]
[ASIC, CDR] Package Losses (dB)	[4, 1]	[4,2]	4+4	4+4	4+4
Max channel loss at Nyquist (dB)	16	15	20	28	26.5*
Max Bump-Bump Loss (dB)	~21	~21	~28	~36	~34.5

* C2C-L loss is lower by 1.5 dB compare to KR because the link only has one connector with about same PCB loss.

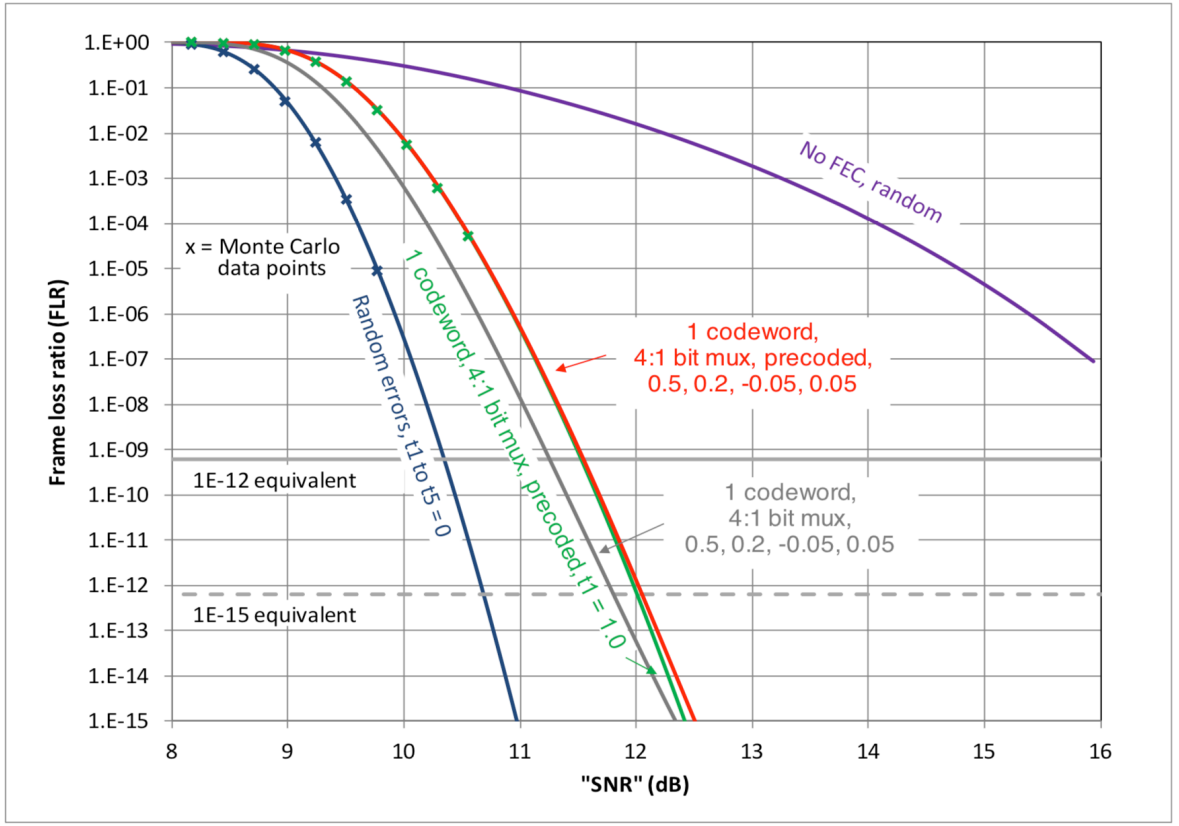
Largest DFE Taps That Link Segment Can Operate with End-End FEC

- **DFE burst error analysis for 4 tap DFE, please see [anslow_3ck_01_0119]**
  - Recommended DFE taps limit for 4 tap is 0≤t1 ≤0.5, -0.05≤t2 ≤0.2, -0.05≤t3 ≤0.1, -0.05≤t4 ≤0.05

100G 4 tap DFE(0.5, -0.05, 0.1, -0.05) worst without precoding

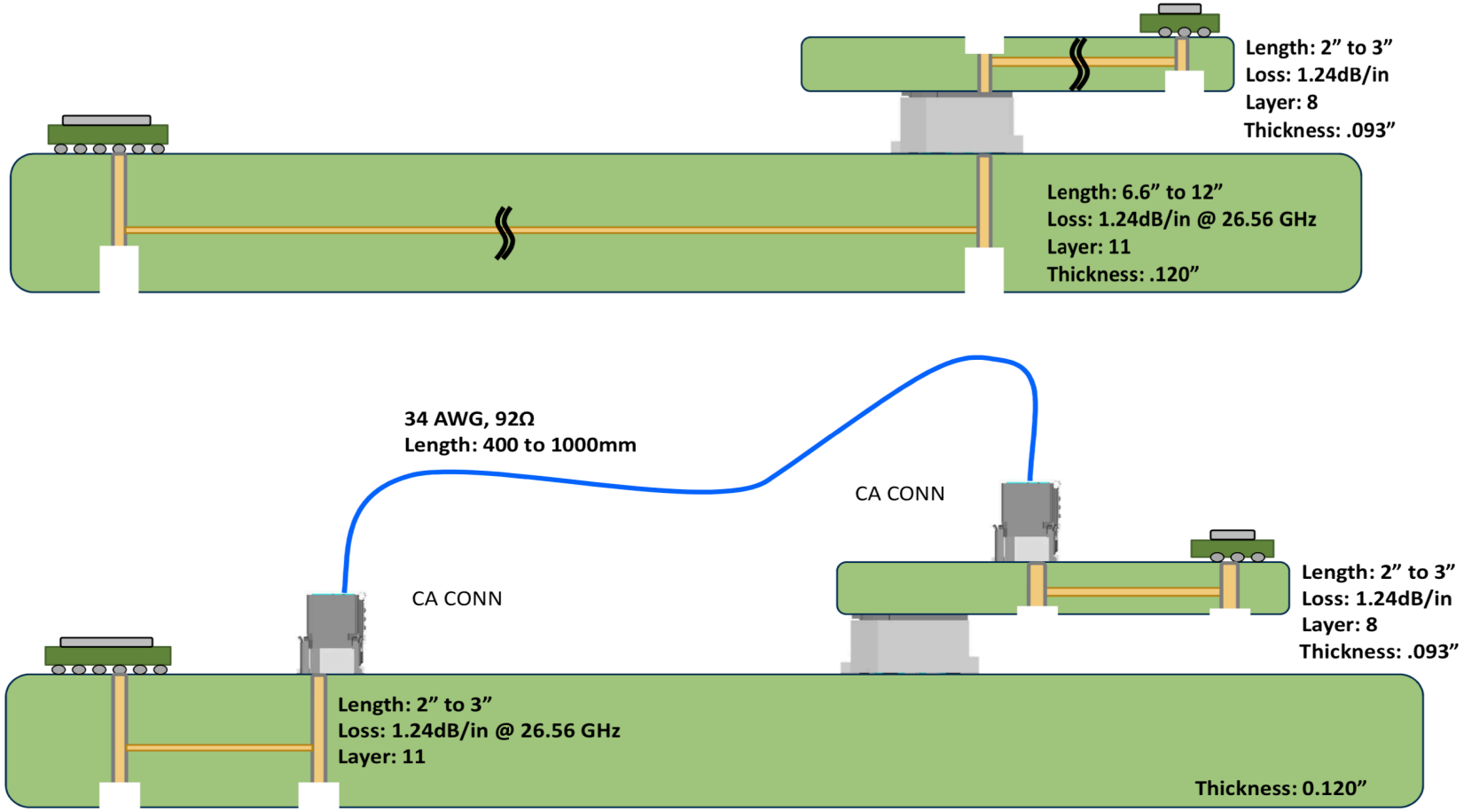


100G 4 tap DFE(0.5, 0.2, -0.05, 0.05) worst with precoding



C2C Channels

- **Construction of C2C channels based on PCB and cable construction provided by Brandon Gore**
  - http://www.ieee802.org/3/ck/public/19_05/gore_3ck_01a_0519.pdf

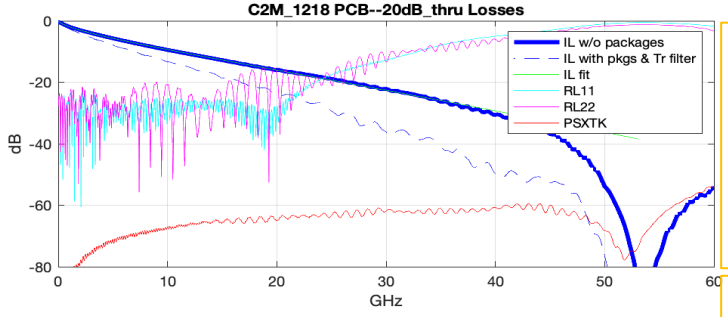


COM 2.7 Table for C2C and C2C-L

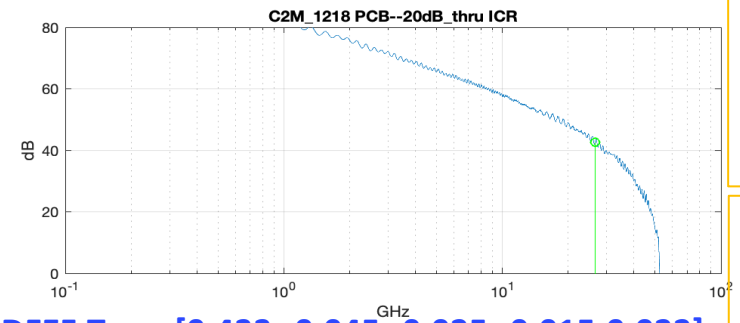
Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.1	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.1400E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_WG_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12 0.12]	nF	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]		RUNTAG	C2M_1218			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	
z_p (TX)	[15 30; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[15 30; 1.8 1.8]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[15 30; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	232	mm
z_p (RX)	[15 30; 1.8 1.8]	mm	[test cases]		DER_0	1.00E-04			z_bp (NEXT)	232	mm
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	232	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	0	mm
R_d	[45 45]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.413	V			TDR and ERL options						
A_fe	0.413	V			TDR	1	logical				
A_ne	0.608	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	300					
f_r	0.75	*fb			TDR_Butterworth	1	logical				
c(0)	0.54		min		beta_x	1.70E+09					
c(-1)	[-0.34:0.02:0]		[min:step:max]		rho_x	0.25					
c(-2)	[0:.02:0.12]		[min:step:max]		fixture delay time	0					
c(1)	[-0.1:0.05:0]		[min:step:max]		TDR_W_TXPKG	1					
N_b	12	UI			N_bx	4	UI				
b_max(1)	0.5				Receiver testing						
b_max(2..N_b)	0.2				RX_CALIBRATION	0	logical				
g_DC	[-20:1:0]	dB	[min:step:max]		Sigma BBN step	5.00E-03	V				
f_z	21.24	GHz									
f_p1	53.1	GHz			Noise, jitter						
f_p2	21.24	GHz			sigma_RJ	0.01	UI				
g_DC_HP	[-6:1:0]		[min:step:max]		A_DD	0.02	UI				
f_HP_PZ	0.66375	GHz			eta_0	8.20E-09	V^2/GHz				
ffe_pre_tap_len	0	UI			SNR_TX	33	dB				
ffe_post_tap_len	0	UI			R_LM	0.95					
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.35										
ffe_post_tap1_max	0.35										
ffe_tapn_max	0.2										
ffe_backoff	1										

Gore C2C 20 dB Channels

20 dB PCB Channel



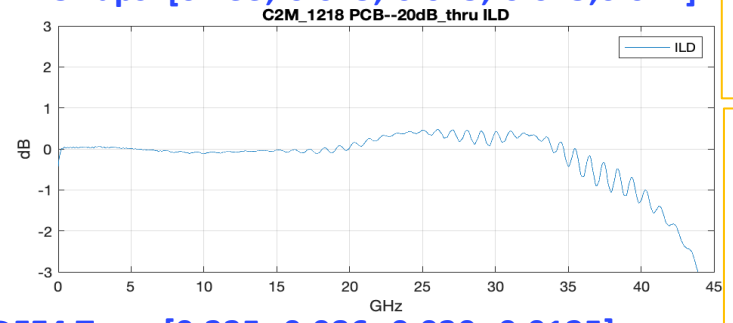
B1(max)=0.5, B[2-12](max)=0.2
COM
Case I=7.13 dB, Case II=5.4 dB
DER at 3 dB COM
Case I=2.4e-12, Case II=1.2e-7



B1(max)=0.5, B[2-8](max)=0.2
COM
Case I=6.1 dB, Case II=5.4 dB
DER at 3 dB COM
Case I=6.0e-9, Case II=1.3e-7

DFE5 Taps=[0.433;-0.045;-0.025;-0.015;0.022]

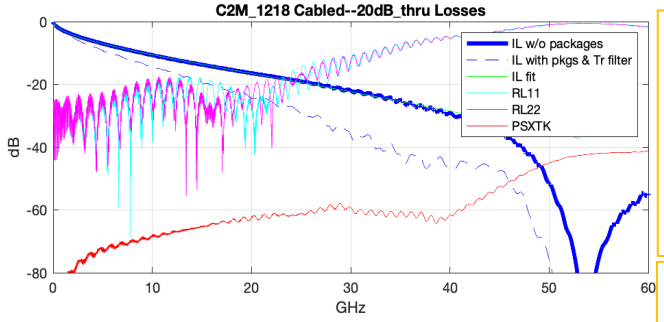
B1(max)=0.5, B[2-5](max)=0.2
COM
Case I=5.9 dB, Case II=5.2 dB
DER at 3 dB COM
Case I=3.3e-8, Case II=2.9e-7



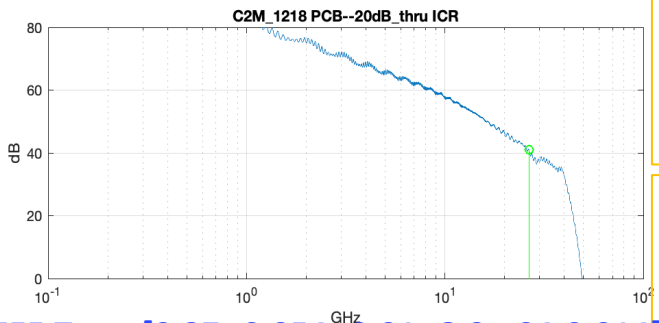
B1(max)=0.5, B[2-4](max)=0.2
COM
Case I=5.5 dB, Case II=5.1 dB
DER at 3 dB COM
Case I=1.5e-7, Case II=4.3e-7

DFE4 Taps=[0.335;-0.086;-0.030;-0.0125]

20 dB Cabled Channel



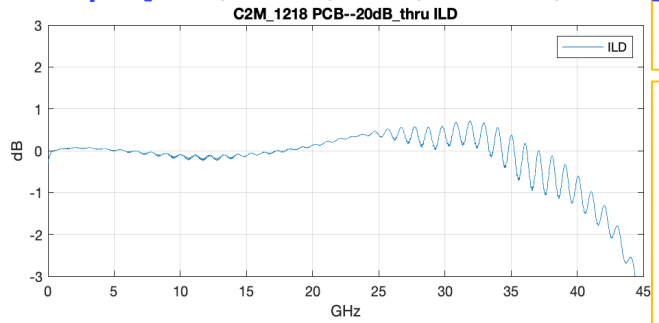
B1(max)=0.5, B[2-12](max)=0.2
COM
Case I=6.9 dB, Case II=5.1 dB
DER at 3 dB COM
Case I=1.0e-10, Case II=1.7e-7



B1(max)=0.5, B[2-8](max)=0.2
COM
Case I=5.9 dB, Case II=4.9 dB
DER at 3 dB COM
Case I=3.0e-8, Case II=9.7e-7

DFE5 Taps=[0.37;-0.054;-0.01;-8.9e-04;0.014]

B1(max)=0.5, B[2-5](max)=0.2
COM
Case I=5.8 dB, Case II=4.8 dB
DER at 3 dB COM
Case I=5.2e-8, Case II=1.2e-6



B1(max)=0.5, B[2-4](max)=0.2
COM
Case I=5.7 dB, Case II=4.8 dB
DER at 3 dB COM
Case I=6.5e-8, Case II=1.2e-6

DFE4 Taps=[0.395;-0.079;-0.045;-0.027]

How to Proceed

- **What should be the loss of C2C-S 16 dB?**
  - What should be C2C-S reference packages
  - Assuming [15, 30] mm for ASIC with 1.8 mm PTH and [4, 15] mm for CDR having PTH of [0, 0.4] mm
- **What should be the loss of C2C-L 26 dB?**
  - What should be C2C-L reference packages
  - Assuming [30, 30] mm for ASIC with 1.8 mm PTH
- **What equalizer would be necessary for each solution assuming bmax=0.5 and b[2, n]=0.2 and DER=1E-5**
  - C2C-S with 16 dB similar to C2M
  - C2C with 20 dB about 5 taps DFE
  - C2C-L with 26 dB about 12 taps DFE
- **Instead of defining C2C-S and C2C-L should we instead define just one C2C with 20 dB if it can be operated with end to end FEC?**
  - Expand C2C-S applications but only have one solution
  - The 20 dB Gore channels can operate with end-end FEC not sure if we can broadly say 20 dB channels can be operated with 5 Tap sufficiently constrain DFE to avoid burst error
  - As shown in case of design such as Facebook minipack 20 dB not sufficient
- **Only C2C-S can leverage C2M equalizer both C2C and C2C-L are new equalizer class given that KR would be overkill for C2C-L.**