Further Discussion on TX dERL Specification

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For IEEE 802.3ck Ad-Hoc

Outlines

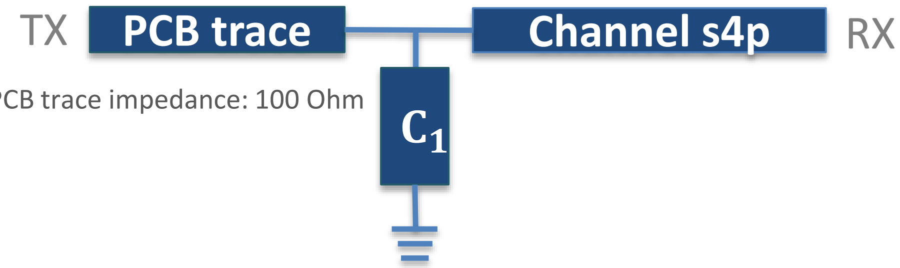
- Background
- TX dERL Impacts on Whole Link Performance
- Conclusion

Background & Proposal

- TX dERL were set as -3 dB based on the analysis in wu_3ck_adhoc_01a_092320
  - dERL = -3 dB was proposed & accepted in D2.0 by considering Z_p, Z_c, & R_d alternated within valid range, as well as test fixture variation
- In dudek_3ck_01_0521, TX dERL = -1 dB was proposed (also in Comment #189 of D2.0)
  - By considering dERL vs. COM with sweeping C_p up to 0.267 pF
  - No consensus on this change for D2.1, but some had concerns on interoperability due to TX dERL = -3 dB
- This contribution leverages diverse channels to evaluate the whole link performance with Tx dERL spec varied from -3 to 0 dB
  - It was noticed that for large values of C_p or C_b will cause serious performance degradation
  - By considering reasonable alternatives of TX parameters, dERL = -3 dB shall be kept under acceptable COM impacts

Channels for Analysis

- Channel diversity generation: 9 IEEE KR channels cascaded with
  - C_1 = [0:25:100] fF
  - PCB trace length = [1 10:10:150] mm
  - Total **720** test channels
  - Channels with ERL < **9.7** dB are removed from the data set



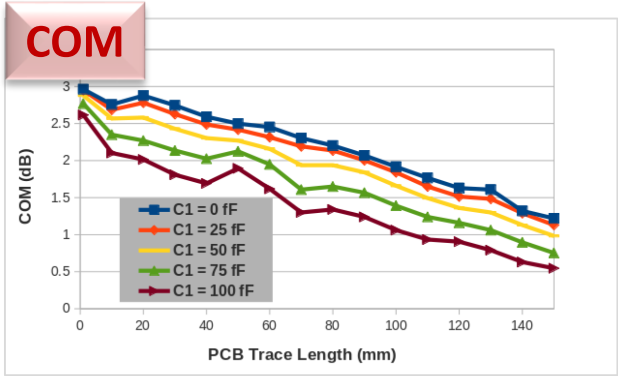
* PCB trace impedance: 100 Ohm

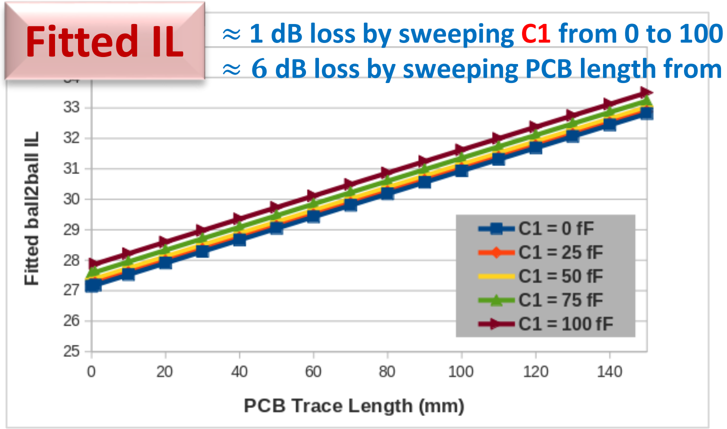
Channel List	NEXT	FEXT
Cable_BKP_28dB_0p575m_more_isi	4	3
Cable_BKP_16dB_0p575m_more_isi	4	3
CaBP_BGAVia_Opt2_28dB	3	5
Std_BP_12inch_Meg7	3	5
DPO_IL_12dB	3	5
OAch4	9	9
CAch3_b2	3	5
Bch2_b7p5_7	3	5
Oach1_t	9	9

Crosstalk channels are included for whole link analysis

Channel Profile

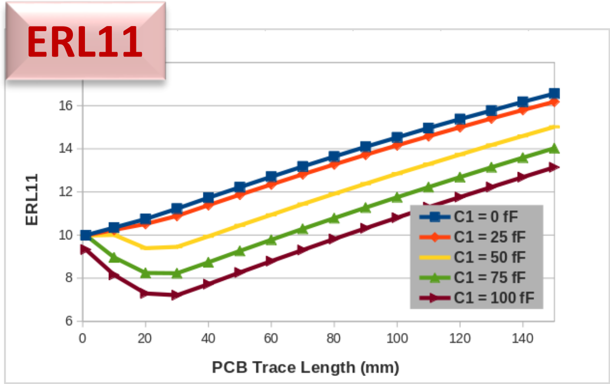
** Take channel "DPO_IL_12dB" as example*





≈ 1 dB loss by sweeping C1 from 0 to 100 fF

≈ 6 dB loss by sweeping PCB length from 1 to 150 mm



- 802.3ck Table 163-11. **Channel ERL** parameter value

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.01	ns
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	—
Length of the reflection signal	N	3500	UI
Equalizer length associated with reflection signal	N_{bx}	21	UI
Time-gated propagation delay	T_{fx}	0	ns
Tukey window flag	tw	1	—

TX ERL Reference Values – Sensitivity Analysis

- TX dERL sensitivity check (TP0v test fixture with IL = 2.12 dB @ 26.56 GHz)
  - Total 320 cases
  - **Normal case**: by considering ERL variation from Z_p, Z_c, and R_d with valid range
  - **Extreme case**: by considering additional variations of C_p & C_b, which are with extreme high values

Parameters	Value in D2p0	Valid Range	Note	Test Range	
				Normal	Extreme
R_d (Ohm)	50	45 ~ 55	50 +/- 10%	[50 55]	[50 55]
Z_p (mm)	31	12 ~ 31		[12 31]	[12 31]
Z_c (Ohm)	87.5	80 ~ 95	87.5 +/- 10%	[80:2.5:87.5]	[80:2.5:87.5]
C_p (fF)	87	<= 87		87	[**100:25:175**]
C_b (fF)	30	<= 30		30	[**50:25:100**]

	Min dERL
Normal	-2.13
Extreme	-5.19

- R_d = single-ended termination resistance
- z_p = transmission line length
- Z_c = transmission line characteristics impedance
- C_p = single-ended package capacitance at package-to-board interface
- C_b = single-ended device bump capacitance

COM Sensitivity Check: Whole Link Analysis

- This experiment aims to show the COM impacts under targeting TX models
  - with TX dERL from -3 to 0
  - both normal & extreme cases are considered
- Rx parameters remain consistent for all test cases
  - COM 3.1 spreadsheet listed in appendix

R_d (Ohm)	C_p (nF)	C_b (nF)	Z_c (Ohm)	Z_p (mm)	ERL	dERL
50.00	0.87	0.30	87.50	12.00	19.37	0.77
50.00	0.87	0.30	87.50	31.00	18.60	0.00
55.00	0.87	0.30	87.50	12.00	18.51	-0.09
50.00	0.87	0.30	85.00	31.00	18.50	-0.10
55.00	0.87	0.30	82.50	12.00	18.42	-0.18
50.00	0.87	0.30	82.50	31.00	18.37	-0.23
50.00	0.87	0.30	80.00	31.00	18.12	-0.48
50.00	1.25	0.30	87.50	31.00	18.01	-0.59
50.00	1.50	0.30	87.50	31.00	17.61	-0.98
50.00	1.75	0.30	87.50	31.00	17.22	-1.38
55.00	0.87	0.30	87.50	31.00	17.04	-1.56
55.00	0.87	0.30	87.50	31.00	17.04	-1.56
55.00	0.87	0.30	85.00	31.00	16.94	-1.66
55.00	0.87	0.30	82.50	31.00	16.76	-1.84
55.00	0.87	0.75	85.00	12.00	16.61	-1.99
50.00	0.87	0.75	87.50	31.00	16.57	-2.03
55.00	0.87	0.30	80.00	31.00	16.47	-2.13
50.00	1.75	0.75	87.50	12.00	15.84	-2.76
55.00	1.25	0.50	85.00	31.00	15.61	-2.99

** Row framed in red is the default case for reference*
** Rows highlighted in yellow is for extreme C_p or C_b cases*

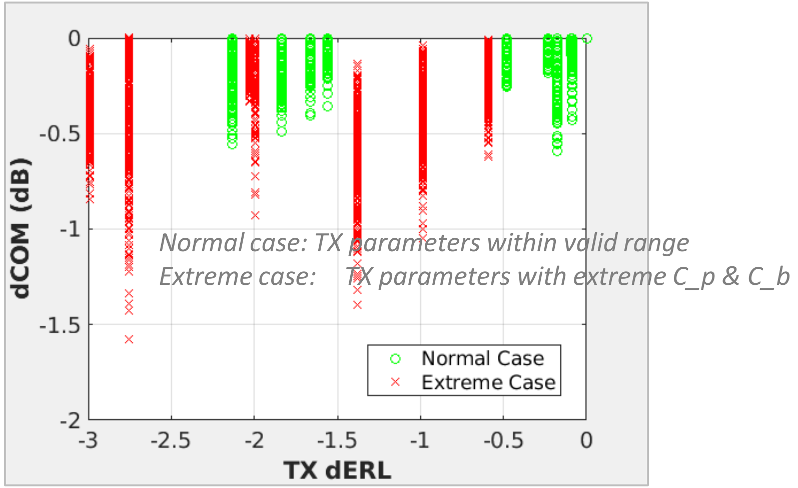
dCOM Sensitivity with TX dERL

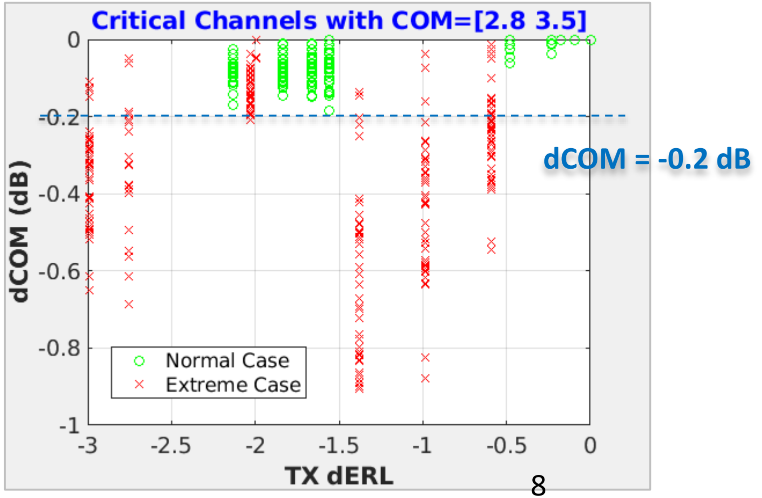
- dCOM = COM - Reference COM (calculated based on the following TX parameters specified in D2p0)

R_d (Ohm)	C_p (nF)	C_b (nF)	Z_c (Ohm)	Z_p (mm)	ERL
50.00	0.87	0.30	87.50	31.00	18.60

- **Normal case**:
  - COM is not sensitive to R_d & Z_c variations
  - For critical channels with COM = [2.8 3.5], COM degradation **<= 0.2 dB**
- **Extreme case**:
  - It's apparently larger C_p & C_b cause worse dERL and hence degrade COM more
  - dCOM > 0.5 dB even we tighten TX dERL specification up to -1 dB

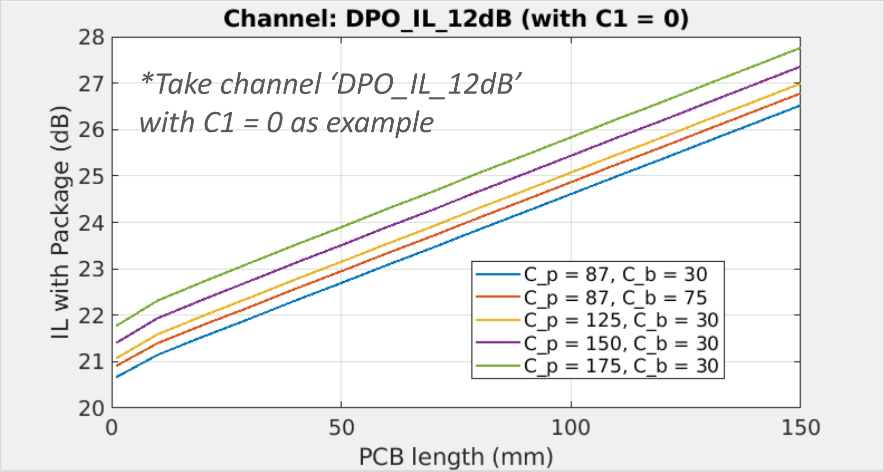
→ ***Is it necessary to allocate dERL margin for C_p & C_b?***

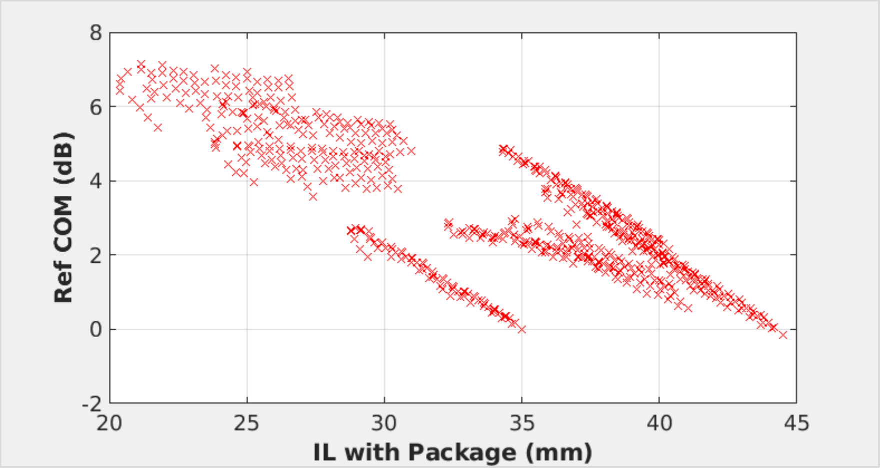




Sensitivity Analysis - IL

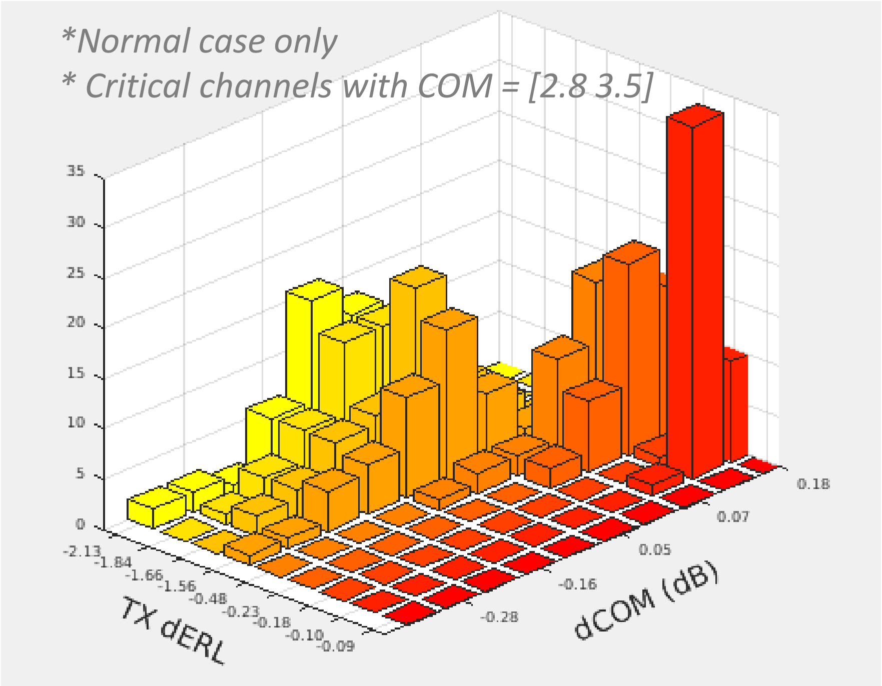
- IL contributed by C_p & C_b
  - IL degradation ≈ **0.25 dB** by C_b = 30 fF → 75 fF
  - IL degradation ≈ **1.21 dB** by C_p = 87 fF → 175 fF
- Correlation between reference COM & IL_wi_pkg
  - Higher IL contributes lower COM





Sensitivity Analysis: dCOM vs TX dERL

- How TX dERL impacts COM?
  - Worse TX dERL → worse dCOM
  - However, COM performs robust under TX dERL up to -2.13 dB
  - dCOM for most of the critical channels falls within -0.2 dB



Summary & Conclusion

- Summary
  - Large values of C_p or C_b will cause serious performance degradation due to additional loss and higher reflection
  - dCOM < 0.2 dB is observed by considering reasonable alternatives of TX parameters, which are with TX dERL up to -2.13 dB
- Keep TX dERL spec = -3 dB

Appendix

COM Spreadsheet for Whole Link Analysis

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]
L_s	[0.12, 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_pselect	[1 2]		[test cases to run]
z_p (TX)	[12 31;1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 29;1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 31;1.8 1.8]	mm	[test cases]
z_p (RX)	[12 29;1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	
A_fe	0.413	V	
A_ne	0.608	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02: 0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	12	UI	
b_max(1)	0.85		
b_max(2..N_b)	[0.3 0.2*ones(1,10)]		
b_min(1)	0.3		
b_min(2..N_b)	[0.05 -0.03*ones(1,10)]		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	8	dB
DER_0	0.0001	
T_r	0.0075	ns
FORCE_TR	1	logical
Local Search	2	
BREAD_CRUMBS	1	logical
SAVE_CONFIG2MAT	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3500	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0]	[port1 port2]
TDR_W_TXPKG	0	
N_bx	21	UI
Tukey_Window	1	logical
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a	[0 0.0009909 0.0002772]	
package_tl_tau	0.006141	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
Table 92–12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	5.790E-03	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	110.3	mm
z_bp (NEXT)	110.3	mm
z_bp (FEXT)	110.3	mm
z_bp (RX)	110.3	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	0	logical
Floating Tap Control		
N_bg	3	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	40	UI span for floating taps
bmaxg	0.05	max DFE value for floating taps
B_float_RSS_MAX	0.02	rss tail tap limit
N_tail_start	25	(UI) start of tail taps limit
ICN parameters		
f_v	0.594	*Fb
f_f	0.594	*Fb
f_n	0.594	*Fb
f_2	40.000	GHz
A_ft	0.600	V
A_nt	0.600	V
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

COM Spreadsheet for TX ERL Analysis

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]
L_s	[0.12, 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 31;1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0;0 0]	mm	[test cases]
z_p (FEXT)	[0 0;0 0]	mm	[test cases]
z_p (RX)	[12 29;1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	
A_fe	0.413	V	
A_ne	0.608	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02: 0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	12	UI	
b_max(1)	0.85		
b_max(2..N_b)	[0.3 0.2*ones(1,10)]		
b_min(1)	0.3		
b_min(2..N_b)	[0.05 -0.03*ones(1,10)]		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 2 3 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTIO	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	8	dB
DER_0	0.0001	
T_r	0.0075	ns
FORCE_TR	1	logical
Local Search	2	
BREAD_CRUMBS	1	logical
SAVE_CONFIG2MA	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	1	logical
TR_TDR	0.01	ns
N	200	
beta_x	0	
rho_x	0.618	
fixture delay time	[2.158e-9 2.158e-9]	[port1 port2]
TDR_W_TXPKG	1	
N_bx	21	UI
Tukey_Window	1	logical
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a	[0 0.0009909 0.0002772]	
package_tl_tau	0.006141	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
Table 92–12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	*[0 3.8206e-04 9.5909e-05]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*110.3*	mm
z_bp (NEXT)	*110.3*	mm
z_bp (FEXT)	*110.3*	mm
z_bp (RX)	*110.3*	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	**0**	**logical**
Floating Tap Control		
N_bg	3	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	40	UI span for floating taps
bmaxg	0.05	max DFE value for floating taps
B_float_RSS_MAX	0.02	rss tail tap limit
N_tail_start	25	(UI) start of tail taps limit
ICN parameters		
f_v	0.594	*Fb
f_f	0.594	*Fb
f_n	0.594	*Fb
f_2	40.000	GHz
A_ft	0.600	V
A_nt	**0.600**	V
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

TX ERL Reference Values – Extreme Case

- dERL calculated with the following device parameters
  - Total 320 test cases

Parameters	Value in D2p0	Test range
R_d (Ohm)	50	[50 55]
z_p (mm)	31	[12 31]
Z_c (Ohm)	87.5	[80:2.5:87.5]
C_p (fF)	87	[87 100:25:175]
C_b (fF)	30	[30 50:25:100]

- R_d = single-ended termination resistance
- z_p = transmission line length
- Z_c = transmission line characteristics impedance
- C_p = single-ended package capacitance at package-to-board interface
- C_b = single-ended device bump capacitance

R_d (Ohm)	C_p (nF)	C_b (nF)	Z_c (Ohm)	Z_p (mm)	ERL	dERL	
50.00	0.87	0.30	87.50	12.00	19.37	0.77	
50.00	0.87	0.30	87.50	31.00	18.60	0.00	D2p0
50.00	0.87	0.50	85.00	12.00	18.59	-0.01	
50.00	1.25	0.30	80.00	12.00	18.59	-0.01	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	
50.00	0.87	0.50	87.50	31.00	17.64	-0.96	
50.00	0.87	0.75	80.00	12.00	17.64	-0.96	
50.00	1.50	0.30	87.50	31.00	17.61	-0.98	
50.00	0.87	0.75	82.50	12.00	17.58	-1.02	
50.00	1.25	0.50	87.50	12.00	17.57	-1.03	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	
55.00	0.87	0.75	80.00	12.00	16.69	-1.91	
55.00	1.50	0.30	80.00	12.00	16.68	-1.92	
55.00	0.87	0.75	85.00	12.00	16.61	-1.99	
50.00	0.87	1.00	80.00	12.00	16.61	-1.99	
50.00	0.87	0.75	87.50	31.00	16.57	-2.03	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	
50.00	1.75	0.75	85.00	31.00	15.63	-2.96	
50.00	0.87	1.00	87.50	31.00	15.63	-2.97	
55.00	1.25	0.50	85.00	31.00	15.61	-2.99	
55.00	0.87	1.00	85.00	12.00	15.59	-3.01	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	
55.00	1.75	1.00	82.50	31.00	13.57	-5.03	
55.00	1.75	1.00	80.00	31.00	13.41	-5.19	

TX ERL Reference Values - Normal Case

- ERL (C_b = 30 fF, C_p = 87 fF) by sweeping
  - R_d = [50 55] Ohm
  - Z_c = [80:2.5:87] Ohm
  - Z_p = [12 31] mm

Parameters	Value in D2p0	Valid range	Note
R_d (Ohm)	50	45 ~ 55	50 +/- 10%
z_p (mm)	31	12 ~ 31	
Z_c (Ohm)	87.5	80 ~ 95	87.5 +/- 10%
C_p (fF)	87	<= 87	
C_b (fF)	30	<= 30	

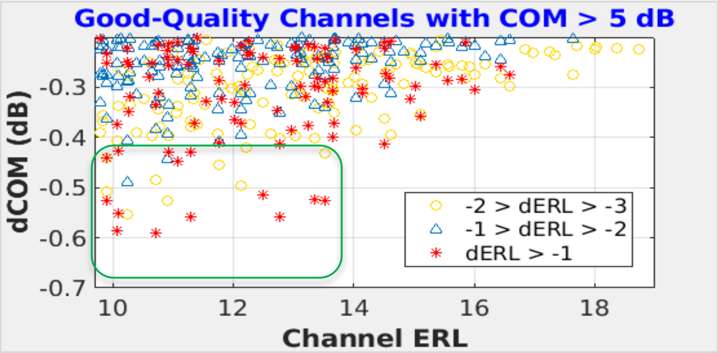
R_d (Ohm)	Z_c (Ohm)	Z_p (mm)	ERL	dERL
50.00	87.50	12.00	19.37	0.77
50.00	87.50	31.00	18.60	0.00
50.00	85.00	31.00	18.50	-0.10
50.00	82.50	31.00	18.37	-0.23
50.00	80.00	31.00	18.12	-0.48
55.00	87.50	31.00	17.04	-1.56
55.00	85.00	31.00	16.94	-1.66
55.00	82.50	31.00	16.76	-1.84
55.00	80.00	31.00	16.47	-2.13

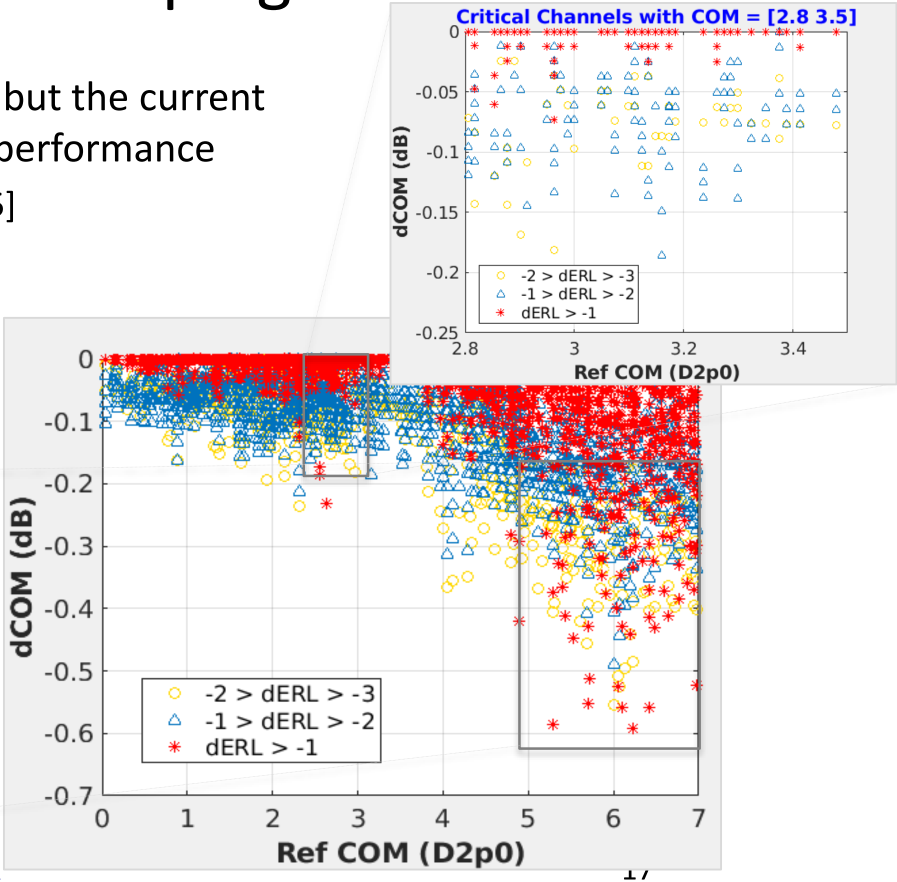
D2p0

TX device model that contributes the worst ERL (within the valid range of TX parameters)

Is Tighter TX dERL Specification Helping?

- For critical channels, tighter TX dERL does help, but the current criterion can already guarantee the acceptable performance
  - dCOM > -0.2 dB for channels with COM = [2.8 3.5]
- For good-quality channels, tighter TX dERL spec makes appreciably less gain
  - For shorter channels, lower channel ERL degrades dCOM





Whole Link Sensitivity Analysis – CH ERL & IL_wi_pkg

- The worst dCOM can be further improved by channel ERL
  - For shorter channels, channel ERL dominates whole link performance

**Those instances are within low IL region*