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The effect of adding noise and restricting DFE tap weights on TP1a measurements for 100GAUI-1 chip to module

Mike Dudek

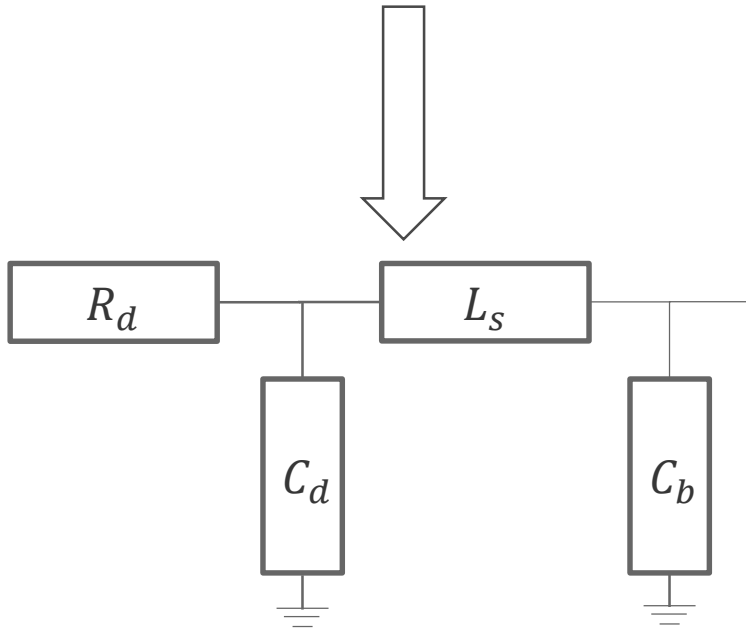
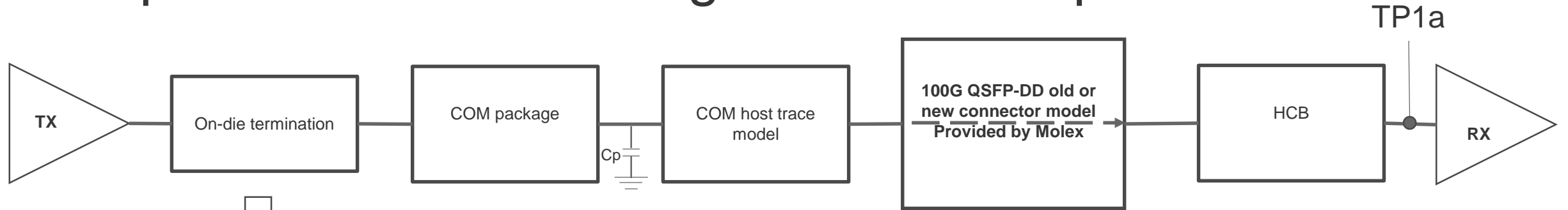
Tao Hu

3/3/2020 Presented at March 4 ad hoc.

Introduction

- This work continues the work presented in Dudek_3ck_01_0719, Dudek_3ck_01_0919, Dudek_3ck_01_01119 and Dudek_3ck-01-0120.
- This presentation explores the effect of adding noise and restricting tap weights on the TP1a measurements.
- It proposes values for these added noise, tap weight restrictions and the related pass/fail criterion for VEC and VEO.

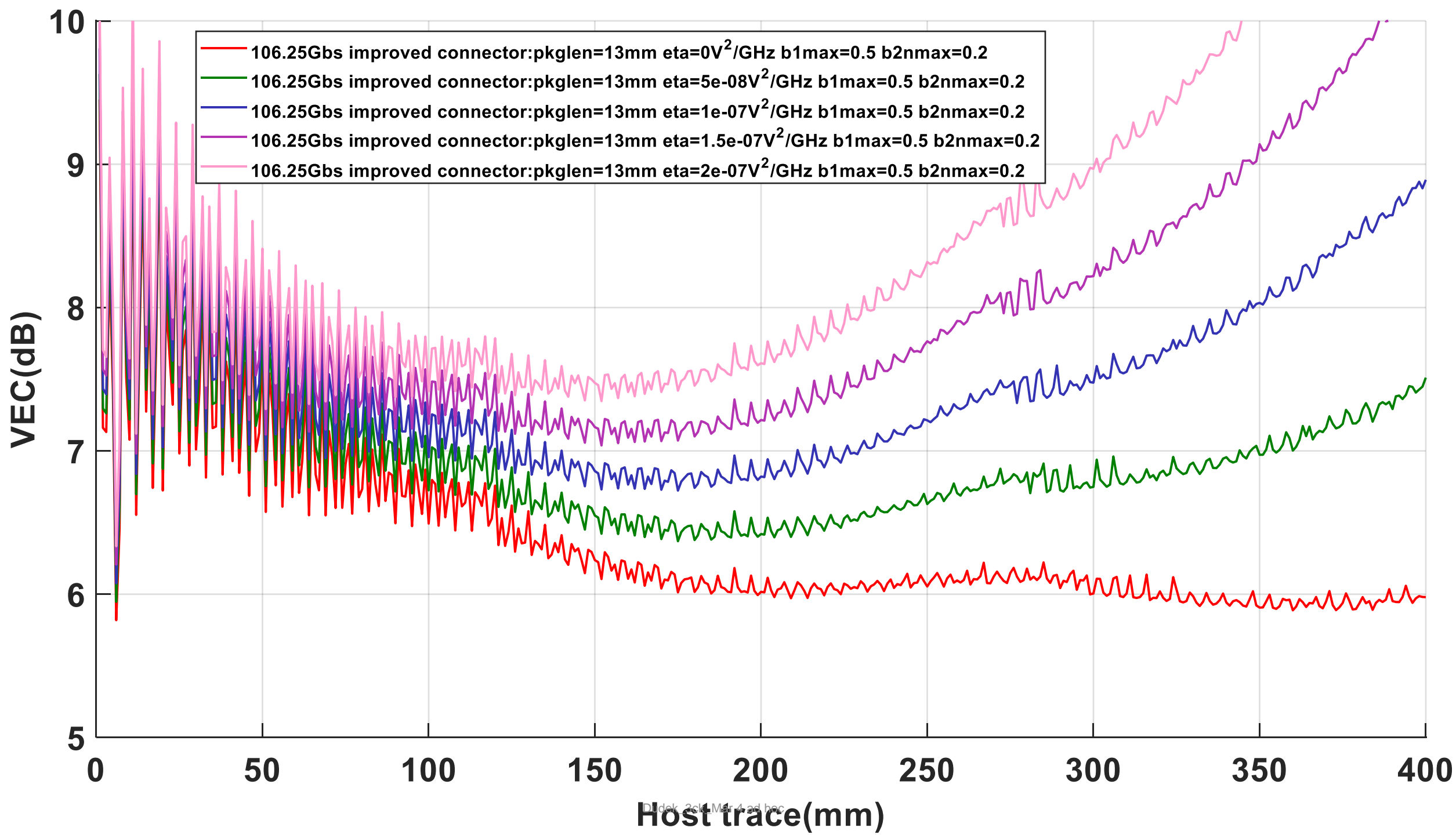
Chip to module block diagram for TP1a performance

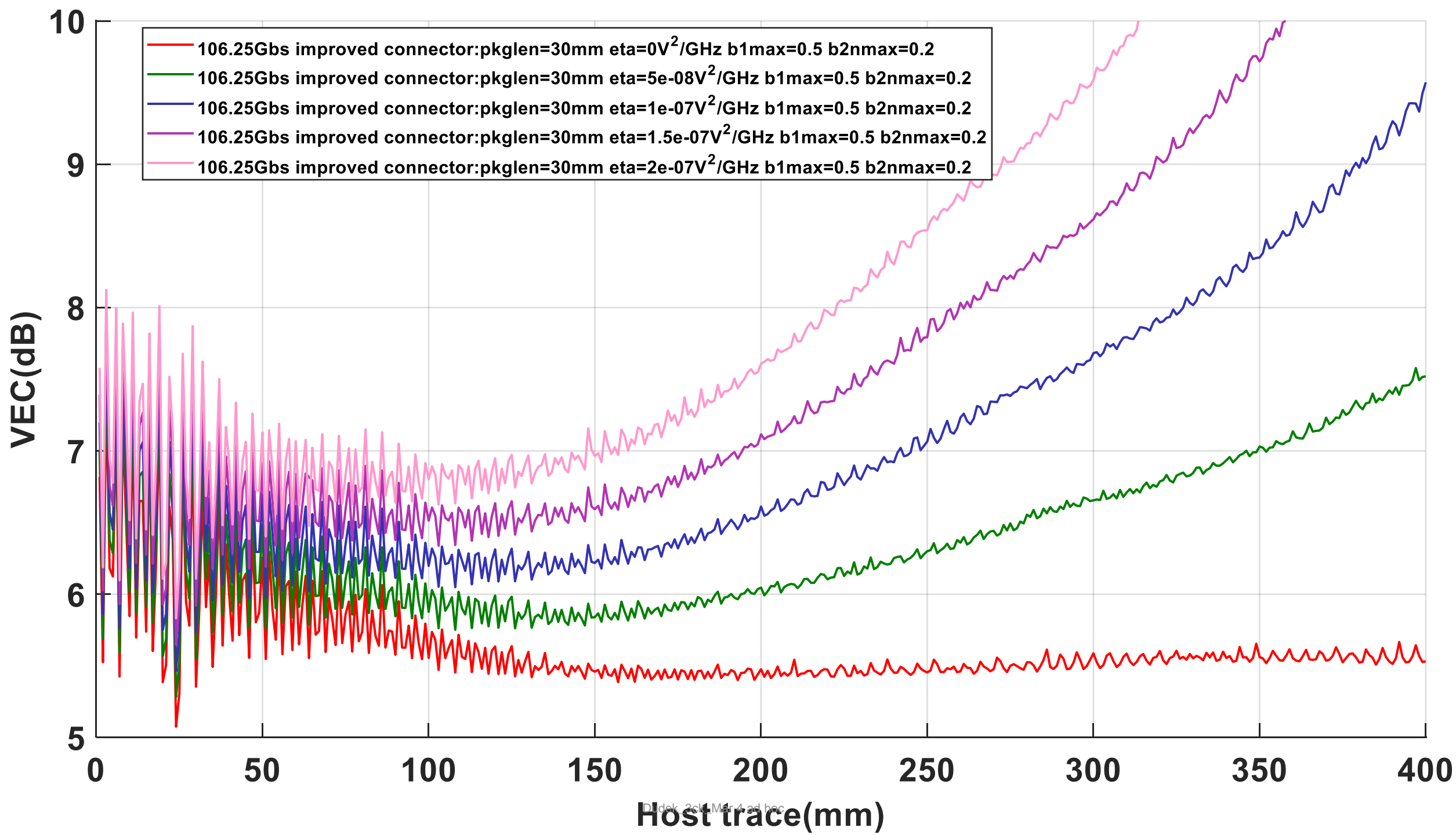


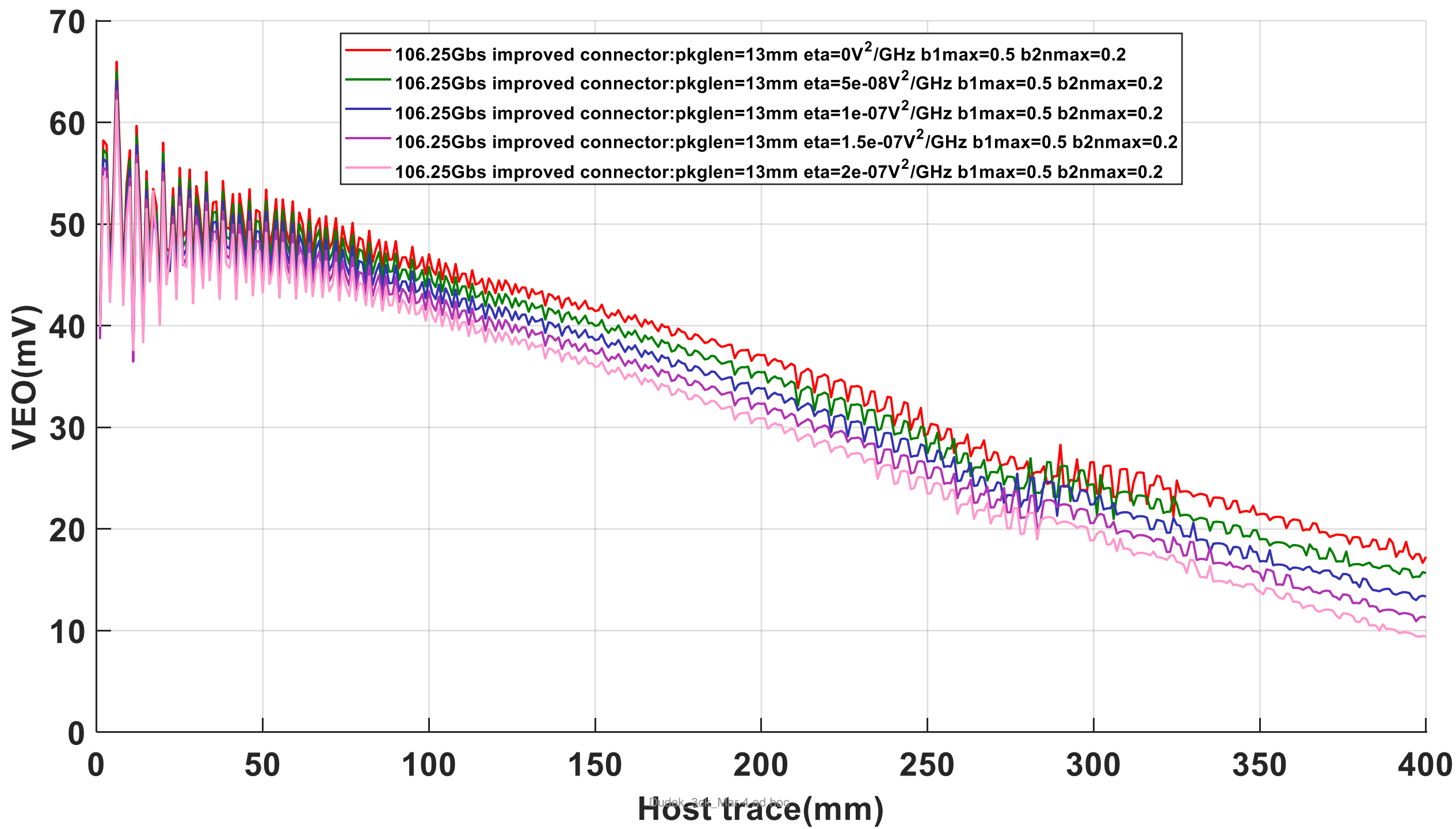
On-die inductor termination

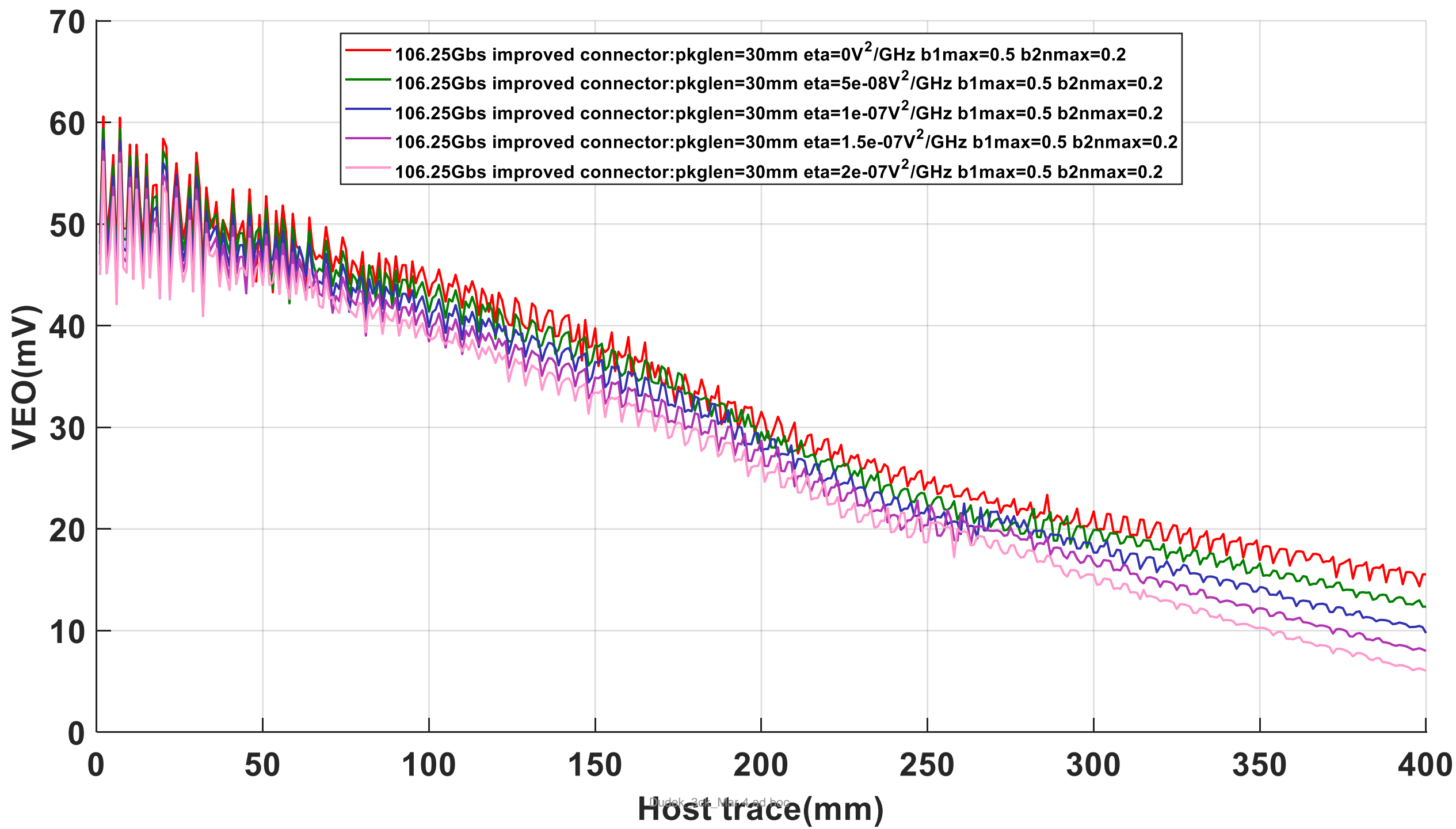
- HCB trace: 100ohm 63.8mm (2.5dB loss) (from COM model)
- TX/RX termination R_d : 50ohm
- Package trace length:
 - 11.5mm (old connector)
 - 13mm (improved connector)
- Host die model:
 - $L_s=120\text{pH}$, $C_d=120\text{fF}$, $C_b=30\text{fF}$
- Sweep host trace length
- Host trace impedance: 100ohm
- A_v : 0.415V A_{ne} : 0.6V A_{fe} : 0.415V
- Crosstalk is not included.
- Lane 3 is used for the simulations
- $\text{Eta}_0=[0, 5e-8, 1e-7, 1.5e-7, 2e-7]\text{V}^2/\text{GHz}$. Note previous work used $8.2e-9\text{V}^2/\text{GHz}$
- TxSNR= 33dB
- Performance is simulated using COM 2.70
- The complete COM table is in the back-up

Effect of added noise at TP1a.





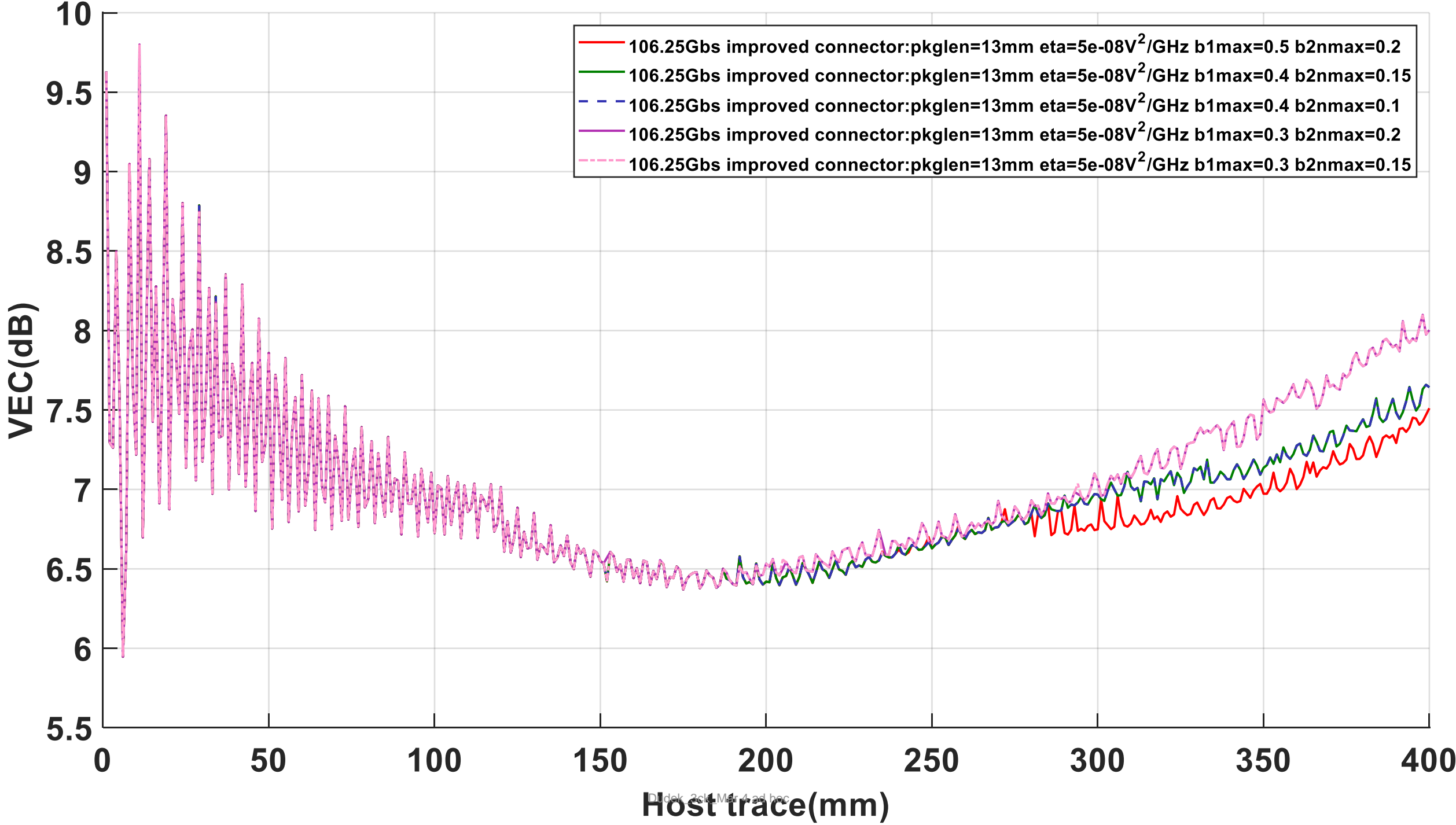


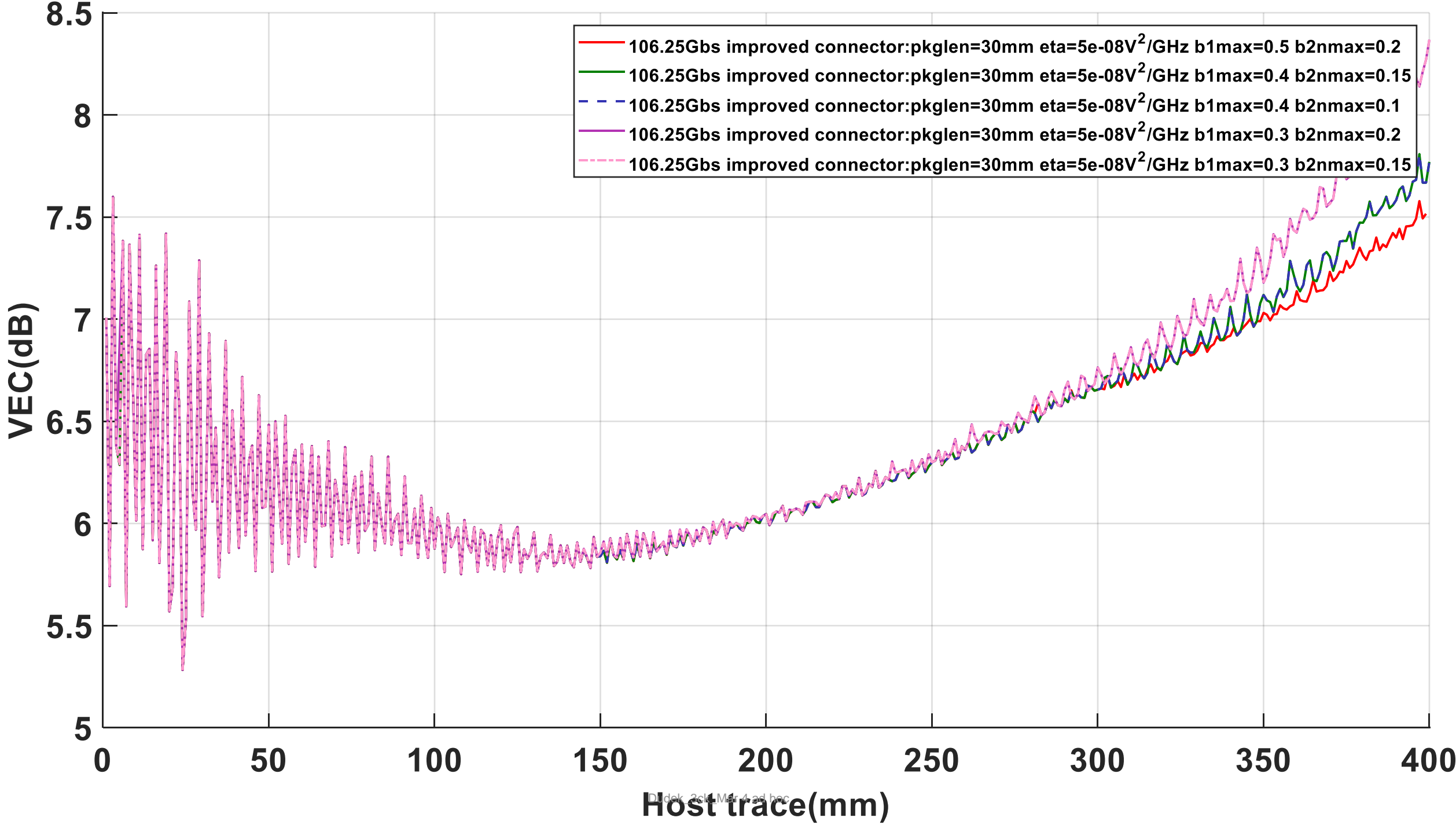


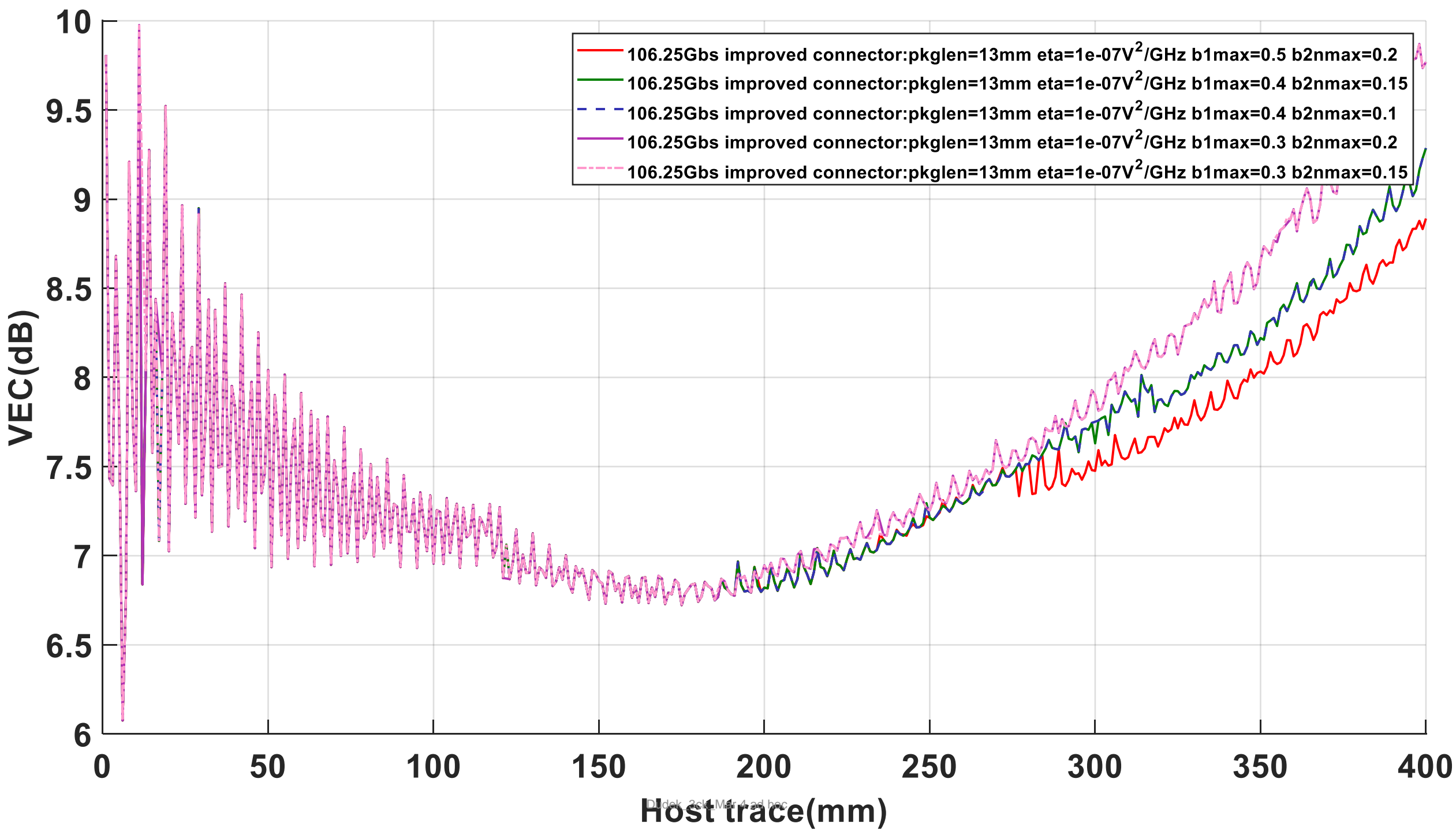
Conclusions on added noise at TP1a.

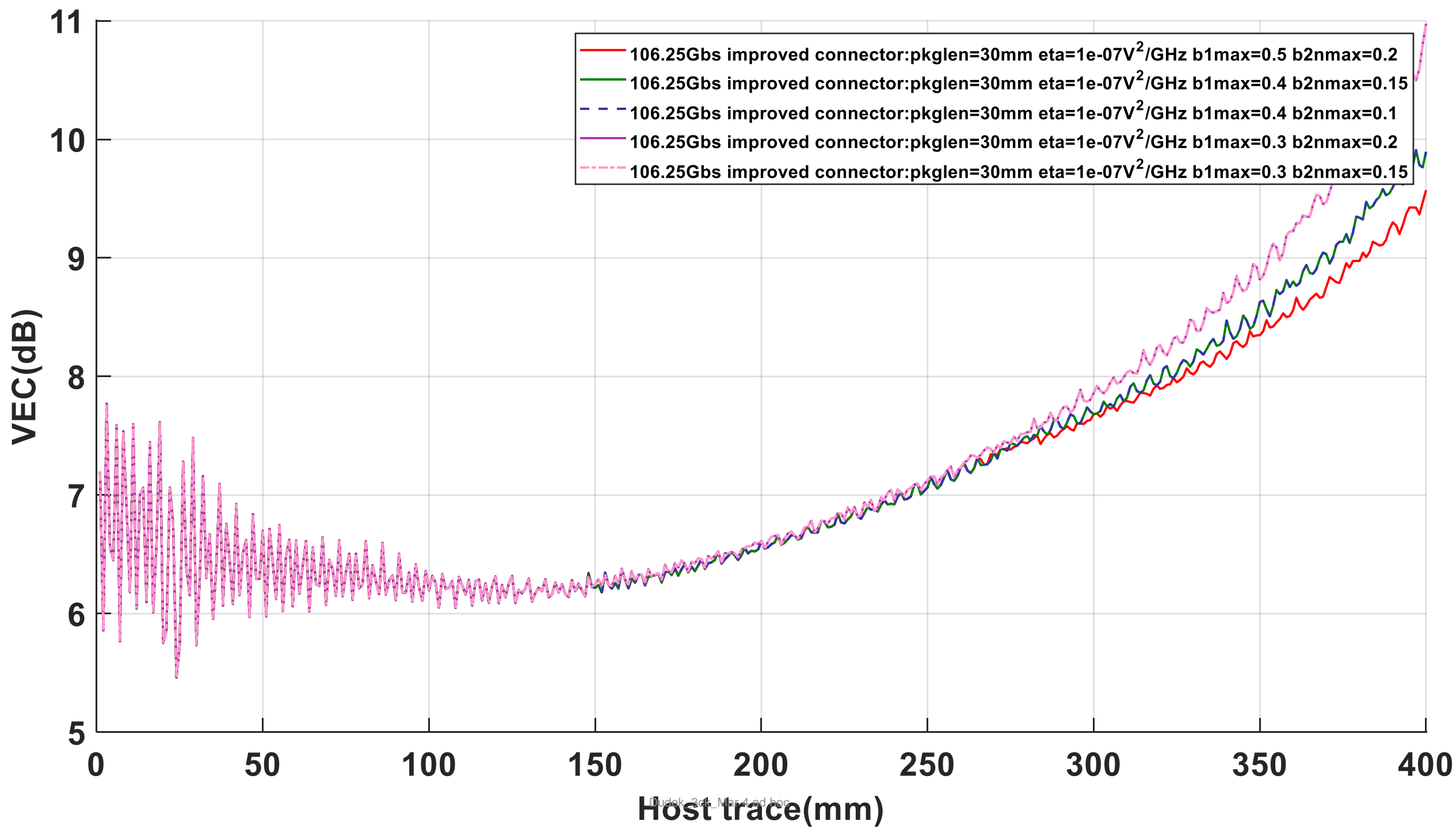
- To allow the 16dB loss channels with the 30mm Tx package to pass without letting the short channels that need a very strong equalizer in the module to pass, the added noise should be Noise spectral density (V^2/GHz): $5e-8$.
- The effect of adding noise to VEO is a general reduction in eye opening that is similar for all channels. With the $5e-8$ value for noise a VEO of 15mV appears to be a good specification value.

Effect of Restricting DFE tap weights at TP1a.

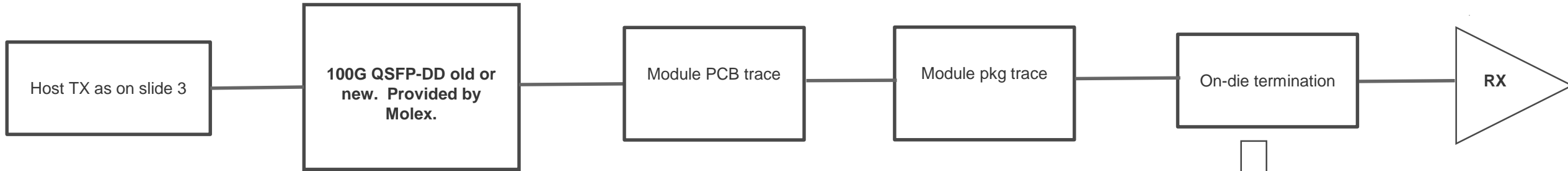




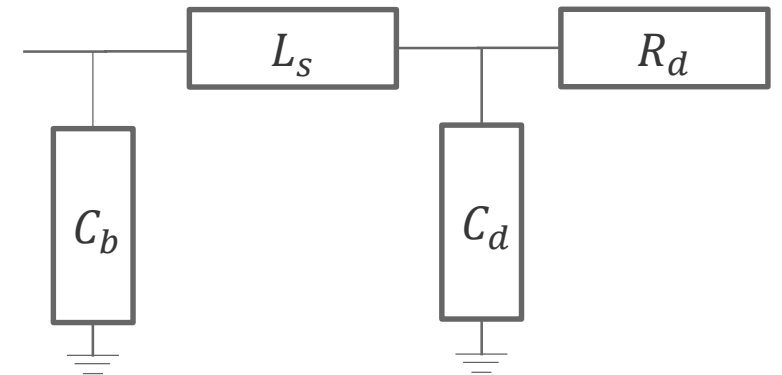




Chip to module block diagram for end to end performance



- RX termination R_d : 50ohm
- Module die/package model $L_s=100\text{pH}$, $C_d=100\text{fF}$, $C_b=30\text{fF}$
- Package Trace 92.5 Ohm, 6mm length
- Sweep module trace length 1-30mm. Trace impedance: 92.5OHM
- Crosstalk is not included.
- Performance is simulated using COM 2.70
- The complete COM table is in the back-up



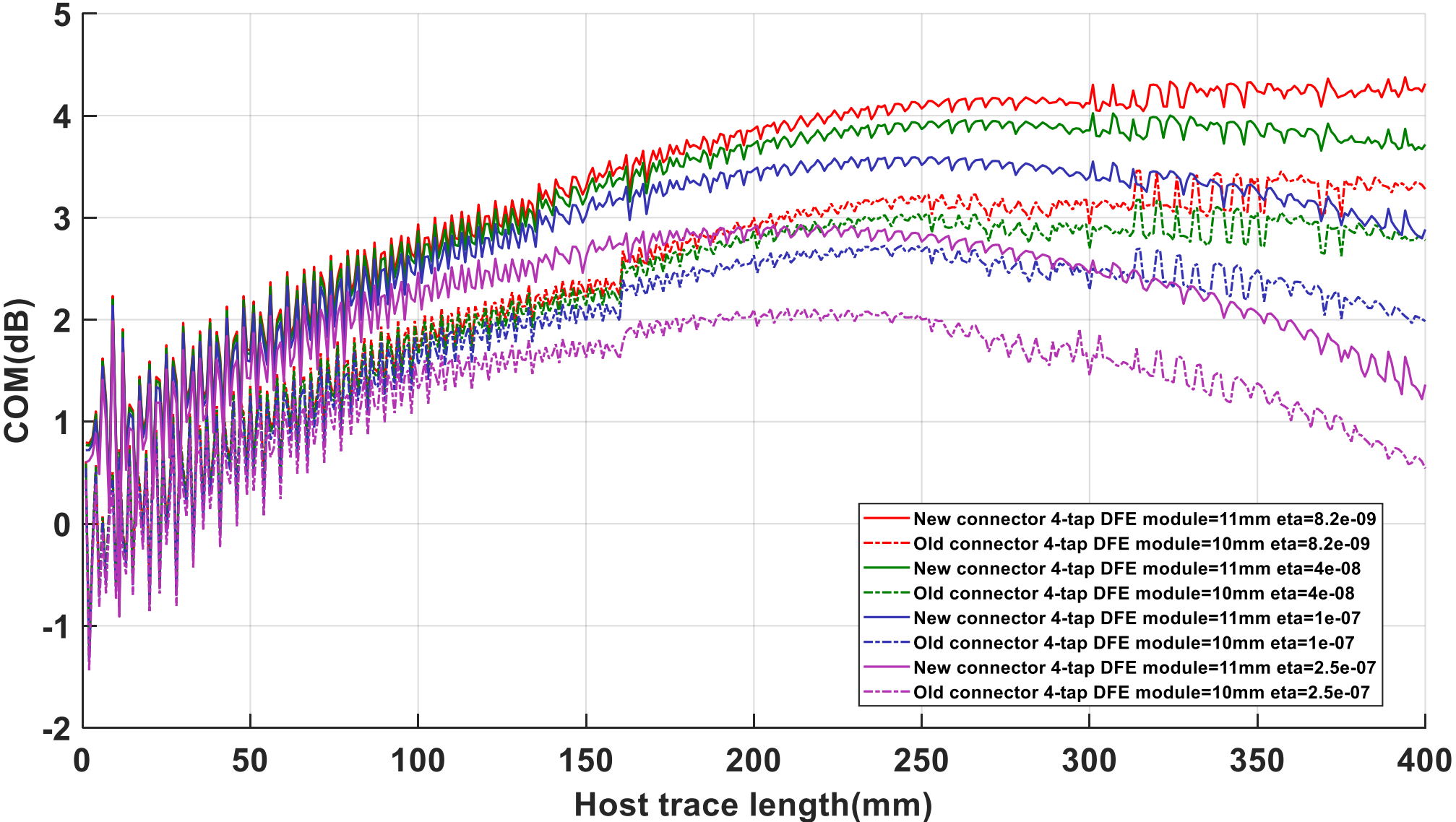
On-die inductor termination

Details of module model.

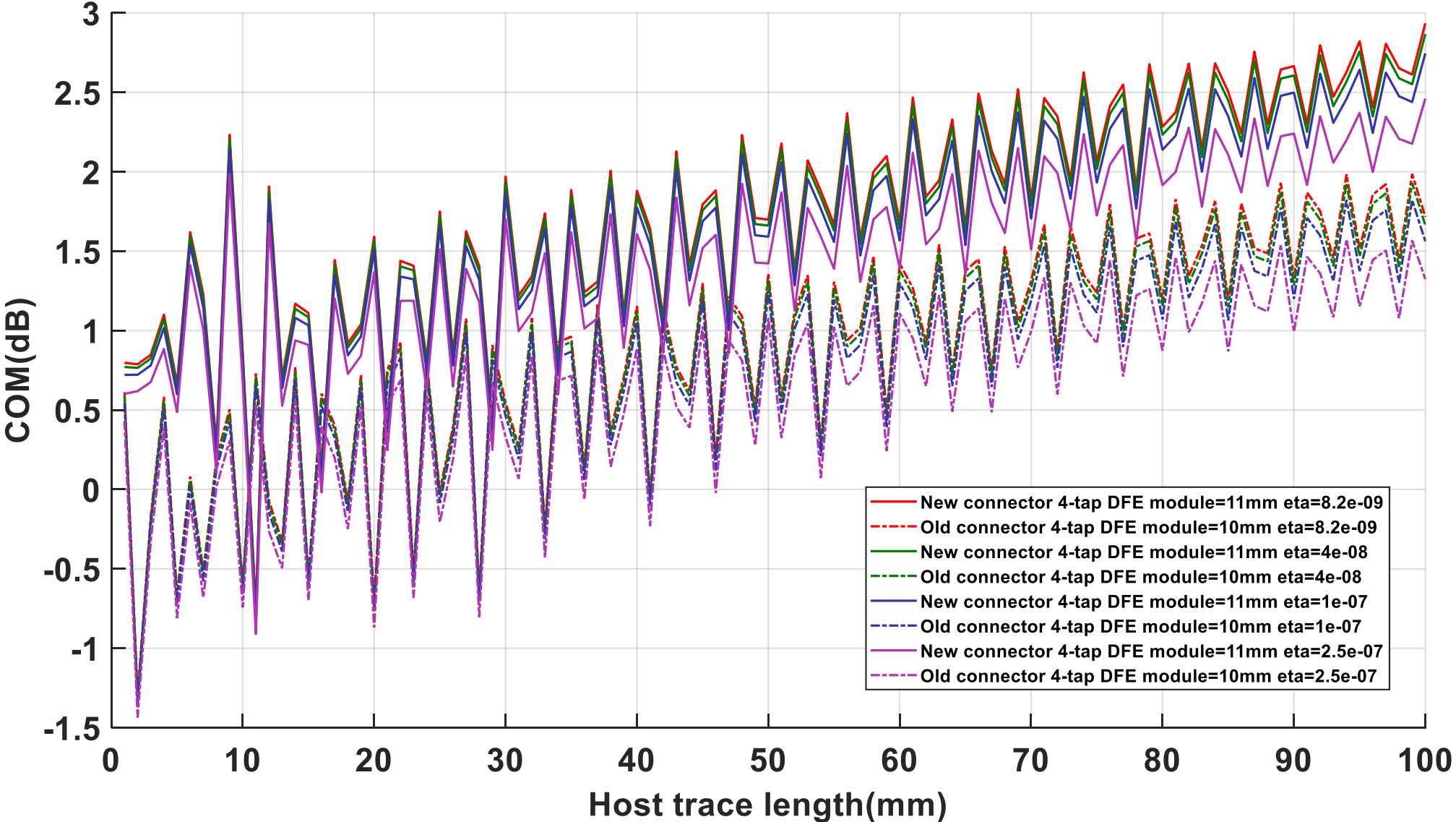
- The following equalizers were used
 - 4 tap DFE
 - 12 tap DFE
 - 10 tap FFE
 - In all cases the Tx FIR was optimized for the VEC at TP1a using the chosen reference equalizer and then the tap weights were frozen for measuring the end to end performance with the various module receivers. (5 tap FFE was not included because previous work had already shown it has inadequate performance.)
- The effect of module IC noise was investigated by varying the value of η_0 . The following values were used.
 - $8.2e-9 \text{ V}^2/\text{GHz}$
 - $4e-8 \text{ V}^2/\text{GHz}$
 - $1e-7 \text{ V}^2/\text{GHz}$
 - $2.5e-7 \text{ V}^2/\text{GHz}$

Module RX: 4-tap DFE

End to end COM (DFE4) examples with approximate worst case module length and TX FIR optimized for 4 tap DFE at TP1a

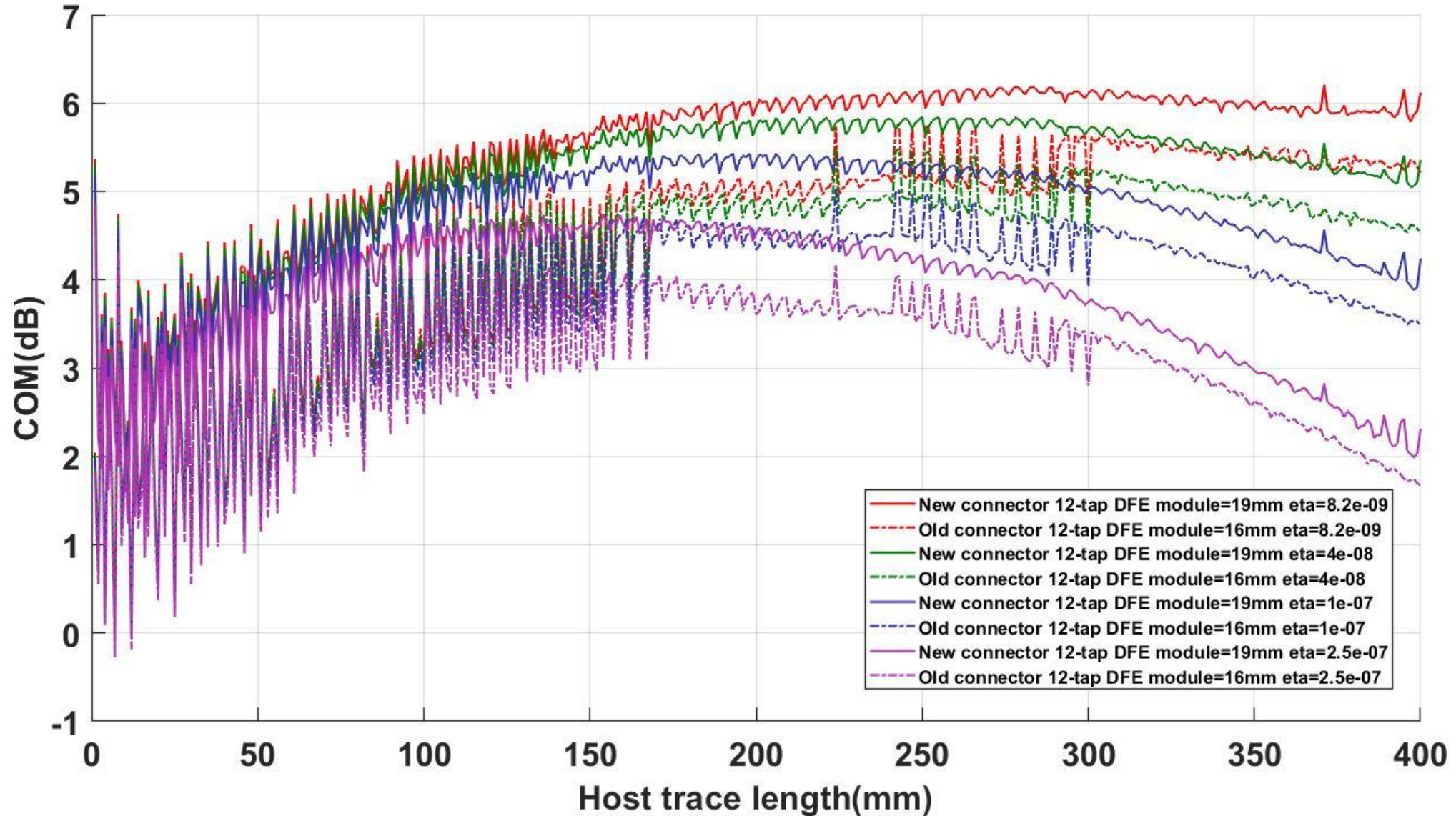


End to end COM examples with approximate worst case module length and TX FIR optimized for 4 tap DFE at TP1a

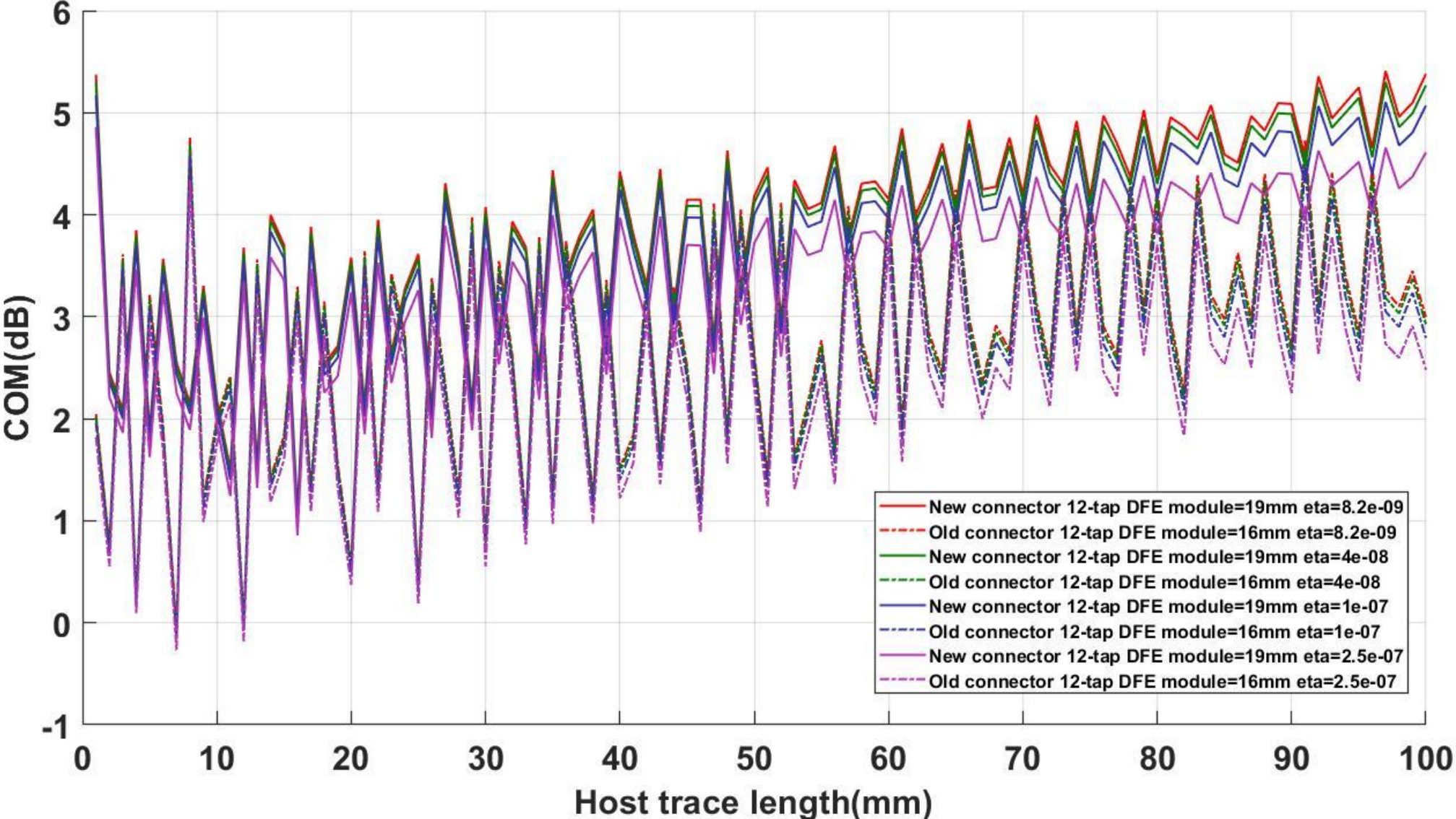


Module RX: 12-tap DFE

End to end COM (DFE12) examples with approximate worst case module length and TX FIR optimized for 4 tap DFE at TP1a

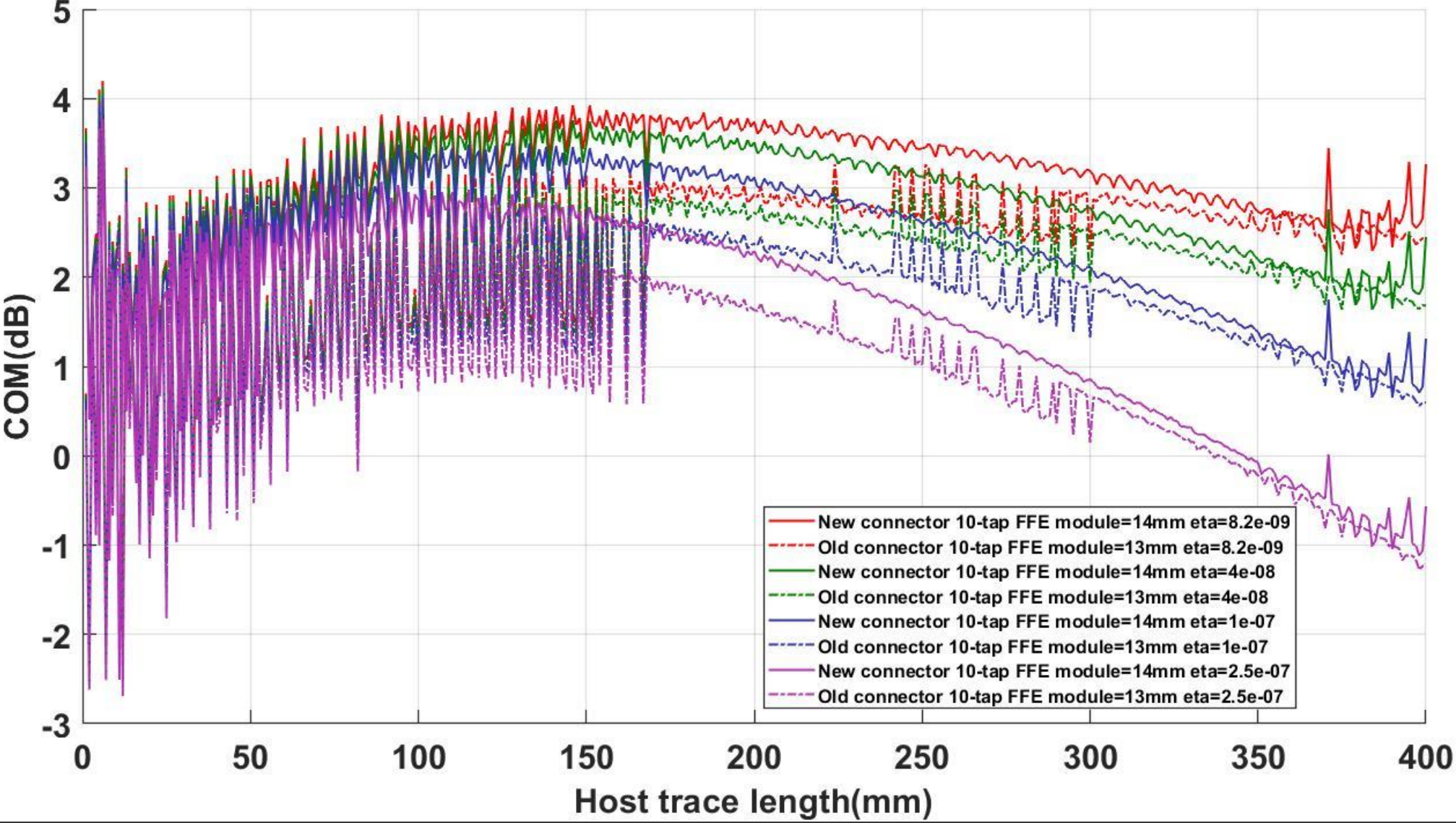


End to end COM (DFE12) examples with approximate worst case module length and TX FIR optimized for 4 tap DFE at TP1a

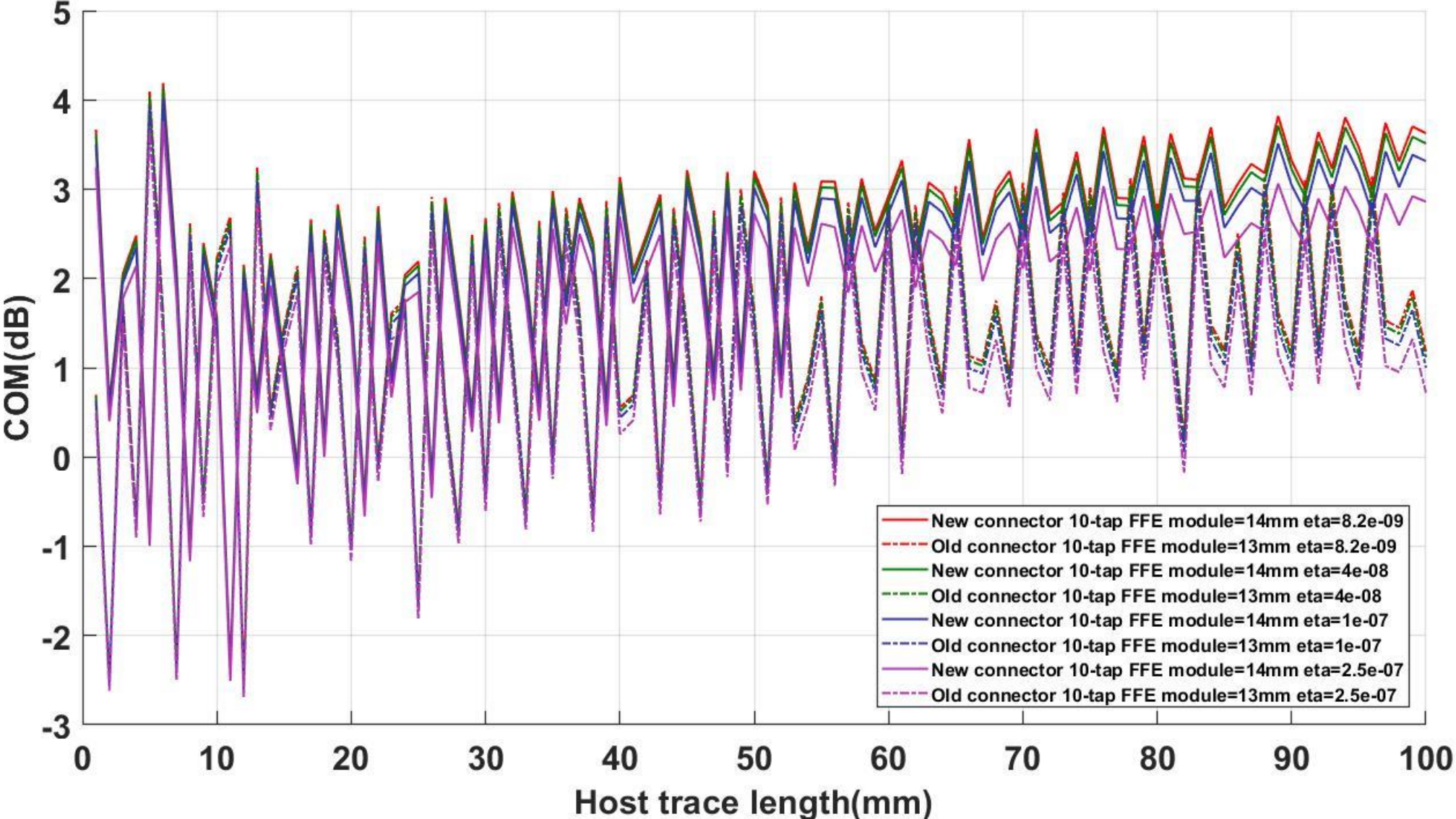


Module RX: 10-tap FFE

End to end COM (FFE10) examples with approximate worst case module length and TX FIR optimized for 4 tap DFE at TP1a



End to end COM (FFE10) examples with approximate worst case module length and TX FIR optimized for 4 tap DFE at TP1a



Conclusions on DFE tap weight restrictions.

- Restricting B2-n at TP1a to 0.1 is not affecting any of these channels, but in case other channels require something larger 0.15 is recommended.
- Restricting B1 at TP1a to less than 0.5 does increase VEC for the longer channels, however the increase is relatively small for B1 max of 0.4 for the channels of interest (<16dB insertion loss).
- All the end to end simulations have b1 limited to 0.5 and bn limited to 0.2. It does not seem likely that significantly larger b1 values are needed in the module than at TP1a.
- It does not appear necessary to restrict b1 to less than 0.5 at TP1a, as these end to end tap weights do not cause excessive error extension, however restricting it to 0.4 would be OK.

Final Conclusions and recommendations.

- The added spectral noise at TP1a should be $5e-8 \text{ V}^2/\text{GHz}$
- The max value of B1 at TP1a should be 0.4
- The max value of Bn at TP1a should be 0.15
- The VEO min value should be 15mV
- With these values the max value of VEC should be 7.5dB to provide adequate performance for the critical 50mm to 160mm host trace lengths where the host could also be used for the CR specification. Note however that there are other impairments that have not been explored in this presentation. In particular the effect of vias and crosstalk in the host.
- The module can work with these hosts by using any or a combination of the following.
 - Not needing a COM of 3dB
 - Using a strong equalizer
 - Having a better IC package
 - Not having a high front end noise.

Back-up

TP1a COM spreadsheet w/ 4-tap DFE RX

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 0]	nF	[TX RX]
L_s	[0.12, 0]	nH	[TX RX]
C_b	[0.3e-4 0]	nF	[TX RX]
z_p_select	[1]		[test cases to run]
z_p (TX)	[13 13; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[13 13; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0; 0 0]	mm	[test cases]
C_p	[0.87e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.415	V	
A_fe	0.415	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.1]		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	4	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-14:1:-3]	dB	[min:step:max]
f_z	12.58	GHz	
f_p1	20	GHz	
f_p2	28	GHz	
g_DC_HP	[-3:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	0	UI	
Include PCB	1	logical	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	0		

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	\\results\100GEL_WG_{date}\	
SAVE_FIGURES	0	logical
Port Order	[13 2 4]	
RUNTAG	C2M_1218	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	0	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	300	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	0.3	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	0.00E+00	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	
TDR_W_TXPKG	1	

Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
Table 92-12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	5.790E-03	ns/mm
board_Z_c	[100 100]	Ohm
z_bp (TX)	7	mm
z_bp (NEXT)	0	mm
z_bp (FEXT)	0	mm
z_bp (RX)	63.8	mm

TX package:

11.5mm for old connector

13mm for improved connector

z_bp(TX):

1 to 400mm w/ step 1mm

End to end COM spreadsheet w/ n-tap DFE RX

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.0e-4]	nF	[TX RX]
L_s	[0.12, 0.1]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	[11.5 11.5; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0.0; 0.0]	mm	[test cases]
z_p (FEXT)	[11.5 11.5; 1.8 1.8]	mm	[test cases]
z_p (RX)	[6.6; 0.0]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.415	V	
A_fe	0.415	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.1]		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	4/7/12	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-14:1:-3]	dB	[min:step:max]
f_z	12.58	GHz	
f_p1	20	GHz	
f_p2	28	GHz	
g_DC_HP	[-3:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	0	UI	
Include PCB	1	logical	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	0		

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	results\100GEL_WG_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_1218	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	0	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	300	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	0.3	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	
TDR_W_TXPKG	1	

Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 92.5 ; 92.5 92.5]	Ohm
Table 92-12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	5.790E-03	ns/mm
board_Z_c	[100 92.5]	Ohm
z_bp (TX)	1:400	mm
z_bp (NEXT)	0	mm
z_bp (FEXT)	0	mm
z_bp (RX)	1:30	mm

TX package:

11.5mm for old connector

13mm for improved connector

z_bp(TX):

1 to 400mm w/ step 1mm

z_bp(RX):

1 to 30mm w/ step 1mm

Eta_0: [8.2e-9 4e-8 1e-7 2.5e-7] V^2/GHz

End to end COM spreadsheet w/ 10-tap FFE

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.0e-4]	nF	[TX RX]
L_s	[0.12, 0.1]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	[13 13; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[00; 00]	mm	[test cases]
z_p (FEXT)	[13 13; 1.8 1.8]	mm	[test cases]
z_p (RX)	[6 6; 0.0]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.415	V	
A_fe	0.415	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.1]		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	0	UI	
b_max(1)	0		
b_max(2..N_b)	0		
g_DC	[-14:1:-3]	dB	[min:step:max]
f_z	18.88	GHz	
f_p1	28	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-3:1:0]		[min:step:max]
f_HP_PZ	0.00025	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	9	UI	
Include PCB	1	logical	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	0		

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	results\100GEL_WG_{date}	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_1218	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	0	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	300	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	0.3	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

TDR_W_TXPKG	1	
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Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.1400E-03	ns/mm
package_Z_c	[87.5 92.5 ; 92.5 92.5]	Ohm
Table 92-12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	5.790E-03	ns/mm
board_Z_c	[100 92.5]	Ohm
z_bp (TX)	41	mm
z_bp (NEXT)	0	mm
z_bp (FEXT)	0	mm
z_bp (RX)	7	mm

TX package:

11.5mm for old connector

13mm for improved connector

z_bp(TX):

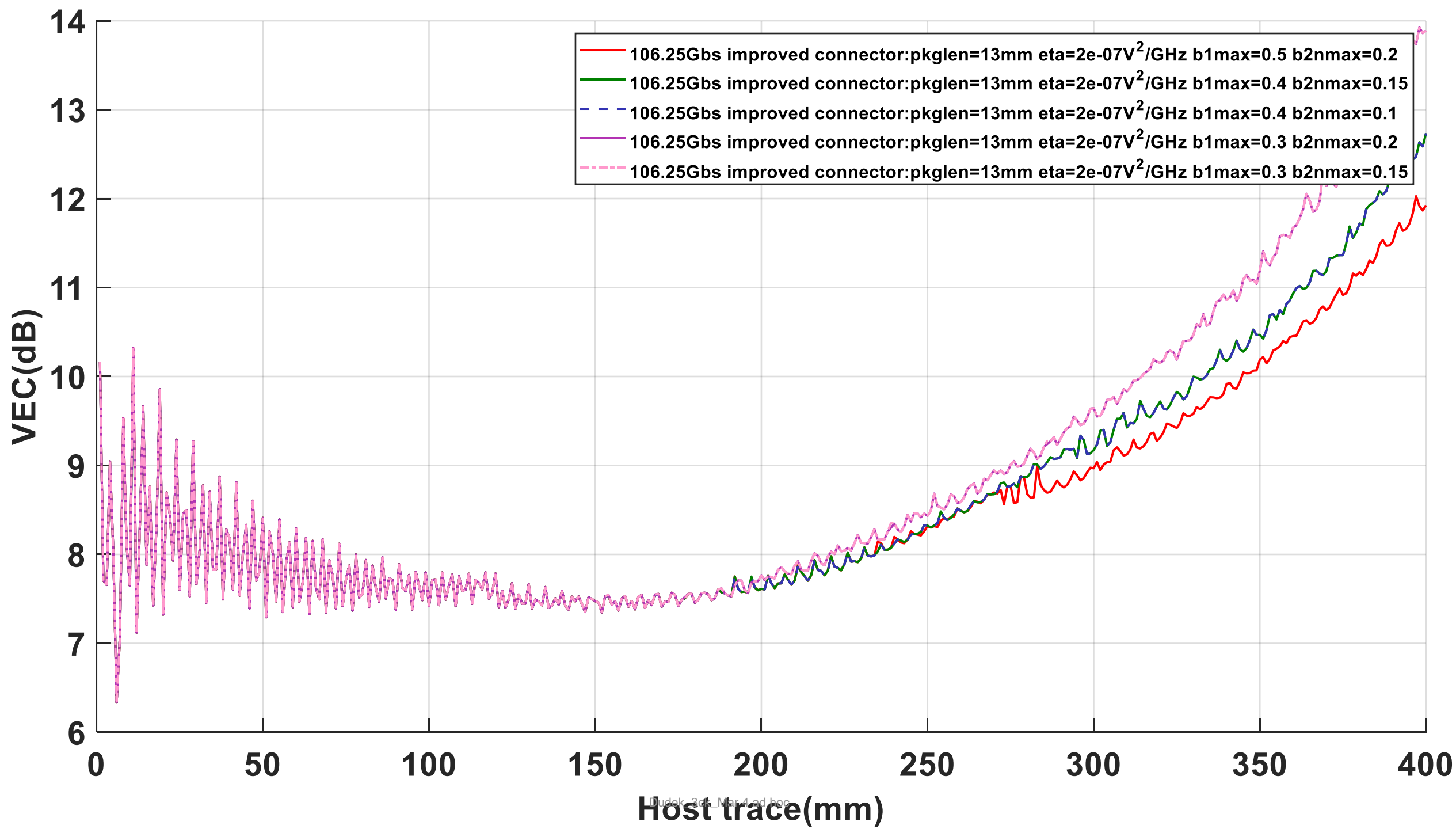
1 to 400mm w/ step 1mm

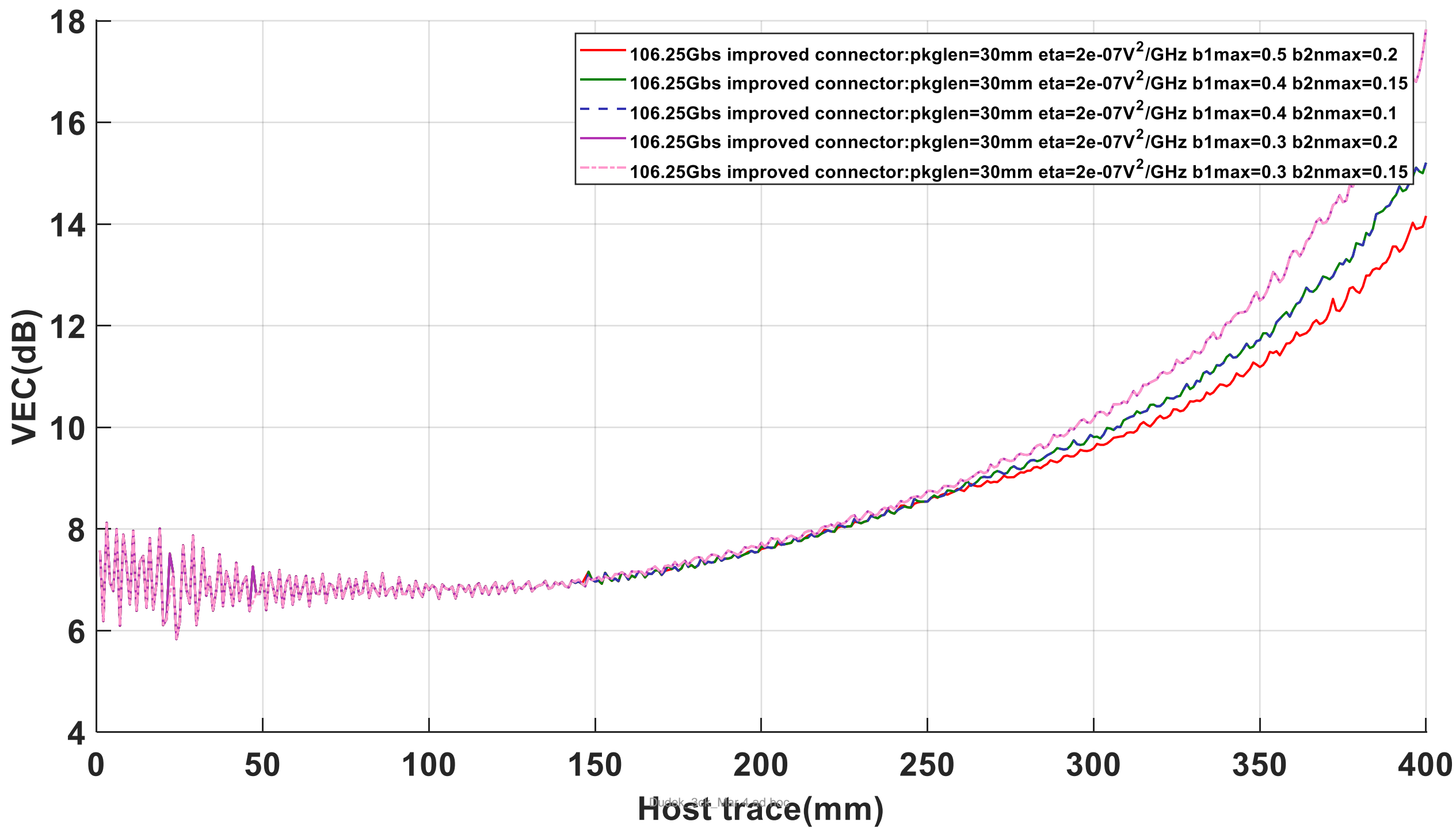
z_bp(RX):

1 to 30mm w/ step 1mm

Eta_0: [8.2e-9 4e-8 1e-7 2.5e-7] V^2/GHz

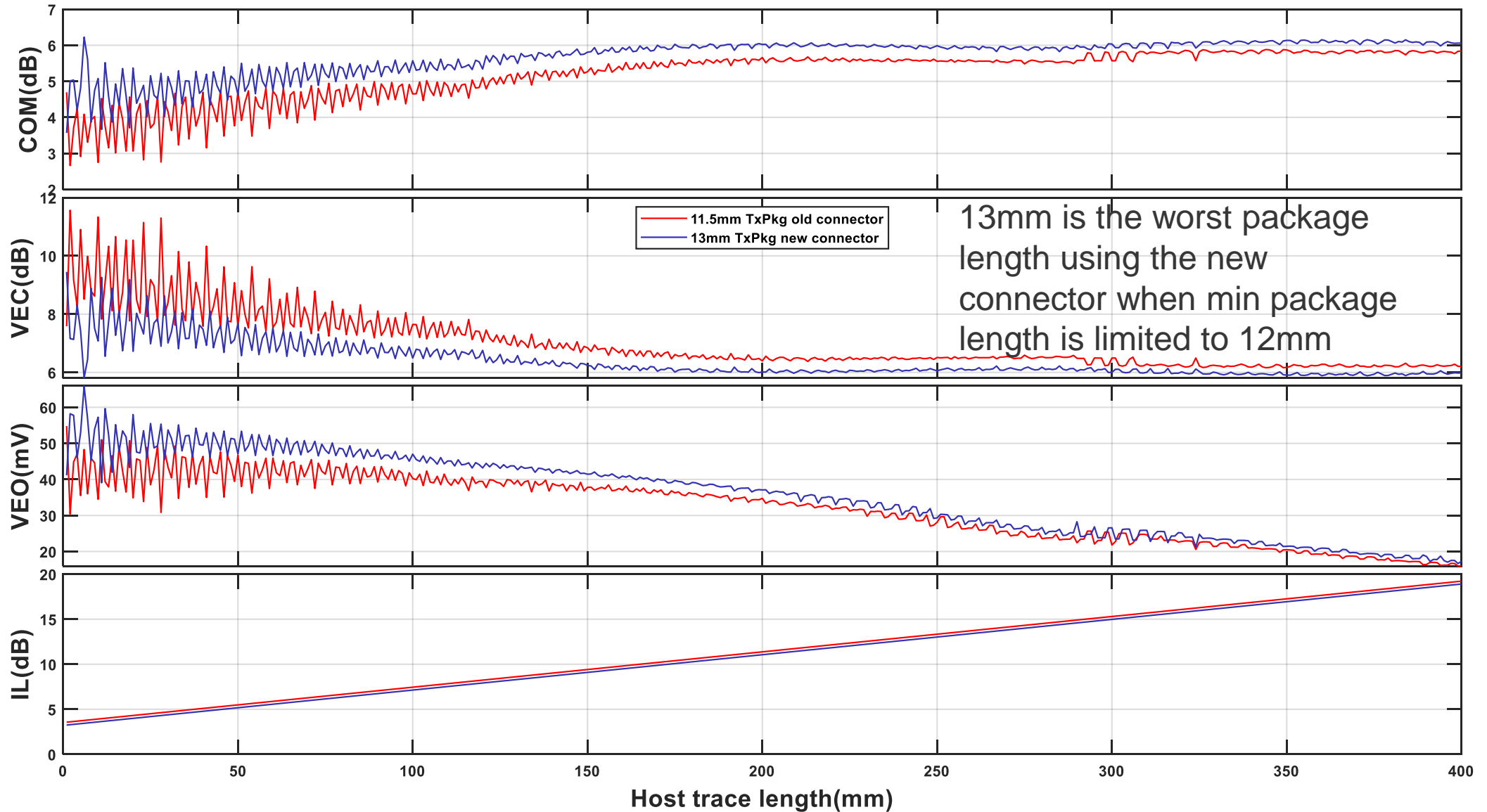
Even higher level of noise

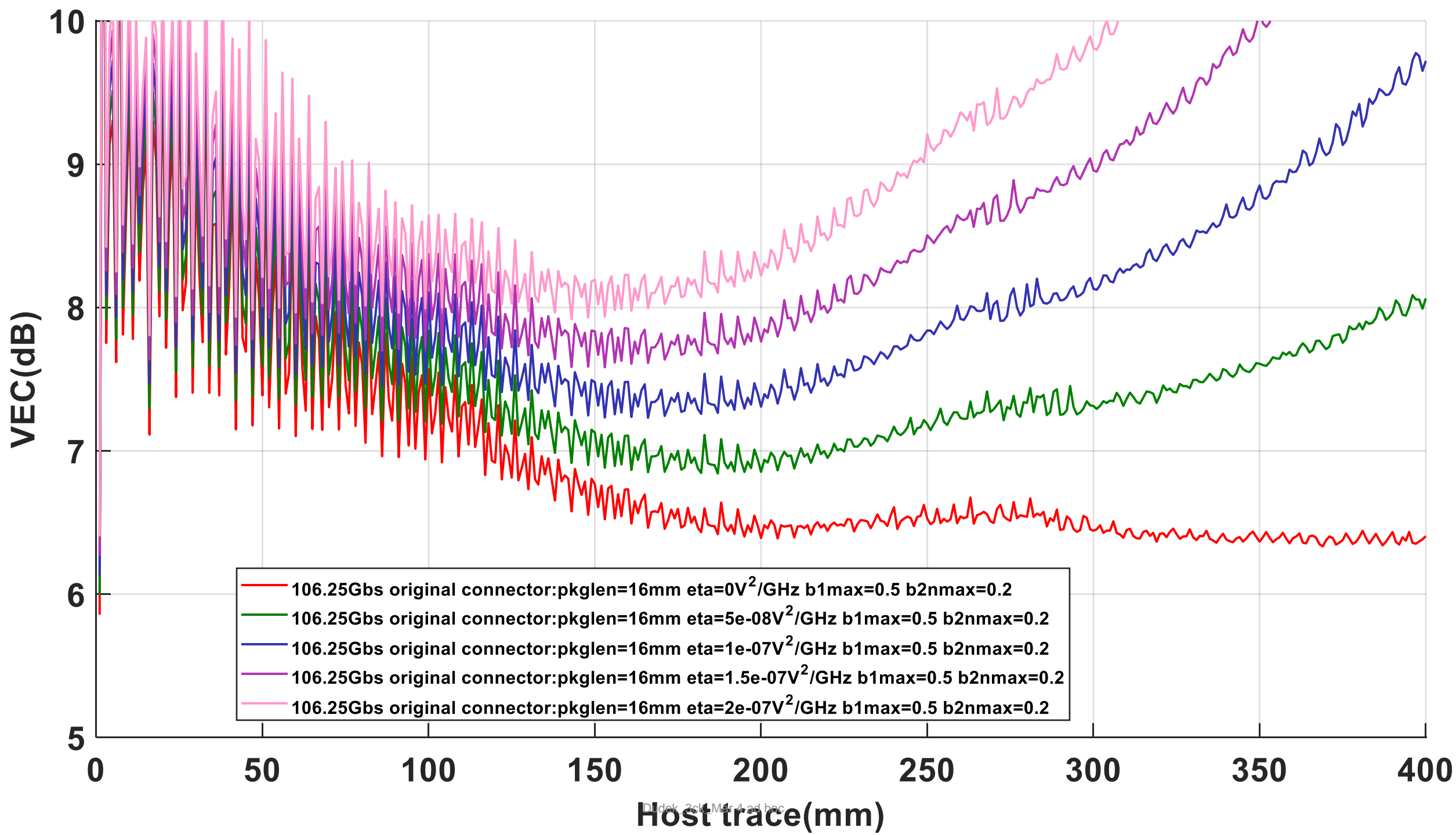


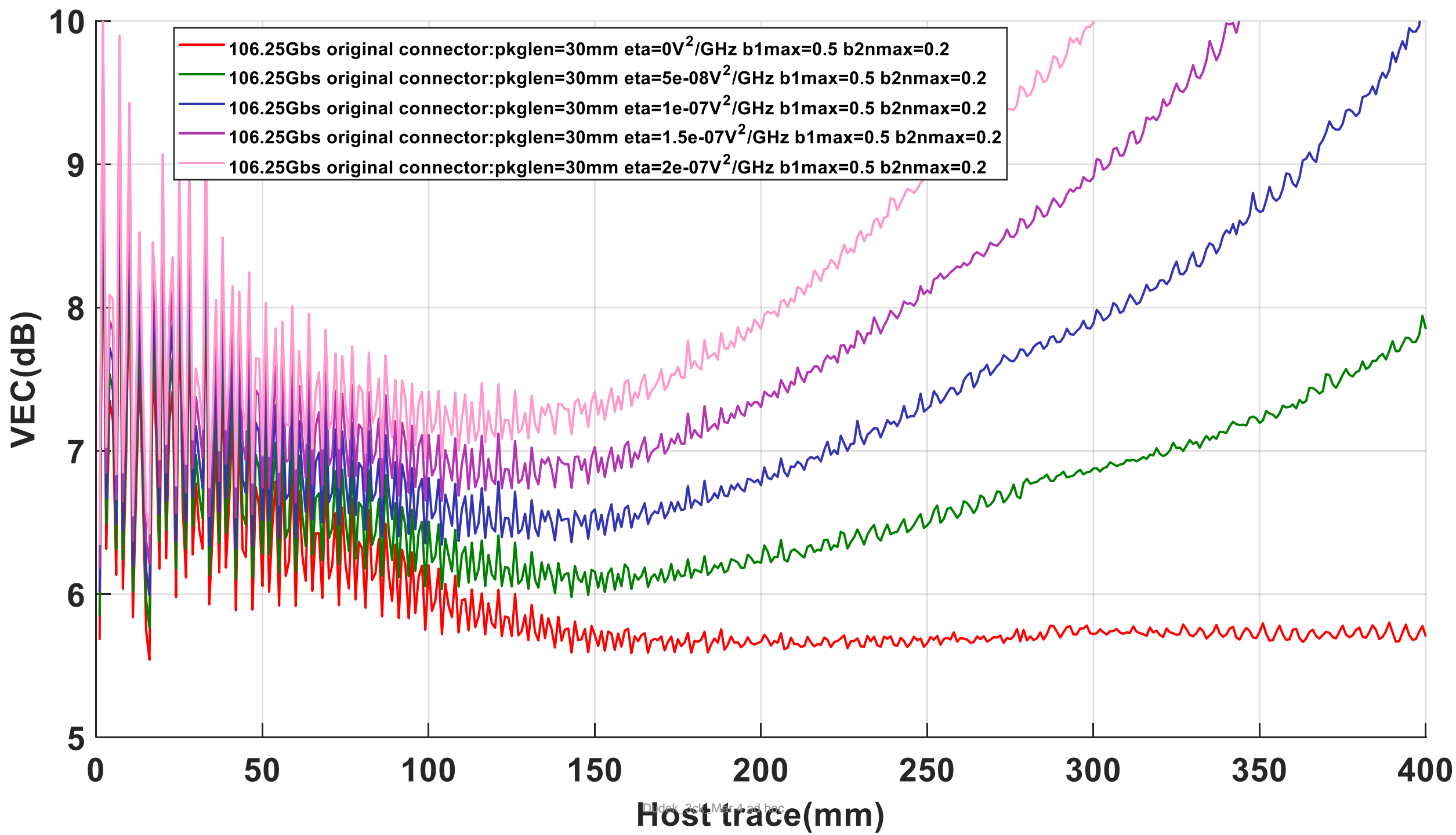


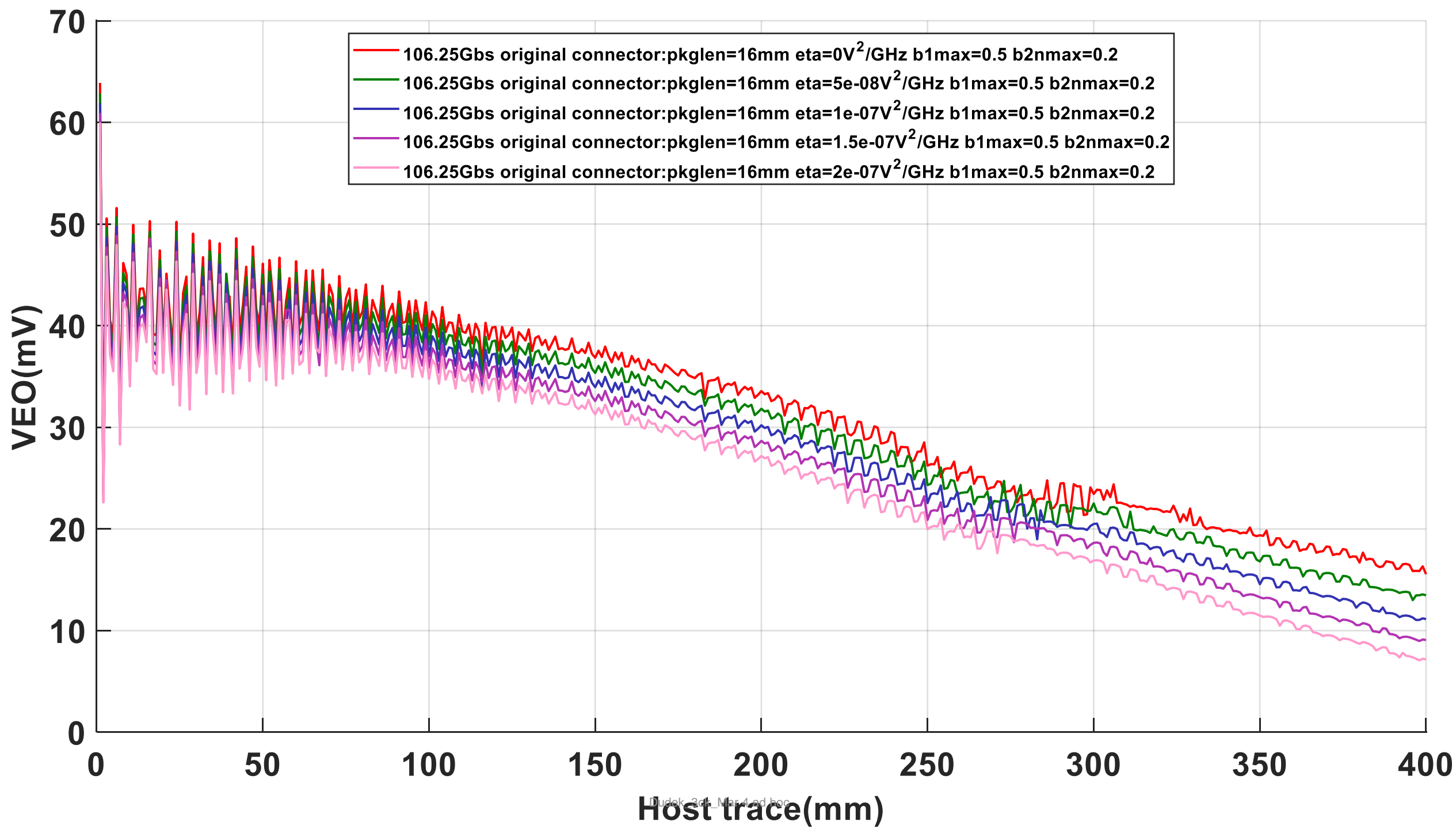
TP1a measurements with old connector

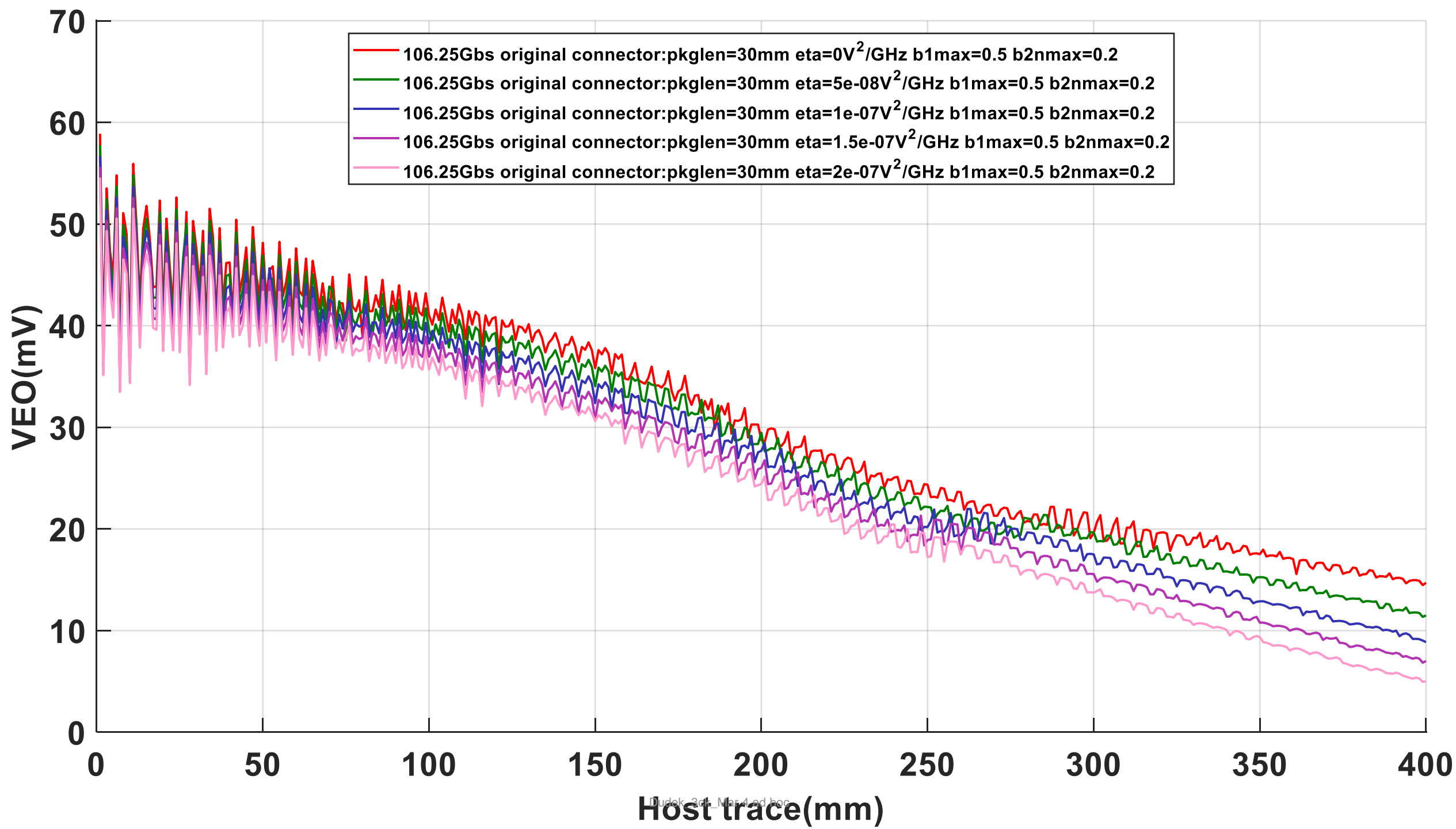
Performance comparison between connectors at TP1a (DFE4)

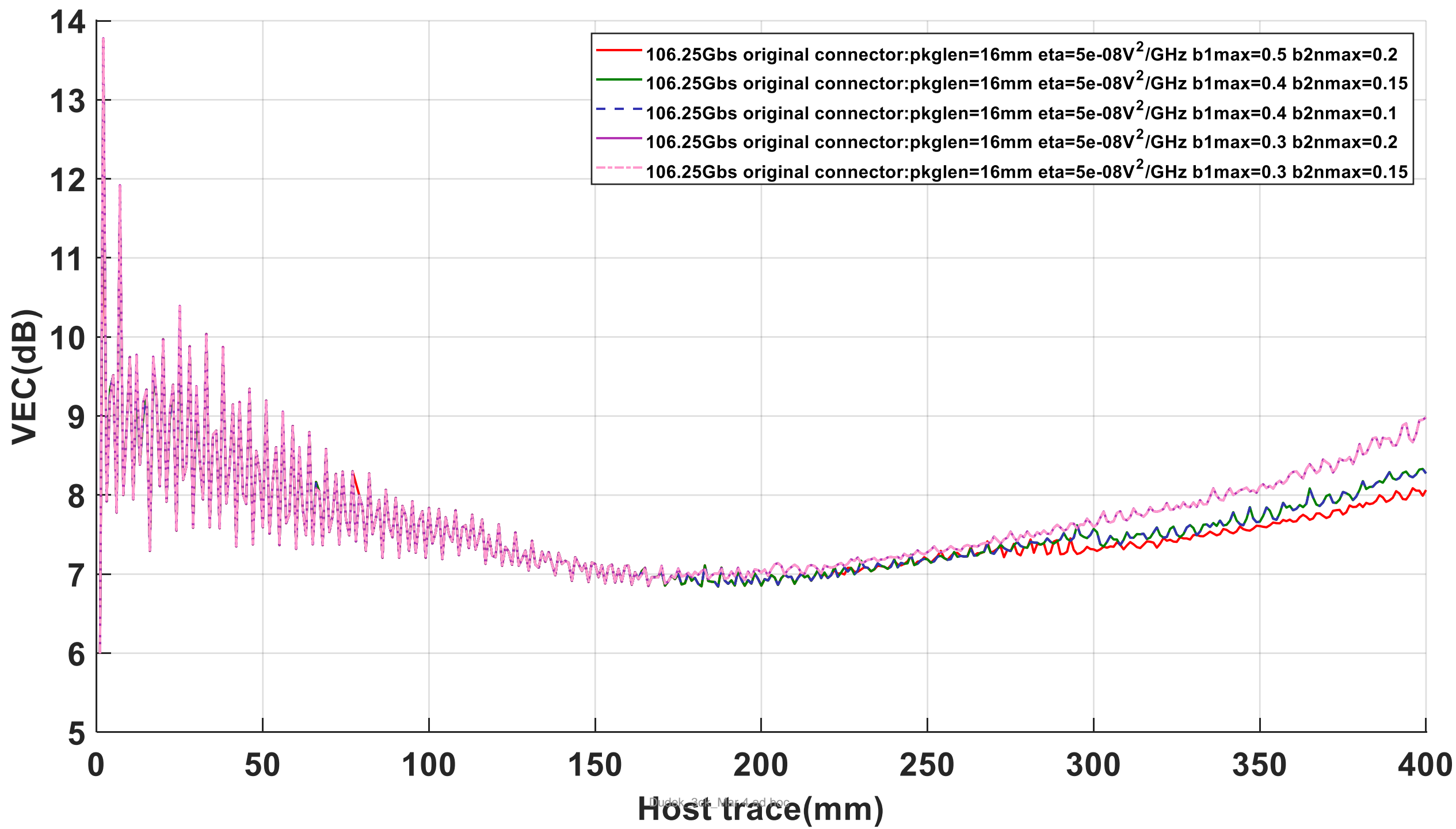


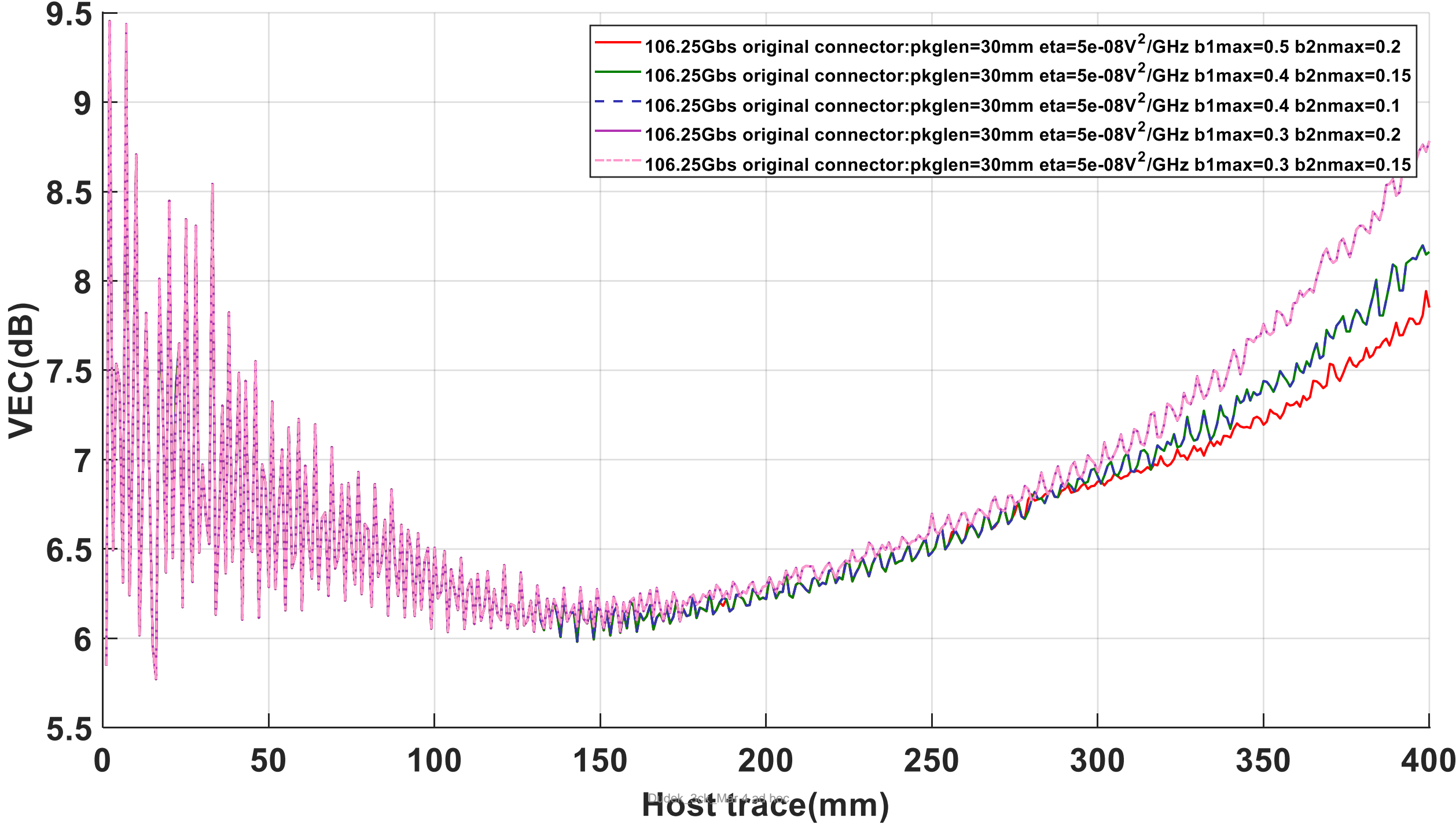


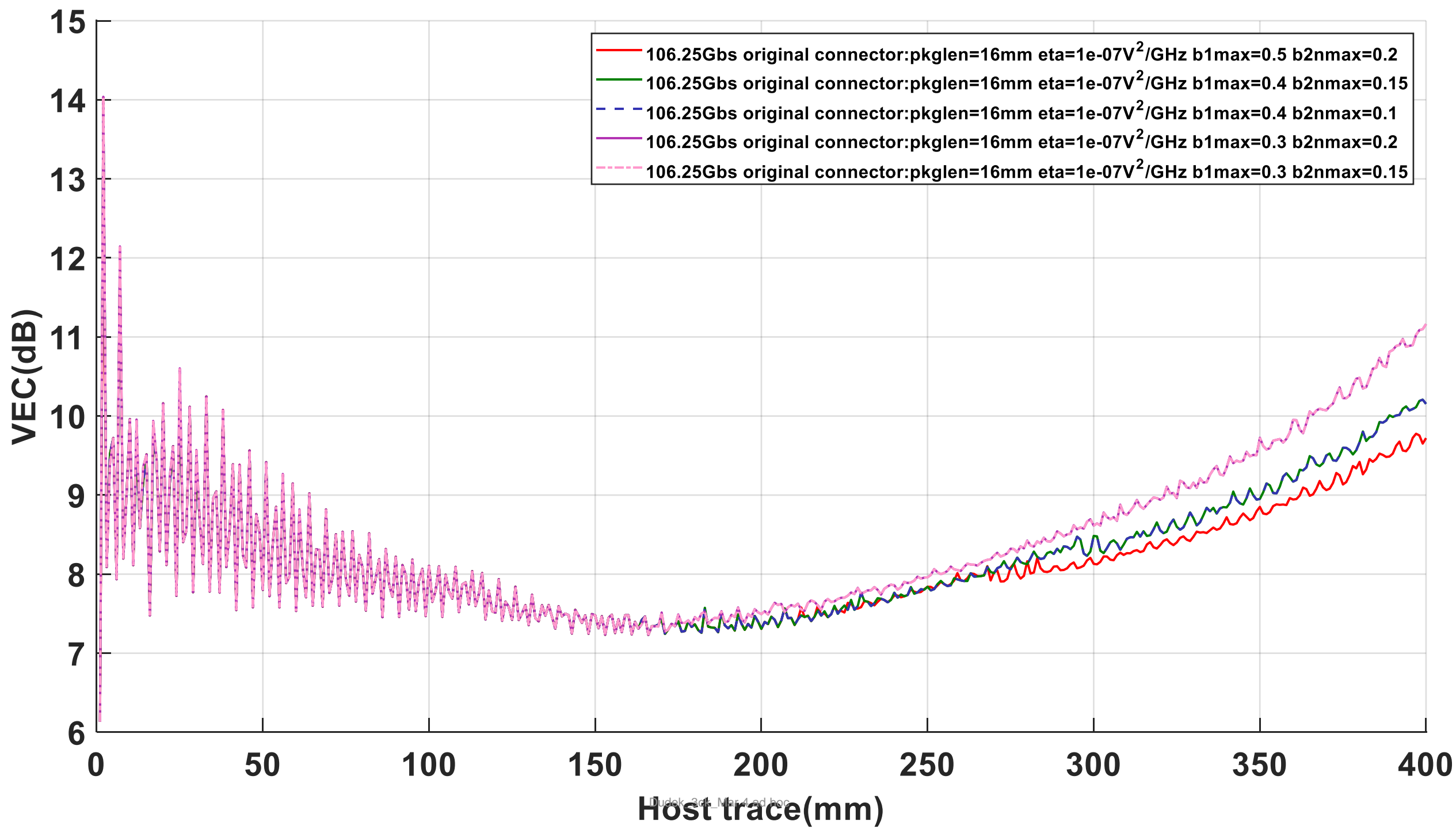


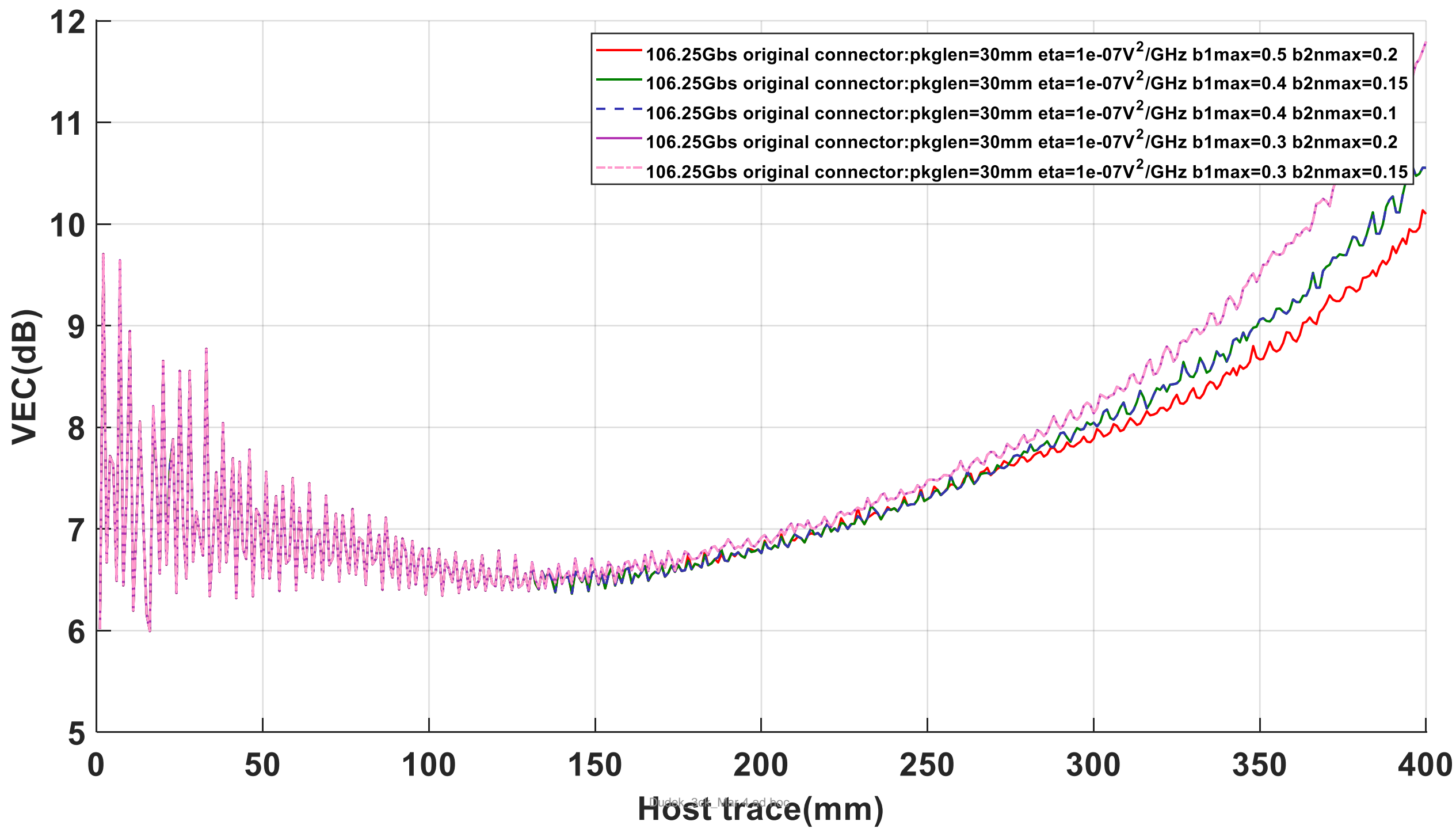


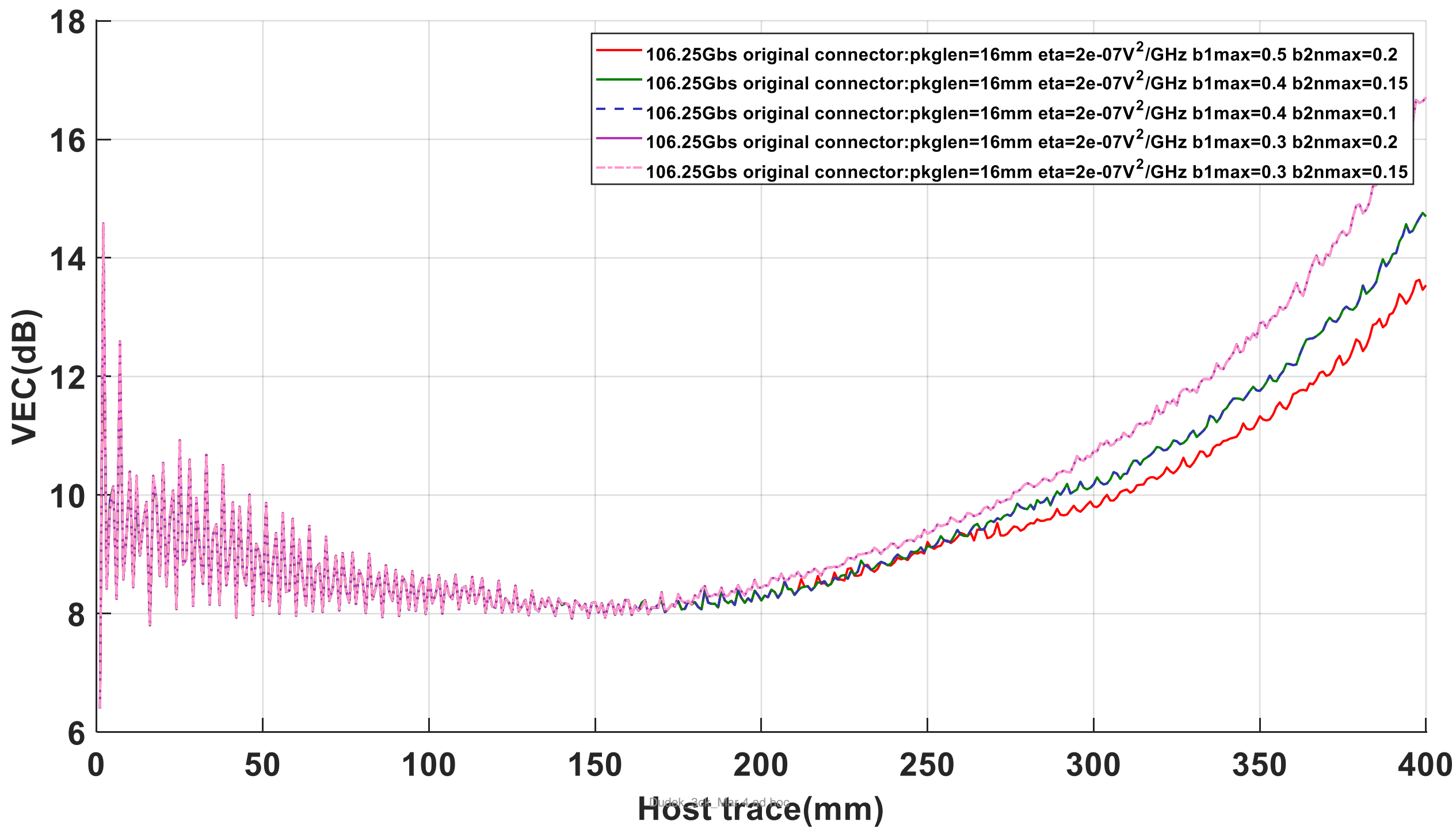


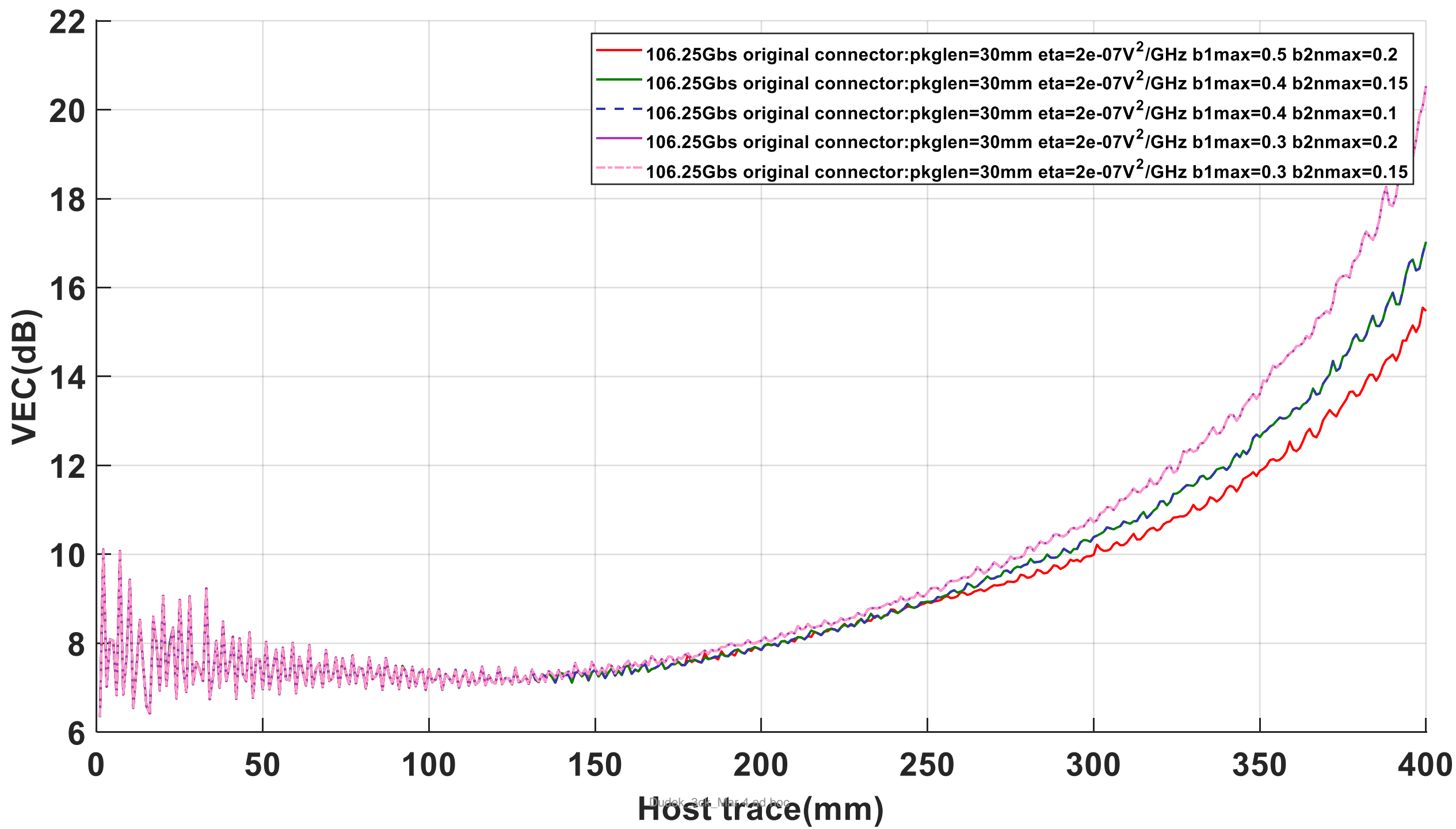






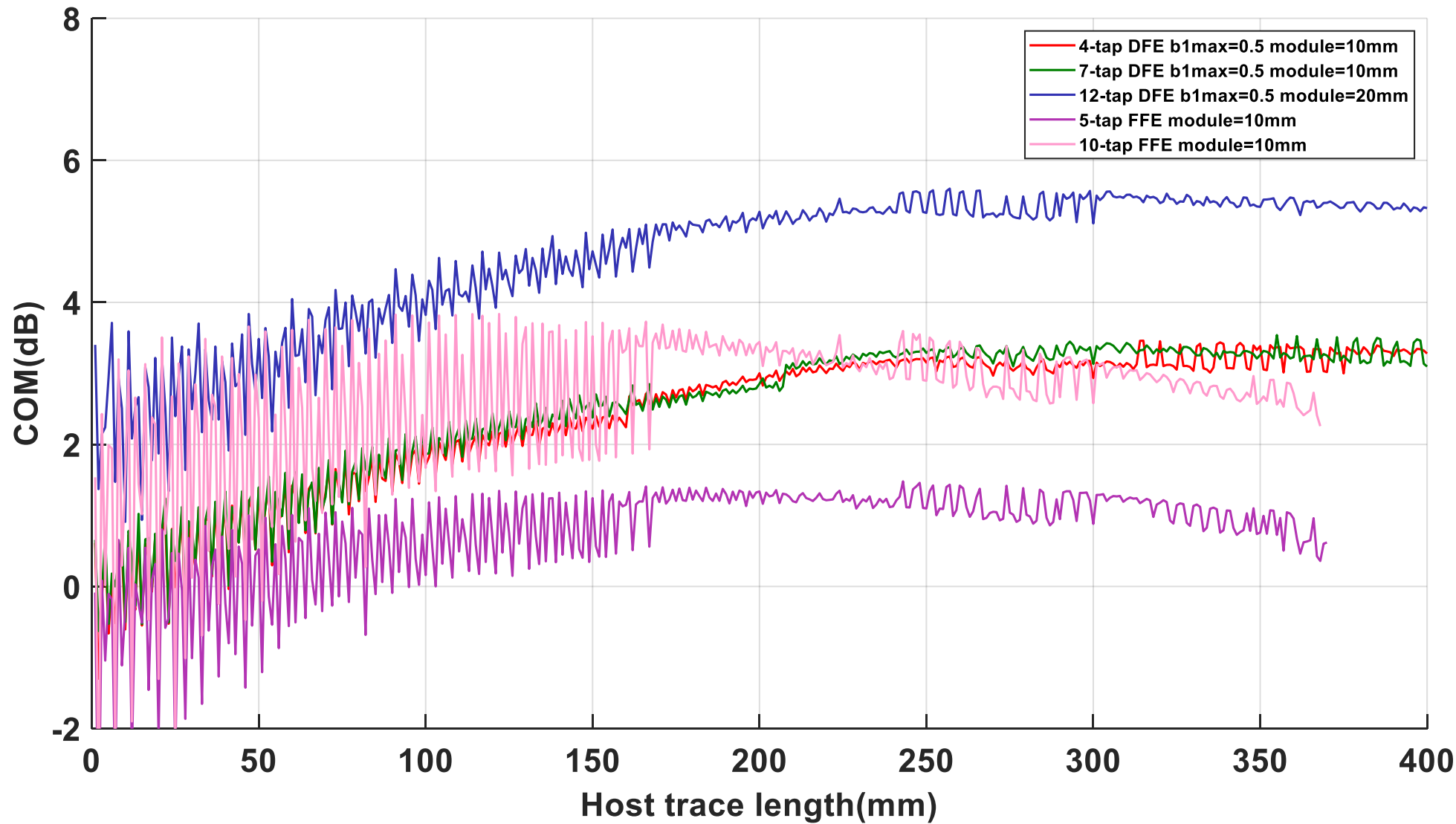






Additional useful back-up

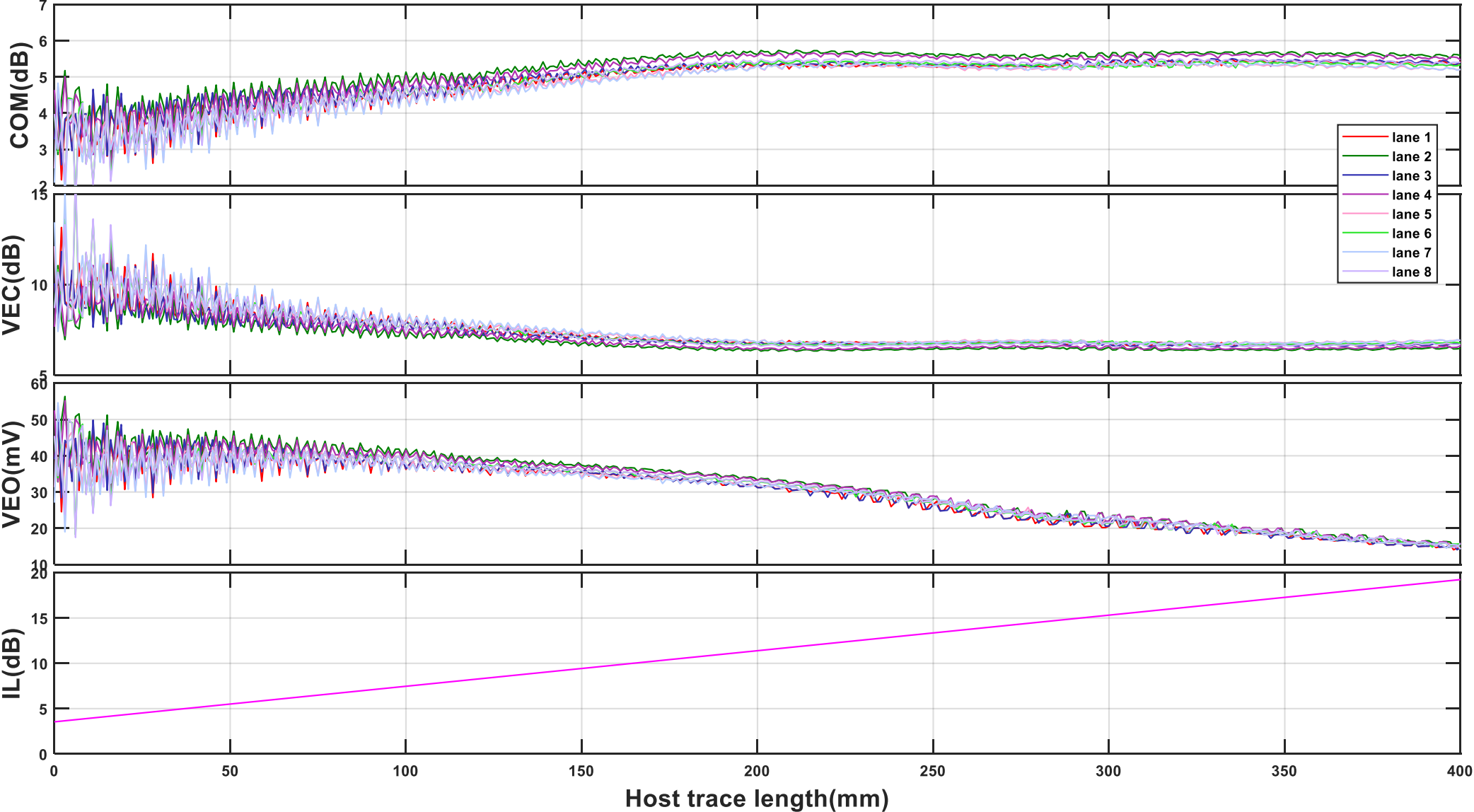
End to end COM examples with approximate worst case module length and TX FIR optimized for 4 tap DFE at TP1a (from Dudek_3ck_01_1119)



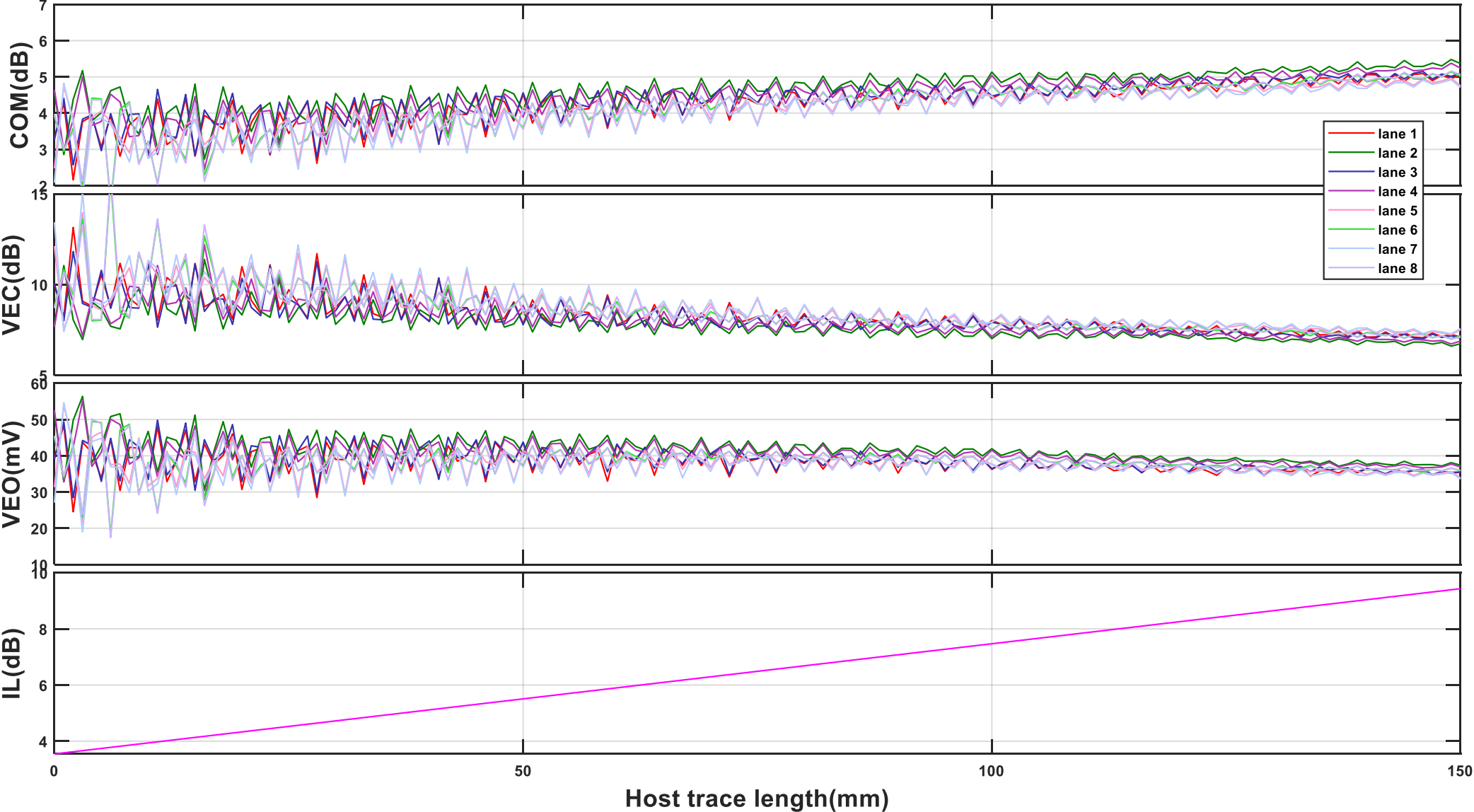
COM PCB and package loss information

- PCB loss at 26.56GHz: $\sim 0.04\text{dB/mm}$, $\sim 1\text{dB/in.}$ (58mm is equivalent to the 2.3dB MCB loss being proposed in the cable small group).
- Package loss at 26.56GHz: 0.1dB/mm
- Insertion loss plotted in this presentation includes host, HCB and connector, but not package.

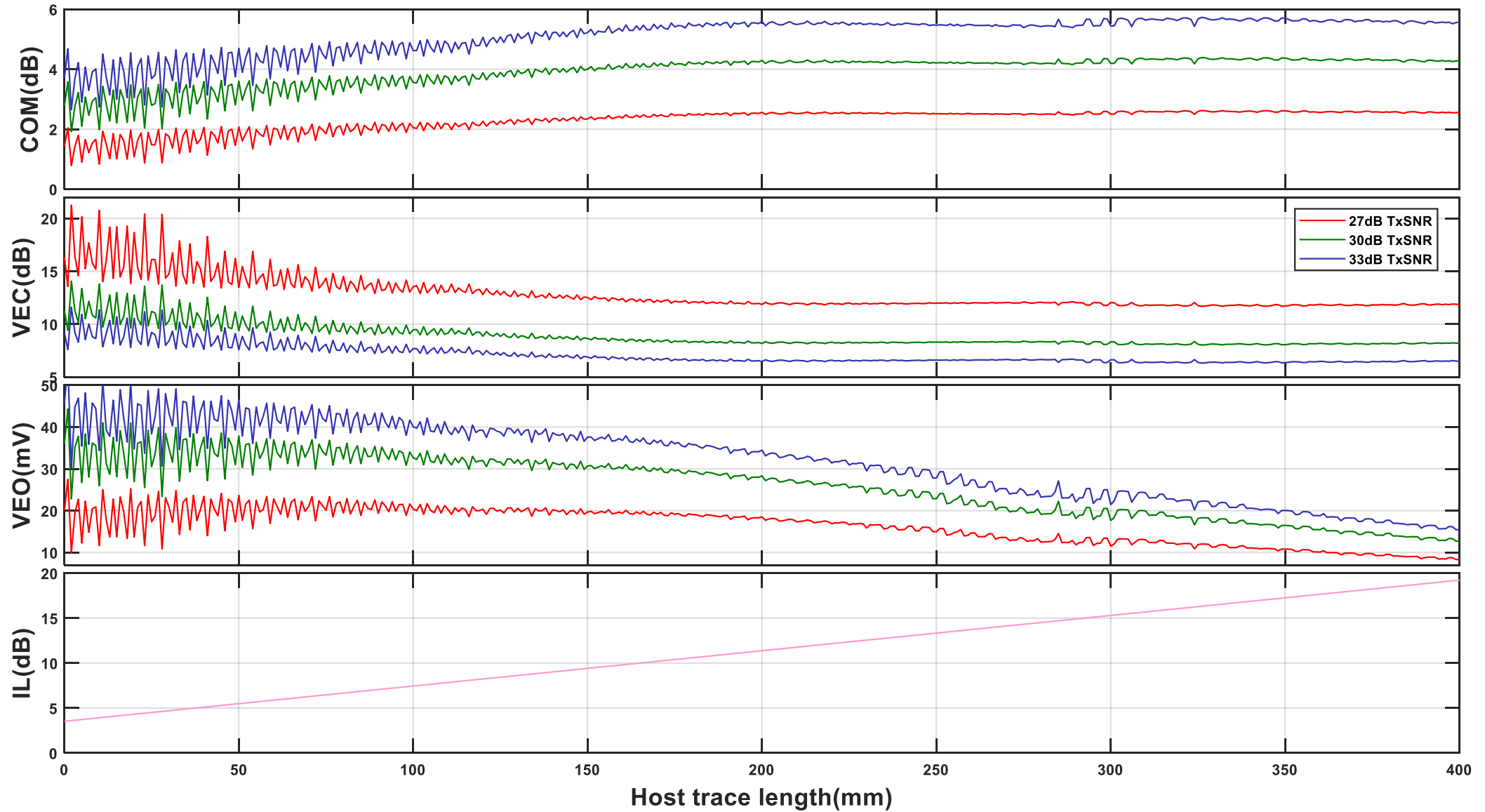
Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host



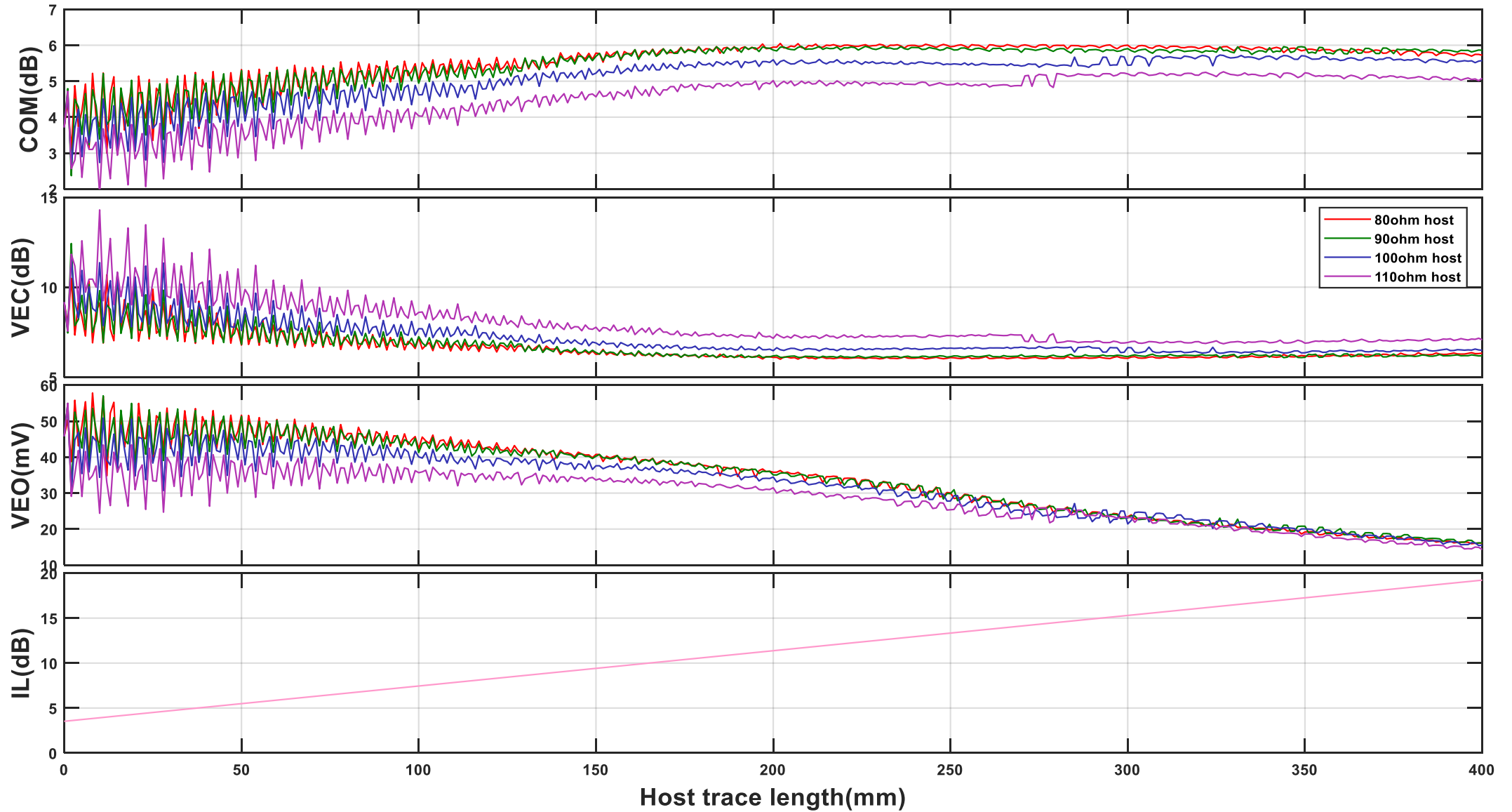
Cd 0.11pF Ls 0pH Cb 0pF 15mm pkg 100ohm host



TP1a results by TxSNR



TP1a results by host impedance



M A R V E L L[®]