# Solutions for Multi-Tap DFE Error Propagation (Summary)

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# Solutions for Multi-Tap DFE Error Propagation

| # | | PMD Solutions | | "PMA Remapping" | "Interleaved FEC" | |
|---|---|---|---|---|---|---|
| | | Constrain DFE weight | EoBD (lu_3ck_01_0319) | "PMA re-mapping" / "4:1 symbol mux" (lu_3ck_adhoc_01_041019) | "2:1 bit mux" (gustlin_3ck_01_0119) | "4:1 bit mux" (nicholl_3ck_adhoc_01b_042419) |
| **Performance** | | **OK** | **OK** (Best) | **OK** | **OK** | **OK** (Slightly worse) |
| **Complexity Increase** | **Host IC** | **Negligible** | | **Negligible** | **1x 50G RS(544, 514) Encoder/Decoder.** | |
| | **CDR** | **0** | | **0** FEC decoders have already been integrated inside CDR. | 2x FECL processing<br>2x 50G + 1x 100G RS(544, 514) Encoder<br>1x 50G RS(544, 514) Decoder.<br>**All the functions are mandatory.** | |
| **Latency Increase** | **Host IC** | **0** | | **0** | **>50ns** | |
| | **CDR** | **0** | | **0ns w/o "FEC recovery" support;**<br>~100ns w/ "FEC recovery" support. | **>150ns 1 CDR;**<br>**>250ns 2 CDR.** | |
| **Protocol independent "FEC recovery" support** | | **No** | | **Yes,** FEC can be self-synchronized. | **No,** Has to process the FECLs and "FEC conversion". | |
| **Define new Alignment Markers** | | **No** | | **No** | **Yes** | **No** |
| **Standard Effort** | | **None** | | **Minor *** | **A New Clause** for "FEC conversion". | |

* Optional PMA-remapping function within PMA Sublayer.

# Thank you !

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