

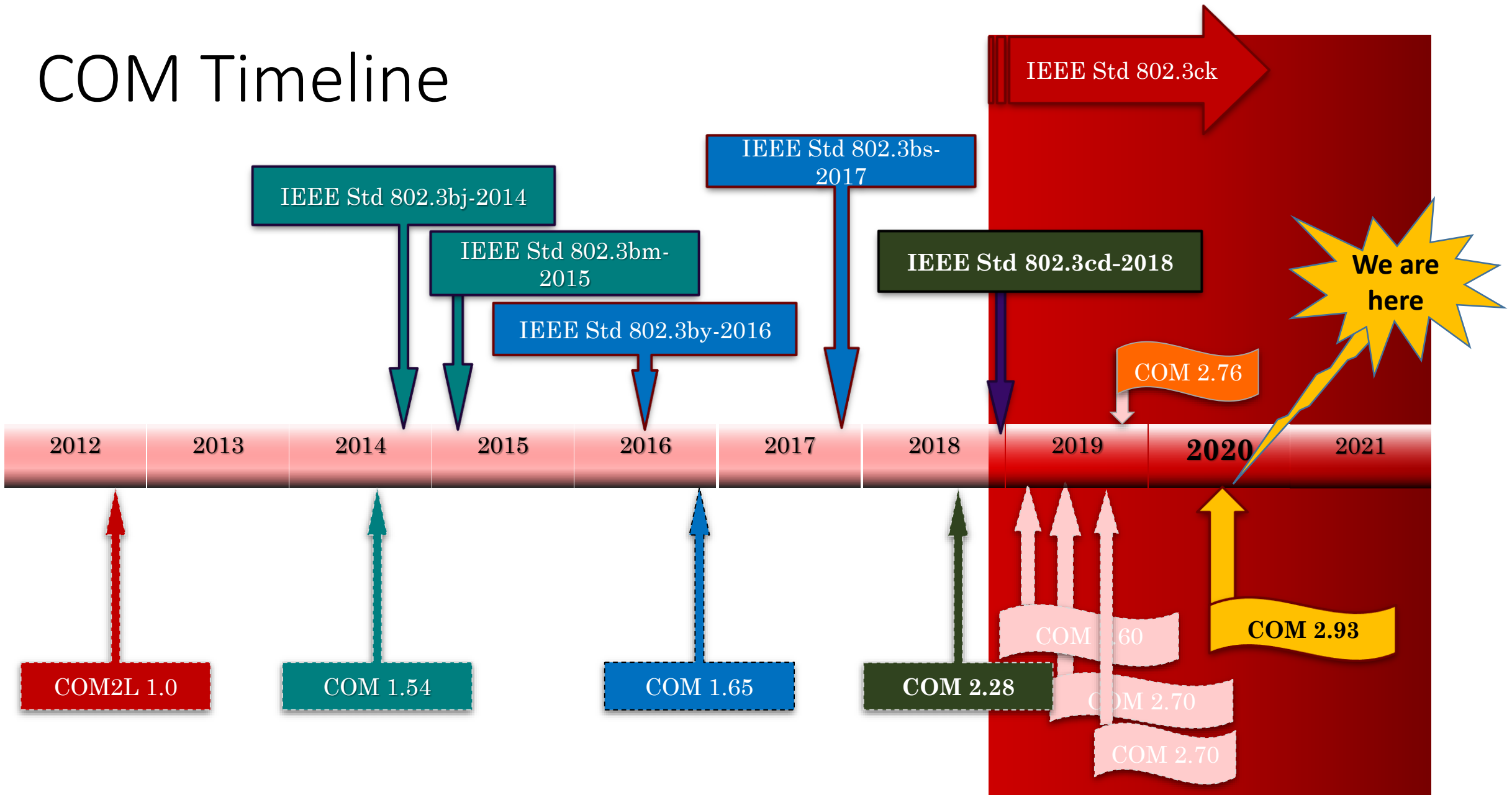
# COM 2.93 UPDATE

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IEEE 802.3 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Task Force Ad Hoc

# COM Timeline



# Motivation

- ❑ Correct problem with Matlab implementation of voltage transfer function
  - EQ 93A-18, 93A-19, and 93A-46
- ❑ No problem for prior COM implementations
- ❑ If  $R_d$  is not 50 ohms or die to die loss is less than 5 dB
  - There maybe an error in the voltage transfer function which is a little pessimistic.
- ❑ Impact is only for very short channel explorations when performing termination sweeping
- ❑ Discovered by Ed Frlan and Bill Kirkland

# Other additions for moving project forward

- ❑ Heuristic speed up for optimizing the equalizers suggested by Adee Ran.
  - Improve COM run time up to 75%
  - May be applicable for test equipment
- ❑ Added  $b_{\min}$  which are minimum DFE tap limits
- ❑ Maximum GDC gain added
- ❑ Feature to remove reflections at packages/board interface
  - See [mellitz\\_3ck\\_01a\\_0320](#)

# New Optional keywords

	keyword	example	comments
Heuristic speed up for optimizing the equalizers			
	<b>Local Search</b>	<b>2</b>	<b>Search coef. distance. If set to 0 use full grid search.</b>
Added $b_{\min}$ which are minimum DFE tap limits			
	<b>b_min(1)</b>	<b>-0.85</b>	<b>DFE lower magnitude limit, first coefficient(ignored if Nb=0)</b>
	<b>b_min(2..N_b)</b>	<b>-[0.3 0.2*ones(1,10)]</b>	<b>DFE lower magnitude limit, second coefficient and on (ignored if Nb&lt;2)</b>
Maximum ACDC gain for gain for CTF			
	<b>GDC_MIN</b>	<b>-18</b>	<b>max acdc gain(dB), usually a negative number i.e. a min</b>
remove reflections at packages/board interface			
	<b>kappa1</b>	<b>1</b>	<b>if set 0 reflection at tp0 are omitted from COM</b>
	<b>kappa2</b>	<b>1</b>	<b>if set 0 reflection at tp5 are omitted from COM</b>

# D1.2 KR configuration example: Please note TBDs

Table 93A-1 parameters				I/O control			Table 93A-3 parameters		
Parameter	Setting	Units	Information				Parameter	Setting	Units
f_b	53.125	GBd		DIAGNOSTICS	1	logical	package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz		DISPLAY_WINDOW	1	logical	package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz		CSV_REPORT	1	logical	package_Z_c	[87.5 87.5 ; 92.5 92.5 ]	Ohm
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]	RESULT_DIR	.\results\100GEL_KR_{date}\		<b>benartsi_3ck_01_0119 &amp; mellitz_3ck_01_0119</b>		
L_s	[0.12, 0.12]	nH	[TX RX]	SAVE_FIGURES	0	logical	Table 92-12 parameters		
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]	Port Order	[1 3 2 4]		Parameter	Setting	
z_p select	[ 1 2 ]		[test cases to run]	RUNTAG	KR_eval_		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]	COM_CONTRIBUTION	0	logical	board_tl_tau	5.790E-03	ns/mm
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]	<b>Operational</b>			board_Z_c	100	Ohm
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]	COM Pass threshold	3	dB	z_bp (TX)	110.3	mm
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]	ERL Pass threshold	10.5	dB	z_bp (NEXT)	110.3	mm
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]	DER_0	1.00E-04		z_bp (FEXT)	110.3	mm
R_0	50	Ohm		T_r	0.006160714	ns	z_bp (RX)	110.3	mm
R_d	[ 50 50]	Ohm	[TX RX]	FORCE_TR	1	logical	C_0	[0.29e-4]	nF
A_v	0.413	V		<b>Local Search</b>	<b>2</b>		C_1	[0.19e-4]	nF
A_fe	0.413	V		<b>TDR and ERL options</b>			<b>Include PCB</b>	<b>0</b>	<b>logical</b>
A_ne	0.608	V		TDR	1	logical	<b>Floating Tap Control</b>		
L	4			ERL	1	logical	N_bg	3	0 1 2 or 3 groups
M	32			ERL_ONLY	0	logical	N_bf	3	taps per group
<b>filter and Eq</b>				TR_TDR	0.01	ns	N_f	40	UI span for floating taps
f_r	0.75	*fb		N	3000		bmaxg	0.05	max DFE value for floating taps
c(0)	0.54		min	beta_x	0.0000E+00		B_float_RSS_MAX	0.02	rss tail tap limit
c(-1)	[-0.34:0.02:0]		[min:step:max]	rho_x	0.618		N_tail_start	25	(UI) start of tail taps limit
c(-2)	[0:0.02:0.12]		[min:step:max]	fixture delay time	[ 0 0 ]	[ port1 port2 ]	<b>ICN parameters</b>		
c(-3)	[-0.06:0.02: 0]		[min:step:max]	TDR_W_TXPKG	0		f_v	0.723	*Fb
c(1)	[-0.2:0.05:0]		[min:step:max]	N_bx	21	UI	f_f	0.723	*Fb
N_b	12	UI		<b>Receiver testing</b>			f_n	0.723	*Fb
b_max(1)	0.85			RX_CALIBRATION	0	logical	f_2	39.844	GHz
b_max(2..N_b)	[0.3 0.2*ones(1,10)]			Sigma BBN step	5.00E-03	V	A_ft	0.600	V
<b>b_min(1)</b>	<b>-0.85</b>			<b>Noise, jitter</b>			<b>A_nt</b>	<b>0.600</b>	<b>V</b>
<b>b_min(2..N_b)</b>	<b>-[0.3 0.2*ones(1,10)]</b>			sigma_RJ	0.01	UI	<b>TBD in document      under consideration</b>		
g_DC	[-20:1:0]	dB	[min:step:max]	A_DD	0.02	UI	<b>new</b>		
f_z	21.25	GHz		eta_0	8.2E-09	V^2/GHz			
f_p1	21.25	GHz		SNR_TX	33	dB			
f_p2	53.125	GHz		R_LM	0.95				
g_DC_HP	[-6:1:0]		[min:step:max]						
f_HP_PZ	0.6640625	GHz							
<b>GDC_MIN</b>	<b>0</b>	<b>dB</b>	<b>0 is and ignore</b>						

# D1.2 CR CA configuration example: Please note TBDs

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]
L_s	[0.12, 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[ 1 2 ]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[ 50 50]	Ohm	[TX RX]
A_v	0.413	V	
A_fe	0.413	V	
A_ne	0.608	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02: 0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	12	UI	
b_max(1)	0.85		
b_max(2..N_b)	[0.3 0.2*ones(1,10)]		
b_min(1)	-0.85		
b_min(2..N_b)	-[0.3 0.2*ones(1,10)]		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	
GDC_MIN	0	dB	0 is and ignore

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-04	
T_r	0.006160714	ns
FORCE_TR	1	logical
Local Search	2	
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	7000	
beta_x	0.0000E+00	
rho_x	0.618	
fixture delay time	[ 0 0 ]	[ port1 port2 ]
TDR_W_TXPKG	0	
N_bx	21	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	1.00E-08	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5 ]	Ohm
benartsi_3ck_01_0119 & mellitz_3ck_01_0119		
Table 92-12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	5.790E-03	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	110.3	mm
z_bp (NEXT)	110.3	mm
z_bp (FEXT)	110.3	mm
z_bp (RX)	110.3	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	1	logical
Floating Tap Control		
N_bg	3	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	40	UI span for floating taps
bmaxg	0.05	max DFE value for floating taps
B_float_RSS_MAX	0.02	rss tail tap limit
N_tail_start	25	(UI) start of tail taps limit
ICN parameters		
f_v	0.723	*Fb
f_f	0.723	*Fb
f_n	0.723	*Fb
f_2	39.844	GHz
A_ft	0.600	V
A_nt	0.600	V
TBD in document	under consideration	
new		

# D1.2 C2C configuration example: Please note TBDs

Table 93A-1 parameters				I/O control			Table 93A-3 parameters		
Parameter	Setting	Units	Information				Parameter	Setting	Units
f_b	53.125	GBd		DIAGNOSTICS	1	logical	package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz		DISPLAY_WINDOW	1	logical	package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz		CSV_REPORT	1	logical	package_Z_c	[87.5 87.5 ; 92.5 92.5 ]	Ohm
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]	RESULT_DIR	.\results\100GEL_KR_{date}\		benartsi_3ck_01_0119 & mellitz_3ck_01_0119		
L_s	[0.12, 0.12]	nH	[TX RX]	SAVE_FIGURES	0	logical	Table 92-12 parameters		
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]	Port Order	[1 3 2 4]		Parameter	Setting	
z_p select	[ 1 2 ]		[test cases to run]	RUNTAG	KR_eval_		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (TX)	[13 31; 1.8 1.8]	mm	[test cases]	COM_CONTRIBUTION	0	logical	board_tl_tau	5.790E-03	ns/mm
z_p (NEXT)	[11 29; 1.8 1.8]	mm	[test cases]	Operational			board_Z_c	100	Ohm
z_p (FEXT)	[13 31; 1.8 1.8]	mm	[test cases]	COM Pass threshold	3	dB	z_bp (TX)	110.3	mm
z_p (RX)	[11 29; 1.8 1.8]	mm	[test cases]	ERL Pass threshold	10.5	dB	z_bp (NEXT)	110.3	mm
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]	DER_0	1.00E-05		z_bp (FEXT)	110.3	mm
R_0	50	Ohm		T_r	0.006160714	ns	z_bp (RX)	110.3	mm
R_d	[ 50 50]	Ohm	[TX RX]	FORCE_TR	1	logical	C_0	[0.29e-4]	nF
A_v	0.413	V		Local Search	2		C_1	[0.19e-4]	nF
A_fe	0.413	V		TDR and ERL options			Include PCB	0	logical
A_ne	0.608	V		TDR	1	logical	Floating Tap Control		
L	4			ERL	1	logical	N_bg	0	0 1 2 or 3 groups
M	32			ERL_ONLY	0	logical	N_bf	0	taps per group
filter and Eq				TR_TDR	0.01	ns	N_f	40	UI span for floating taps
f_r	0.75	*fb		N	2000		bmaxg	0.05	max DFE value for floating taps
c(0)	0.54		min	beta_x	0		B_float_RSS_MAX	0.02	rss tail tap limit
c(-1)	[-0.34:0.02:0]		[min:step:max]	rho_x	0.618		N_tail_start	25	(UI) start of tail taps limit
c(-2)	[0:0.02:0.12]		[min:step:max]	fixture delay time	[ 0 0 ]	[ port1 port2 ]	ICN parameters		
c(-3)	[-0.06:0.02: 0]		[min:step:max]	TDR_W_TXPKG	0		f_v	0.723	*Fb
c(1)	[-0.2:0.05:0]		[min:step:max]	N_bx	6	UI	f_f	0.723	*Fb
N_b	6	UI		Receiver testing			f_n	0.723	*Fb
b_max(1)	0.85			RX_CALIBRATION	0	logical	f_2	39.844	GHz
b_max(2..N_b)	0.2			Sigma BBN step	5.00E-03	V	A_ft	0.600	V
b_min(1)	-0.85			Noise, jitter			A_nt	0.600	V
b_min(2..N_b)	-0.2			sigma_RJ	0.01	UI	TBD in document		
g_DC	[-20:1:0]	dB	[min:step:max]	A_DD	0.02	UI	under consideration		
f_z	21.25	GHz		eta_0	8.2E-09	V^2/GHz	new		
f_p1	21.25	GHz		SNR_TX	33	dB			
f_p2	53.125	GHz		R_LM	0.95				
g_DC_HP	[-4:1:0]		[min:step:max]						
f_HP_PZ	0.6640625	GHz							



**Thank You!**