C2M TP1a VEC and VEO vs. Whole Link COM Correlation

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IEEE 802.3ck Task Force

Contributors

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Outline

- Background
- Channels and COM Settings for Analysis
- TP1a to Whole Link Correlation
- Modified VEC Mask
- Summary

TP1a VEC vs. Whole Link COM

- Phil Sun had explored this topic since 2019 Long Beach meeting
  - sun_3ck_01b_0119, sun_3ck_01_0319, sun_3ck_01_0519 – explored four possible reference receiver & the correlation of TP1a VEC to whole link COM
    - Proposed to have VEC threshold 9.0 dB or 10.5 dB
    - 9.0 dB: if receiver A (4-tap DFE) or receiver B (5-tap FFE with 1-tap DFE) were adapted
    - 10.5 dB: if receiver C (5-tap FFE) or receiver D (4-tap DFE with b1max=0) were adapted
- Mike Li and Mau-Lin Wu also explored this topic independently
  - li_3ck_01_0319, li_3ck_02a_0519, wu_3ck_01a_0919
- Host 2 module short channel issue was raised
  - li_3ck_02a_0519, dudek_3ck_01_0719, sun_3ck_adhoc_01_081419, akinwale_3ck_adhoc_01a_08282019, wu_3ck_01a_0919, dudek_3ck_01_0919, sun_3ck_01b_0919
- Ali Ghiasi and Phil Sun raised the ideas of replacing VEC-only threshold by VEC_and_VEO combined threshold
  - ghiasi_3ck_02a_0919, sun_3ck_01b_0919
- In this contribution, we explored VEC_and_VEO combined threshold vs whole link COM correlation by
  - Analysis of total 19 IEEE host to module channels, short and long
  - Sweeping wide range of TX host trace length by considering short channel issue
- Observation
  - VEC_and_VEO combined threshold show no improvements

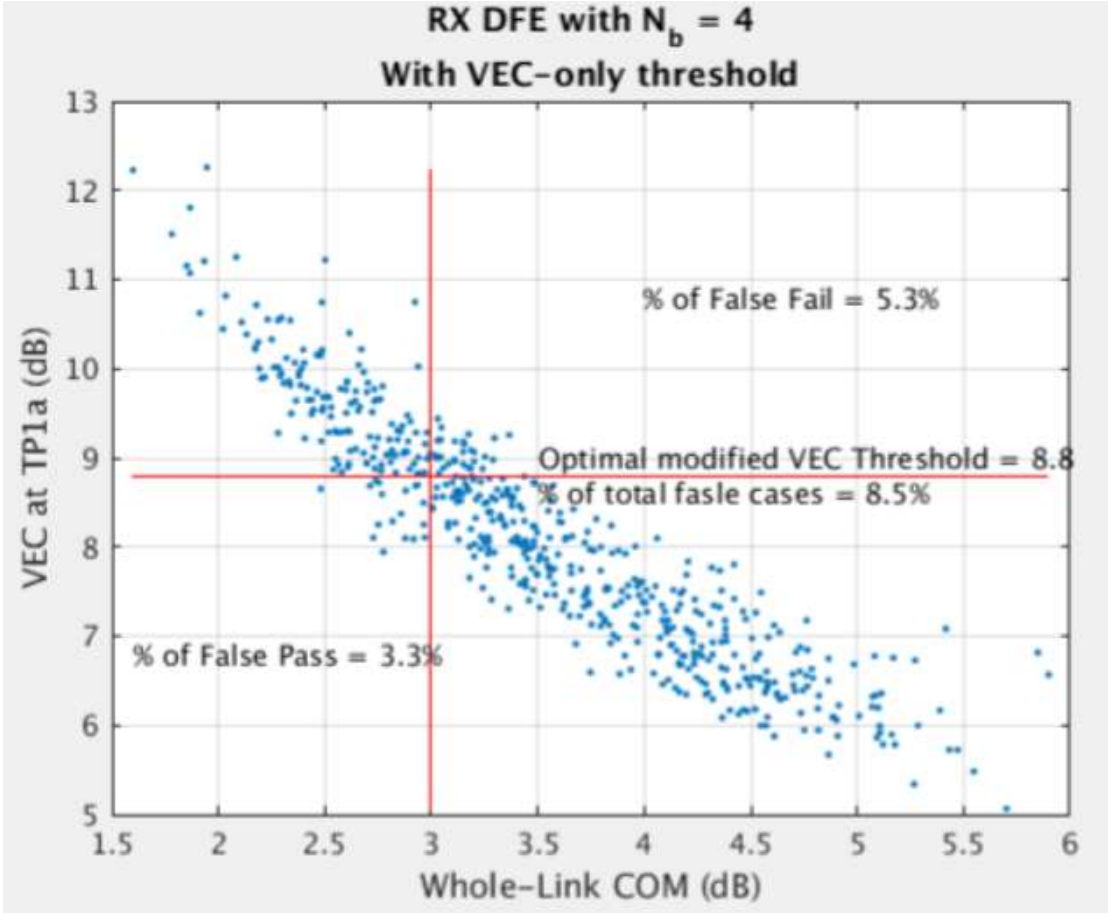
Channel and Analysis

- Channel and reference receiver
  - Whole-link & TP1a analysis for total 19 IEEE C2M host-to-module channels
    - Sweep host package trace length, z_p1(TX)
      - z_p1(TX) = [5:0.5:10 11:1:20 22:2:36]
    - total 19 * 29 = 551 CH+PKG test cases
  - RX with sweeping tap number
    - DFE with 3 ~ 4 taps
- COM parameter settings [details in appendix]
  - COM 2.70
  - Whole link: TX PKG + H2M Channels + RX PKG
    - On-die
      - Host [healey_3ck_adhoc_01_061219]
      - Module: Table 1
    - PKG
      - Host [baseline]
      - Module: Table 1
    - g_DC = [-14:1:0] dB
    - g_DC_HP = [-3:1:0] dB
  - TP1a: TX PKG + H2M Channels
    - Set ‘zero’ to related RX PKG & on-die settings

Table 1

Spec	[Host, Module]	Unit
C_d	[1.2e-4 0.85e-4]	nF
L_s	[0.12 0.12]	nH
C_b	[0.3e-4 0.3e-4]	nF
R_d	[50 50]	Ohm
C_p	[0.87 0.65]	nF
z_p(RX)	[5 0]	Ohm

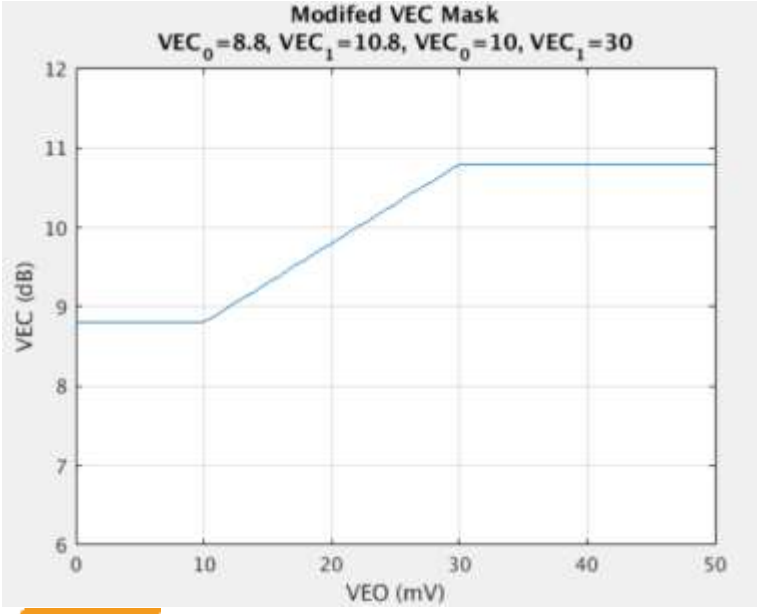
TP1a vs. Whole Link Correlation – 4-tap DFE

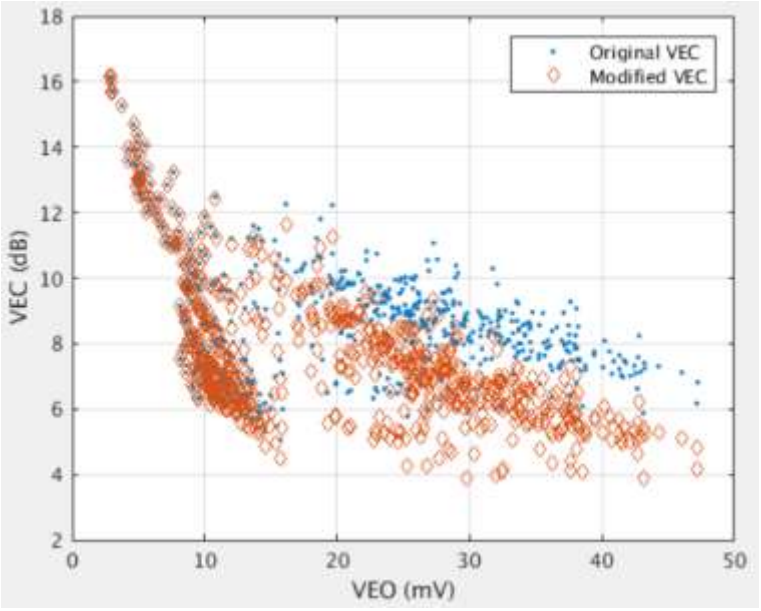


- Methodology
  - Find optimal VEC threshold by minimizing % of total false cases
  - Total false cases = False Fail + False True
  - False Fail
    - COM >= 3 dB, while VEC > VEC_TH
  - False Pass
    - COM < 3 dB, while VEC <= VEC_TH
- Correlation of VEC to COM is obvious
- Results
  - Optimized VEC_TH = 8.8 dB
  - % of total false = 8.5%
  - False cases distribute among several channels

VEC_and_VEO Combined Threshold

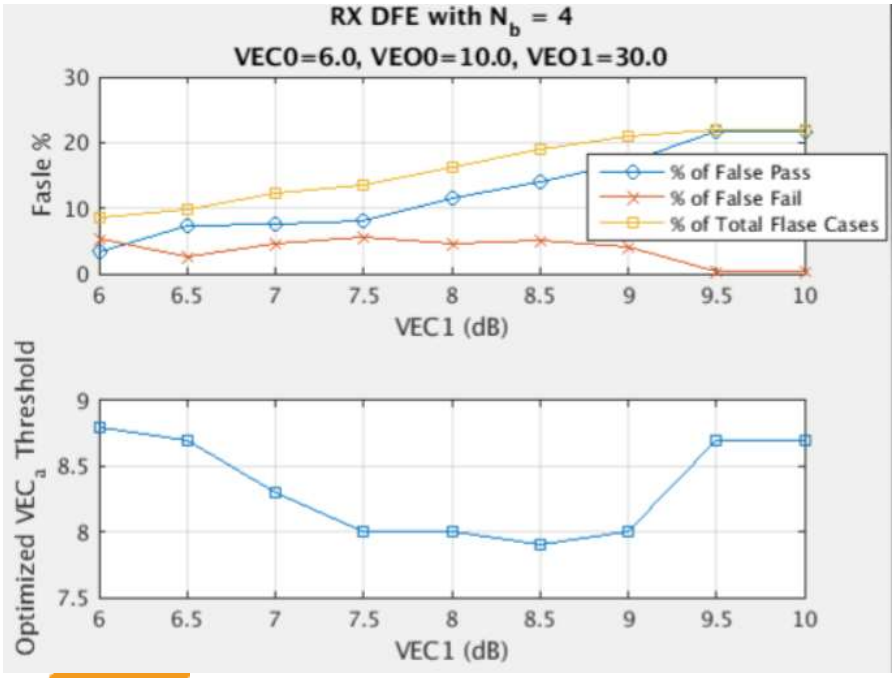
- Ideas
  - If VEO is larger than some specific threshold (***VEO$_0$***), VEC threshold could be relaxed (larger)
- Derivative of ***VEC$_a$***, modified VEC
  - $$VEC_a(i) = \begin{cases} VEC(i), & if\ VEO(i) < VEO_0 \\ VEC(i) - Slope_m \times (VEO(i) - VEO_0), & if VEO_0 \le VEO(i) < VEO_1 \\ VEC(i) - (VEC_1 - VEC_0), & otherwise \end{cases}$$
  - $Where\ Slope_m = (VEC_1\text{-}VEC_0)/(VEO_1\text{-}VEO_0)$
- Find optimized VEC Threshold based on ***VEC$_a$*** by minimizing total false ratio
- We sweep ***VEC$_0$***, ***VEC$_1$***, ***VEO$_0$*** and ***VEO$_1$*** to find solutions

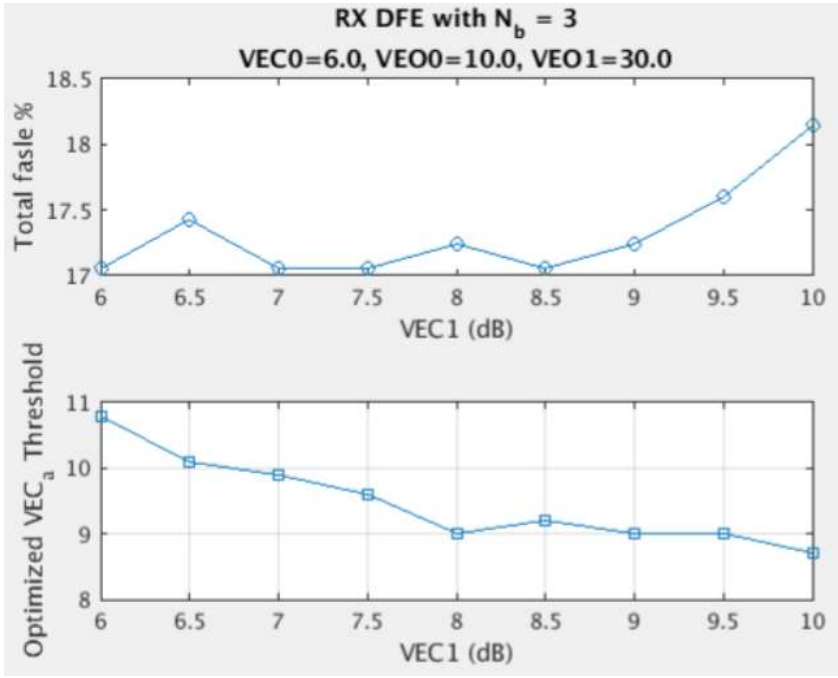




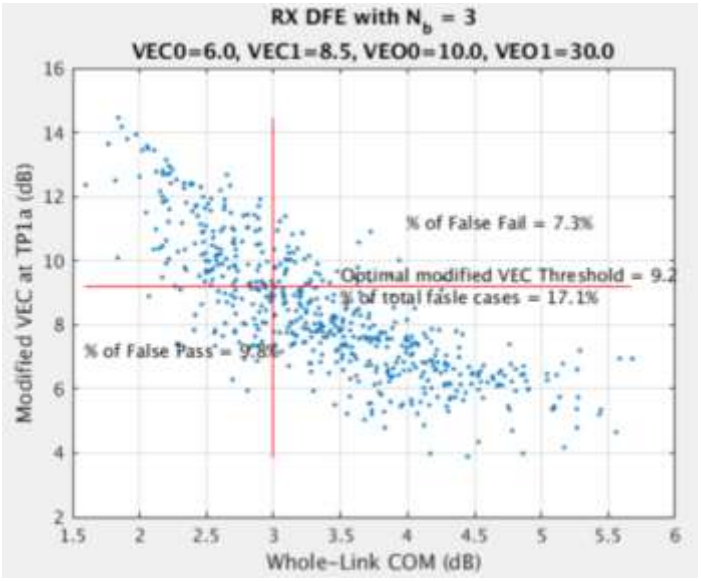
Modified VEC Mask – Results

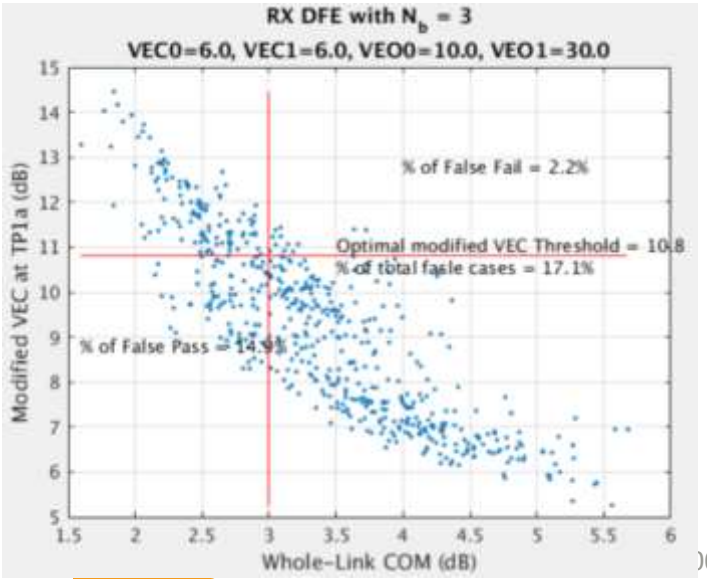
- N_b = 4 case, the case with VEC modification is best
  - VEC1 = VEC0
  - VEC_TH = 8.8 dB
  - False % = 8.5%
- N_b = 3 case, modified VEC mask has same 'Total false %' for several settings
  - VEC1 = VEC0 + 0, 1.0, 1.5, 2.5 dB
  - VEC_TH = 9 ~ 11 dB
  - False % = 17.1%



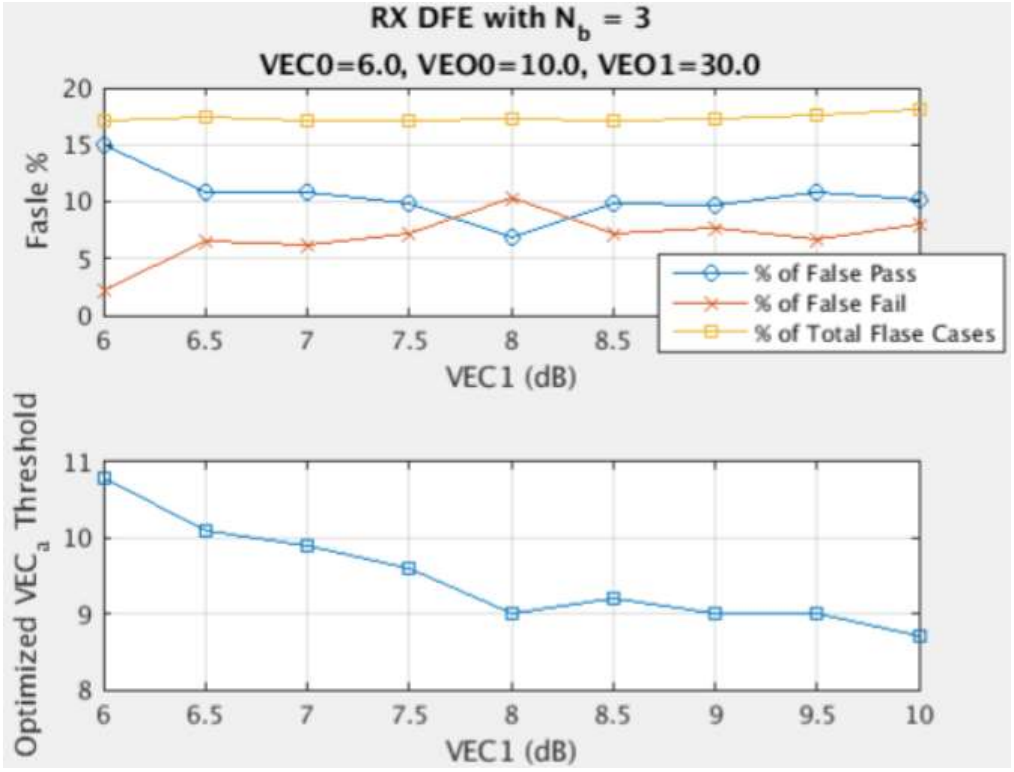


N_b=3 case – Better Balance False Ratios





- Better balanced False ratios
- VEC1-VEC0 = 2.5 dB vs. 0 dB
  - 2.5 dB: 9.8% + 7.3% = 17.1%
    - False cases distribute among several channels
  - 0 dB: 14.9% + 2.2% = 17.1%



Summary

- By DFE reference receiver, 4-tap DFE has good correlation for TP1a VEC vs. whole-link COM
  - With total false ratio = 8.5% by VEC threshold = 8.8 dB
  - For 3-tap DFE, the correlation degrade to false ratio = 17.1%
- With modified VEC mask by considering VEO together
  - Can’t improve false ratio for 4-tap DFE case
  - Only improve balance among False Pass and False Fail distribution for 3-tap DFE case
  - Modified VEC mask doesn’t help a lot
- Proposal
  - Make it simple as taking VEC-only mask

everyday genius

Host to Module Short Channel Issue

- Performance fluctuates a lot for different host trace lengths, which were disclosed in
  - li_3ck_02a_0519, dudek_3ck_01_0719
- Jane Lim provided four Host-to-Module (H2M) channels for analysis
  - lim_3ck_adhoc_01_073119
- Some analysis of 'short channel issue' were included in
  - sun_3ck_adhoc_01_081419 – Phil proposed to avoid this issue by adding package/host trace design constraints?
  - akinwale_3ck_adhoc_01a_08282019 – Femi analyzed this issue by Intel's H2M channels
  - wu_3ck_01a_0919, dudek_3ck_01_0919, sun_3ck_01b_0919 – more analysis disclosed in 2019 Indianapolis meeting
- The majority thought it's essential to identify a solution to the C2M short channel issue before adopting a reference receiver and VEC specification
  - Straw Poll #8 of minutes_3ck_0919_unconfirmed
    - Results: Y:25, N: 2, A: 17

C2M Channels for Analysis

Contribution	Zip files	Channel	SxP Files
lim_3ck_01a_0319	lim_3ck_01_0319_c2m.zip	Tx7_L10	112G_16dB_(QSFPDD+module card)_TX7_L10
		Tx7_L23	112G_16dB_(QSFPDD+module card)_TX7_L23
		Tx3_L10	112G_16dB_(QSFPDD+module card)_TX3_L10
		Tx3_L23	112G_16dB_(QSFPDD+module card)_TX3_L23
		Tx7_Asic	112G_16dB_(QSFPDD+module card)_TX7_Asic
		Tx3_Asic	112G_16dB_(QSFPDD+module card)_TX3_Asic
lim_3ck_adhoc_01_073119	lim_3ck_adhoc_02_073119.zip	Ch5a_2"	Channel5a_Smaller_Pad_2inch_trace
		Ch5b_3"	Channel5b_Smaller_Pad_3inch_trace
		Ch5c_4"	Channel5c_Smaller_Pad_4inch_trace
		Ch5d_9"	Channel5d_Smaller_Pad_9inch_trace
akinwale_3ck_adhoc_01a_08282019	akinwale_3ck_C2M_channels_TP0a_100ohms_08222019.zip	2''100Ohm	C2M_2p0in_100Ohm_thru1.s4p
		3''100Ohm	C2M_3p0in_100Ohm_thru1.s4p
		4''100Ohm	C2M_4p0in_100Ohm_thru1.s4p
	akinwale_3ck_C2M_channels_TP0a_85ohms_08222019.zip	2''85Ohm	C2M_2p0in_85Ohm_thru1.s4p
		3''85Ohm	C2M_3p0in_85Ohm_thru1.s4p
		4''85Ohm	C2M_4p0in_85Ohm_thru1.s4p
	akinwale_3ck_C2M_channels_TP0a_93Ohms_08222019.zip	2''93Ohm	C2M_2p0in_93Ohm_thru1.s4p
		3''93Ohm	C2M_3p0in_93Ohm_thru1.s4p
		4''93Ohm	C2M_4p0in_93Ohm_thru1.s4p

COM Settings – Whole Link

Table 93A-1 parameters					I/O control				Table 93A3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_KR_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 0.85e-4]	nF	[TX RX]		SAVE_FIGURES	1	logical				
L_s	[0.12, 0.12]	nH	[TX RX]		Port Order	[2 1 4 3]			Table 92E2 parameters 5.2dB at 26.56GHz		
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]		RUNTAG	KR_eval_			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	1.286 dB/in or 0.0506 dB/mm at 100 ohms
z_p (TX)	[12 16; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 5; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[12 16; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	102.7	mm
z_p (RX)	[2 5; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	102.7	mm
C_p	[0.87e-4 0.65e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	102.7	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	102.7	mm
R_d	[50 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.39	V	vp/vf=.694		TDR and ERL options						
A_fe	0.39	V	vp/vf=.694		TDR	1	logical		Floating Tap Control		
A_ne	0.578	V			ERL	1	logical		N_bg	0	0 1 2 or 3 groups
L	4				ERL_ONLY	0	logical		N_bf	0	taps per group
M	32				TR_TDR	0.01	ns		N_f	40	UI span for floating taps
filter and Eq					N	3000			bmaxg	0.2	max DFE value for floating taps
f_r	0.75	*fb			beta_x	2.53E+09					
c(0)	0.54		min		rho_x	0.25					
c(-1)	[-0.26:0.02:0]		[min:step:max]		fixture delay time	0	s				
c(-2)	[0:0.02:0.10]		[min:step:max]		TDR_W_TXPKG	1					
c(-3)	[-0.04:0.02:0]		[min:step:max]		N_bx	24	UI		yellow indicates WIP		
c(1)	[-0.2:0.05:0]		[min:step:max]		Receiver testing						
N_b	4	UI			RX_CALIBRATION	0	logical				
b_max(1)	0.5				Sigma BBN step	5.00E-03	V				
b_max(2..N_b)	0.2				Noise, jitter						
g_DC	[-14:1:0]	dB	[min:step:max]		sigma_RJ	0.01	UI				
f_z	21.25	GHz			A_DD	0.02	UI				
f_p1	21.25	GHz			eta_0	8.20E-09	V^2/GHz				
f_p2	53.125	GHz			SNR_TX	33	dB				
g_DC_HP	[-3:1:0]		[min:step:max]		R_LM	0.95					
f_HP_PZ	0.6640625	GHz									

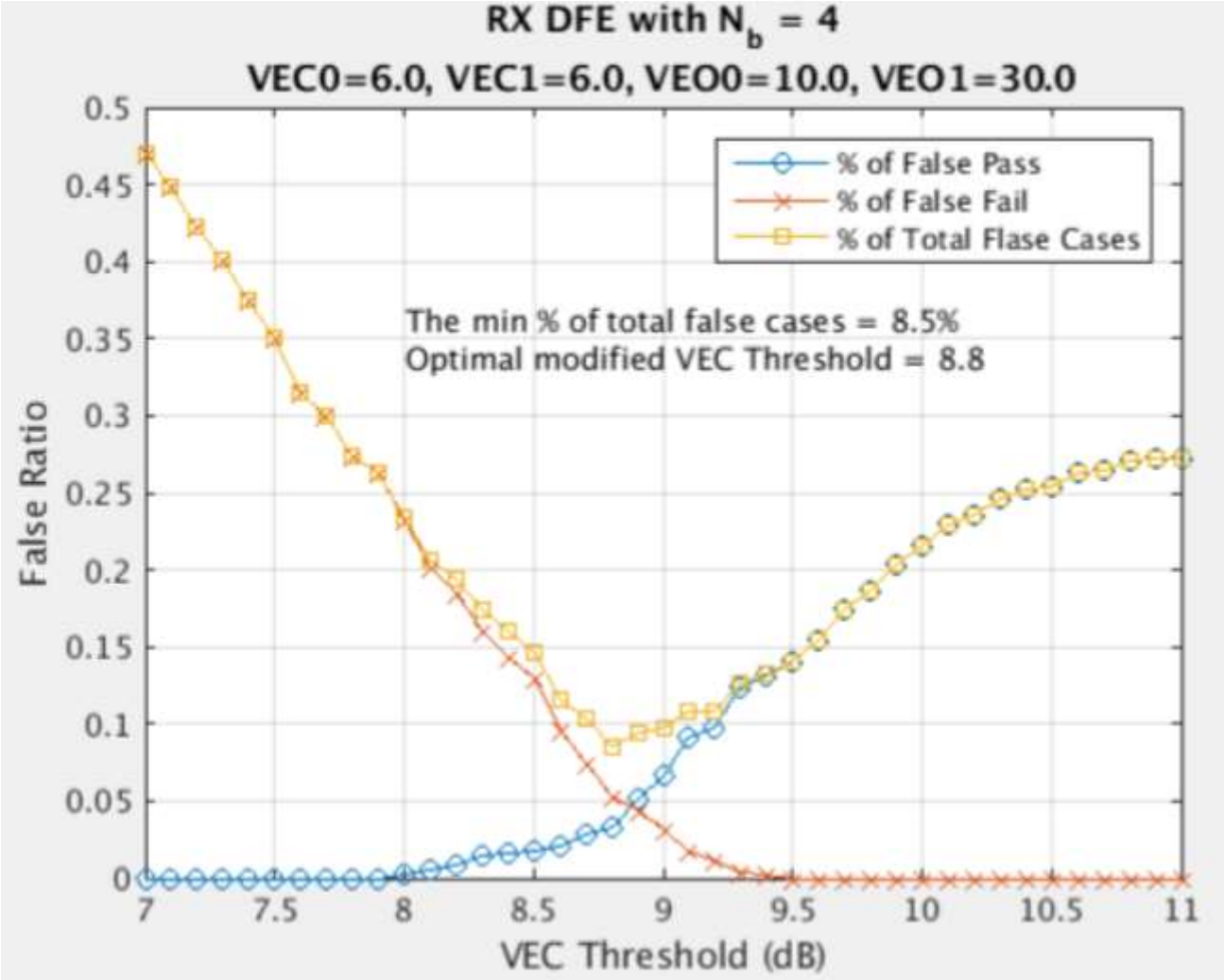
PS: Ran for test case 2 only

COM Settings – TP1a

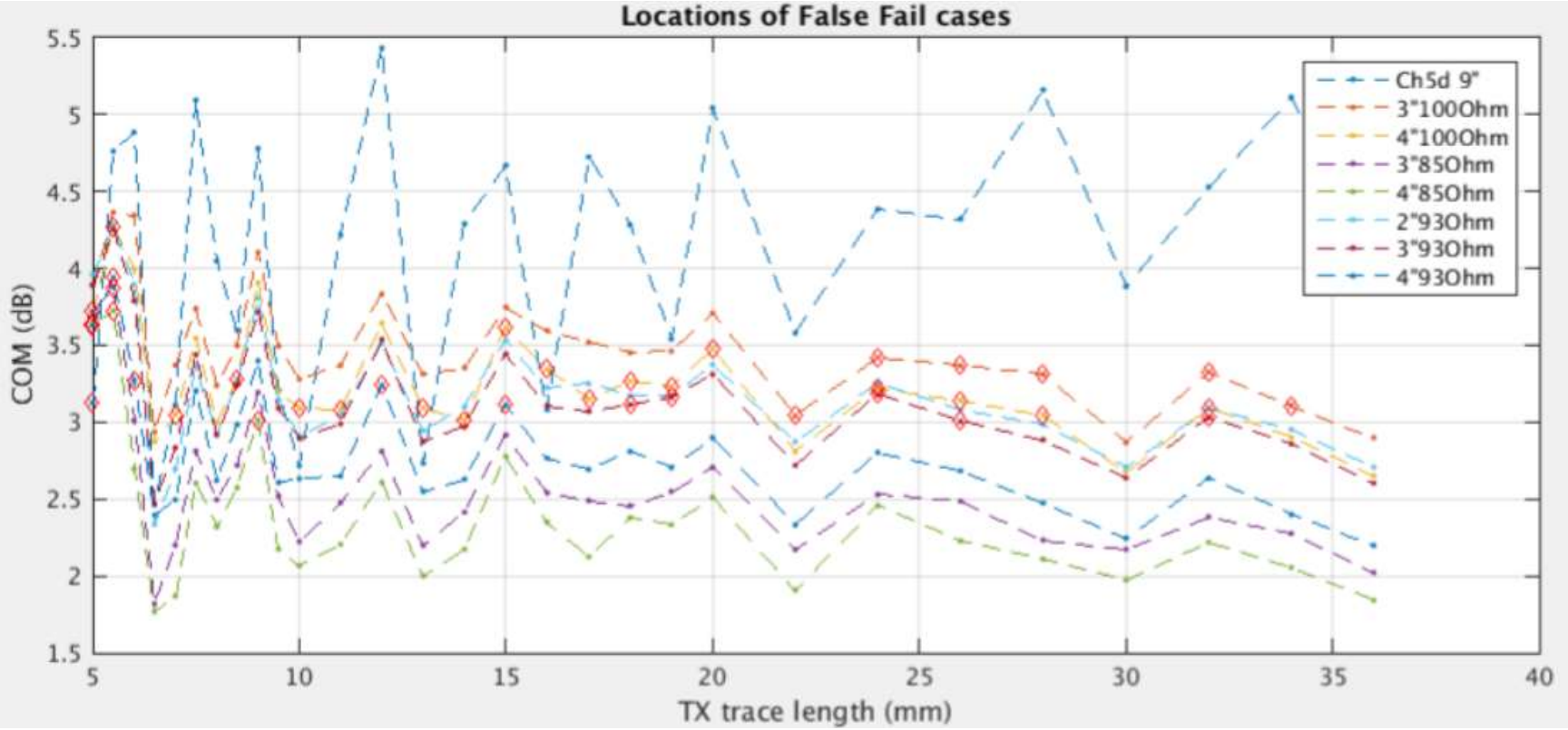
Table 93A-1 parameters					I/O control				Table 93A~~3~~ parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_KR_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 0]	nF	[TX RX]		SAVE_FIGURES	1	logical				
L_s	[0.12, 0]	nH	[TX RX]		Port Order	[2 1 4 3]			Table 92~~1~~2 parameters 5.2dB at 26.56GHz		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	KR_eval_			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	1.286 dB/in or 0.0506 dB/mm at 100 ohms
z_p (TX)	[12 16; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[12 16; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	102.7	mm
z_p (RX)	[0 0; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	102.7	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	102.7	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	102.7	mm
R_d	[50 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.39	V	vp/vf=.694		TDR and ERL options						
A_fe	0.39	V	vp/vf=.694		TDR	1	logical		Floating Tap Control		
A_ne	0.578	V			ERL	1	logical		N_bg	0	0 1 2 or 3 groups
L	4				ERL_ONLY	0	logical		N_bf	0	taps per group
M	32				TR_TDR	0.01	ns		N_f	40	UI span for floating taps
filter and Eq					N	3000			bmaxg	0.2	max DFE value for floating taps
f_r	0.75	*fb			beta_x	2.53E+09					
c(0)	0.54		min		rho_x	0.25					
c(-1)	[-0.26:0.02:0]		[min:step:max]		fixture delay time	0	s				
c(-2)	[0:0.02:0.10]		[min:step:max]		TDR_W_TXPKG	1					
c(-3)	[-0.04:0.02:0]		[min:step:max]		N_bx	24	UI		yellow indicates WIP		
c(1)	[-0.2:0.05:0]		[min:step:max]		Receiver testing						
N_b	4	UI			RX_CALIBRATION	0	logical				
b_max(1)	0.5				Sigma BBN step	5.00E-03	V				
b_max(2..N_b)	0.2				Noise, jitter						
g_DC	[-14:1:0]	dB	[min:step:max]		sigma_RJ	0.01	UI				
f_z	21.25	GHz			A_DD	0.02	UI				
f_p1	21.25	GHz			eta_0	8.20E-09	V^2/GHz				
f_p2	53.125	GHz			SNR_TX	33	dB				
g_DC_HP	[-3:1:0]		[min:step:max]		R_LM	0.95					
f_HP_PZ	0.6640625	GHz									

PS: Ran for test case 2 only

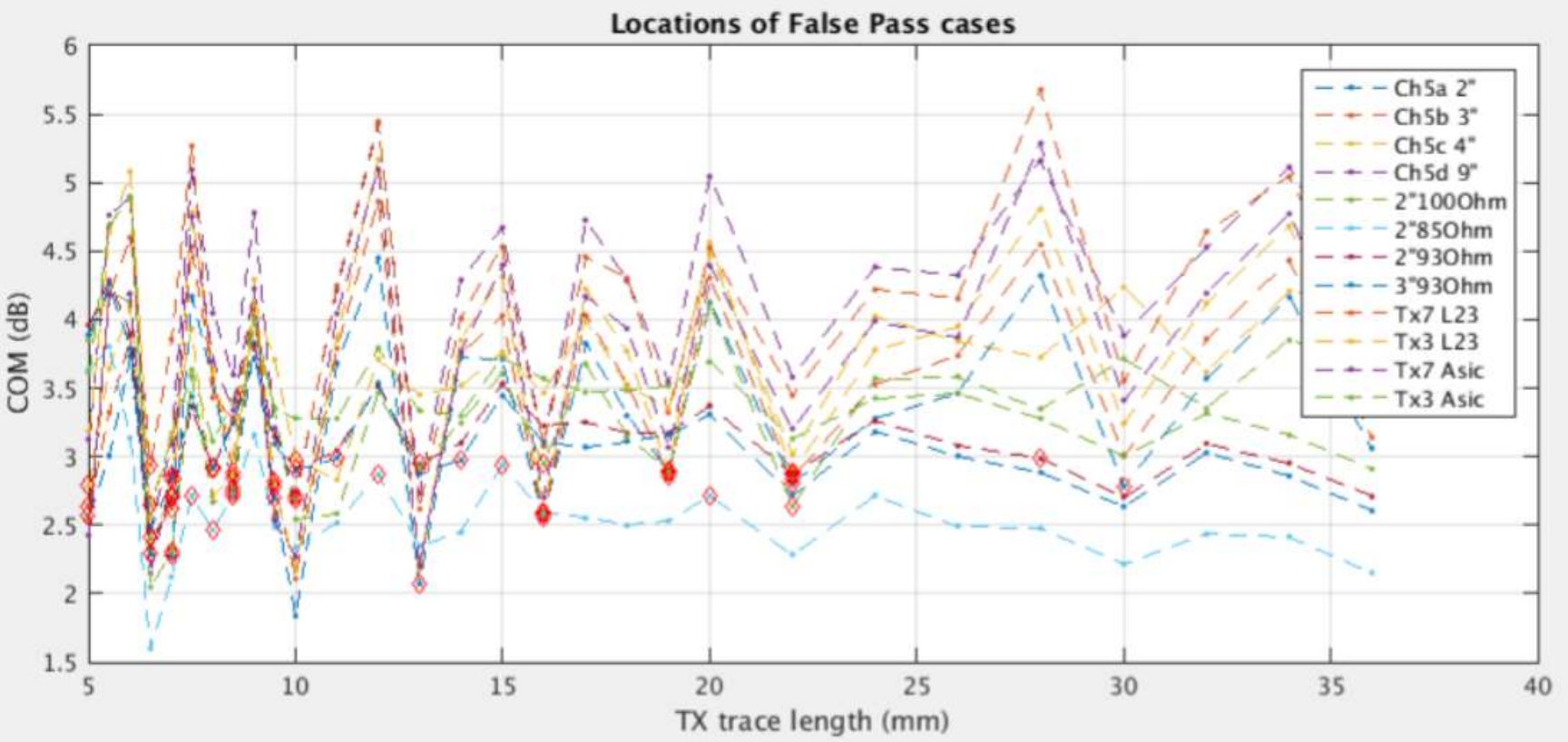
Trade off False Ratios by VEC Threshold



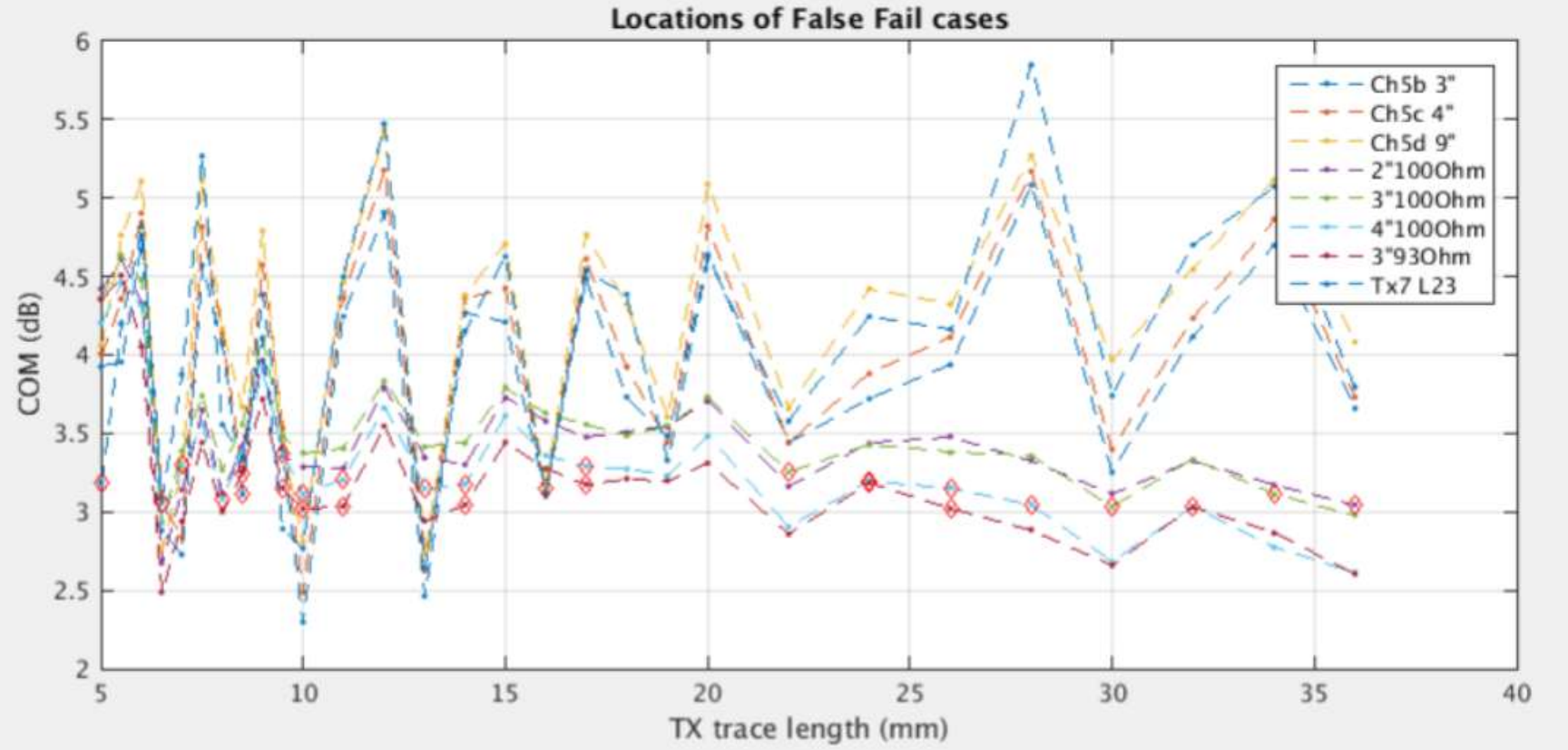
Locations of False Fail Cases – N_b = 3
VEC1 – VEC0 = 2.5



Locations of False Pass Cases – N_b = 3 VEC1 – VEC0 = 2.5



Locations of False Fail Cases – N_b = 4 VEC1-VEC0 = 0



Locations of False Pass Cases – N_b = 4 VEC1-VEC0 = 0