Host to Module Short Channel Issue – Channels Comparison

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IEEE 802.3ck Task Force

Outline

- Channels and COM settings
- Whole-Link Analysis – Comparison
  - COM, ERL, ICN
  - TDR and SBR
- Possible Improvement on Channels
- Summary

Channels and COM Settings

- Channel and reference receiver
  - Whole-link & TP1a analysis for 12 IEEE C2M host-to-module channels
    - 2-in, 3-in, & 4-in channels
    - Three channels from Cisco/Jane in 2019/July
    - Nine channels from Intel/Femi in 2019/Aug
      - Three different PCB impedance: 100 Ohm, 93 Ohm, 85 Ohm
    - Sweep host package trace length, z_p1(TX)
      - z_p1(TX) = [5:0.5:10 11:1:20 22:2:36]
  - DFE with 4 taps
- COM parameter settings [details in appendix]
  - COM 2.75
  - Whole link: TX PKG + H2M Channels + RX PKG
    - On-die
      - Host [healey_3ck_adhoc_01_061219]
      - Module: Table 1
    - PKG
      - Host [baseline]
      - Module: Table 1
    - g_DC = [-14:1:0] dB
    - g_DC_HP = [-3:1:0] dB
  - TP1a: TX PKG + H2M Channels
    - Set 'zero' to related RX PKG & on-die settings

Table 1

Spec	[Host, Module]	Unit
C_d	[1.2e-4 0.85e-4]	nF
L_s	[0.12 0.12]	nH
C_b	[0.3e-4 0.3e-4]	nF
R_d	[50 50]	Ohm
C_p	[0.87 0.65]	nF
z_p(RX)	[5 0]	Ohm

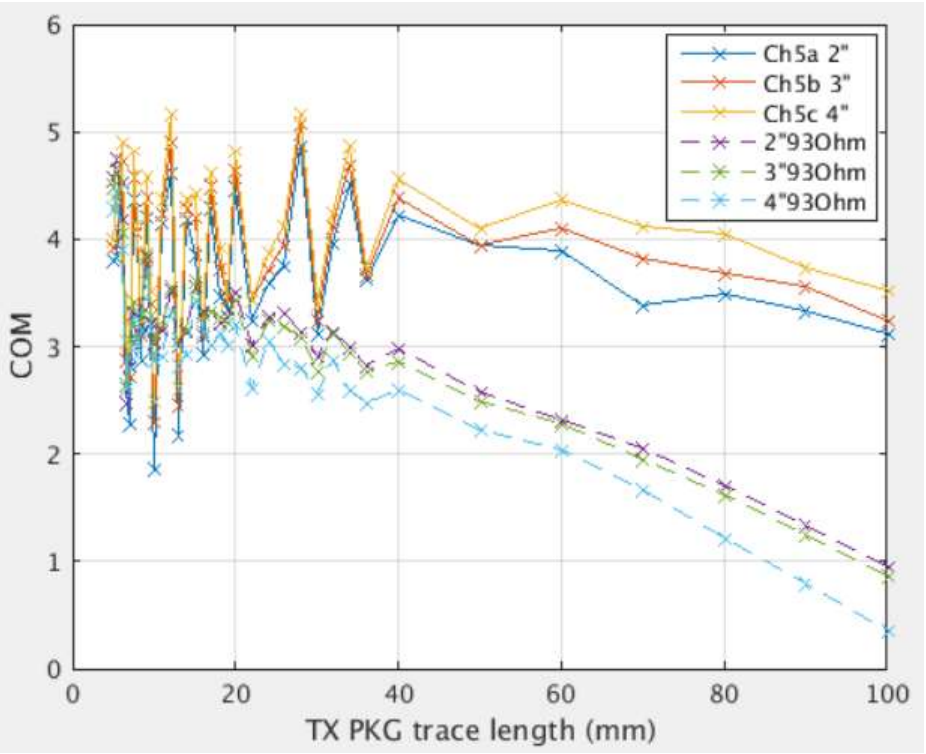
Comparison Items – Whole Link

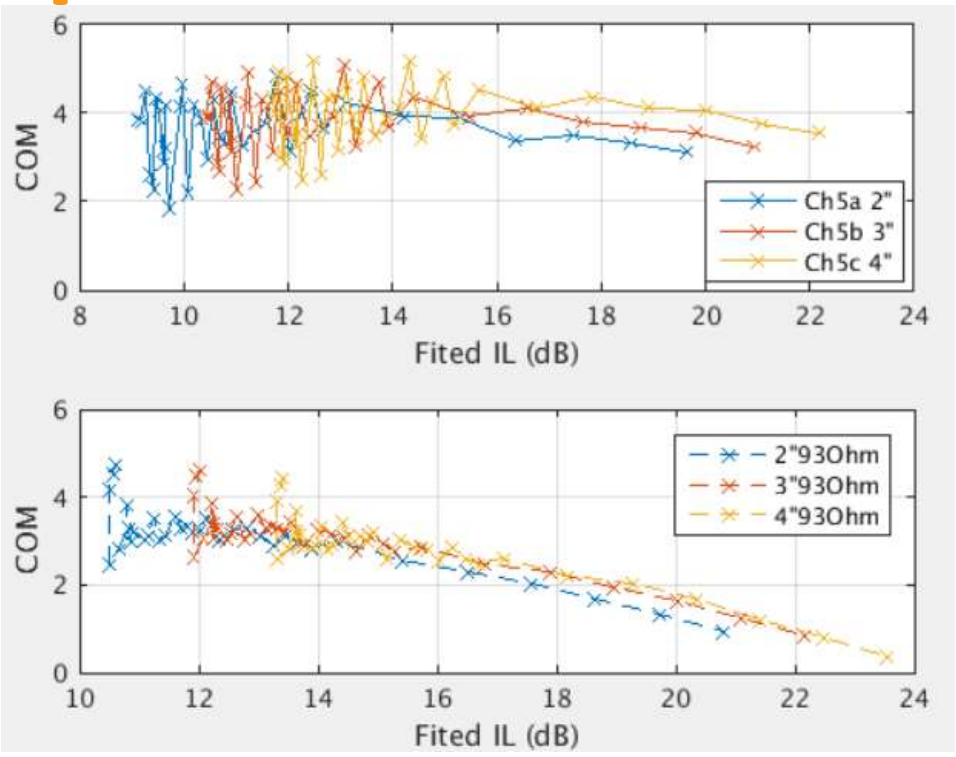
- Compare the following two channel sets

Contribution	Channel
lim_3ck_adhoc_01_073119	Ch5a_2"
	Ch5b_3"
	Ch5c_4"
akinwale_3ck_adhoc_01a_082820 19	2''93Ohm
	3''93Ohm
	4"93Ohm

- Observed parameters
  - Fit_IL = Fitted IL with package (bump-to-bump) at Nyquist frequency
  - COM, ERL, ICN
  - FOM noise distributions

COM Comparisons

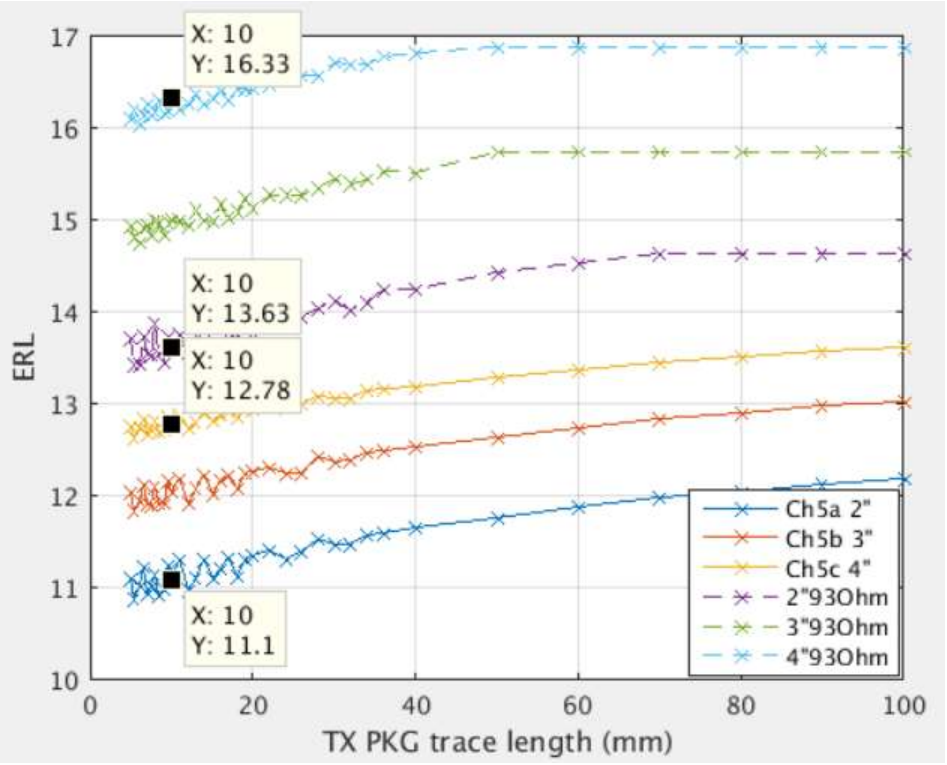


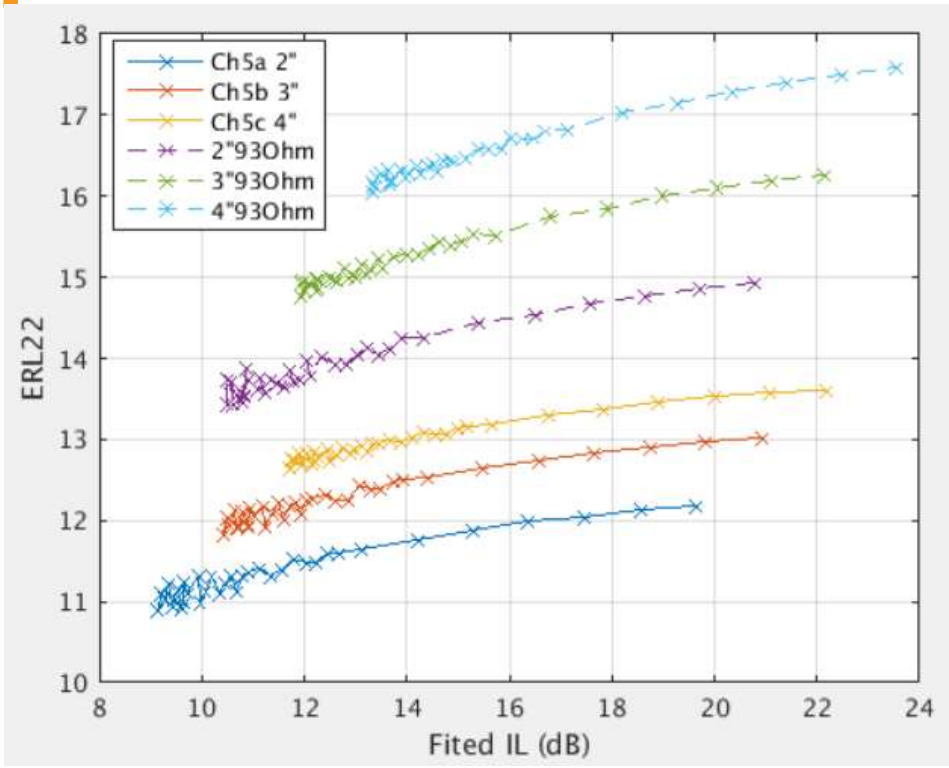


- COM degrades by increasing TX PKG trace length
  - Obviously for Femi's channel set
  - Not so obvious for Jane's channel set
  - Femi's set: longer PCB trace, worse COM

- Observing COM vs. IL – decreasing by larger IL
  - Obviously for Femi's channel set after TX PKG trace length >= 13 mm & IL >= 14 dB
  - Not so obvious for Jane's channel set, only TX PKG length >= 40 mm & IL >= 18 dB
  - Why?

ERL Comparisons



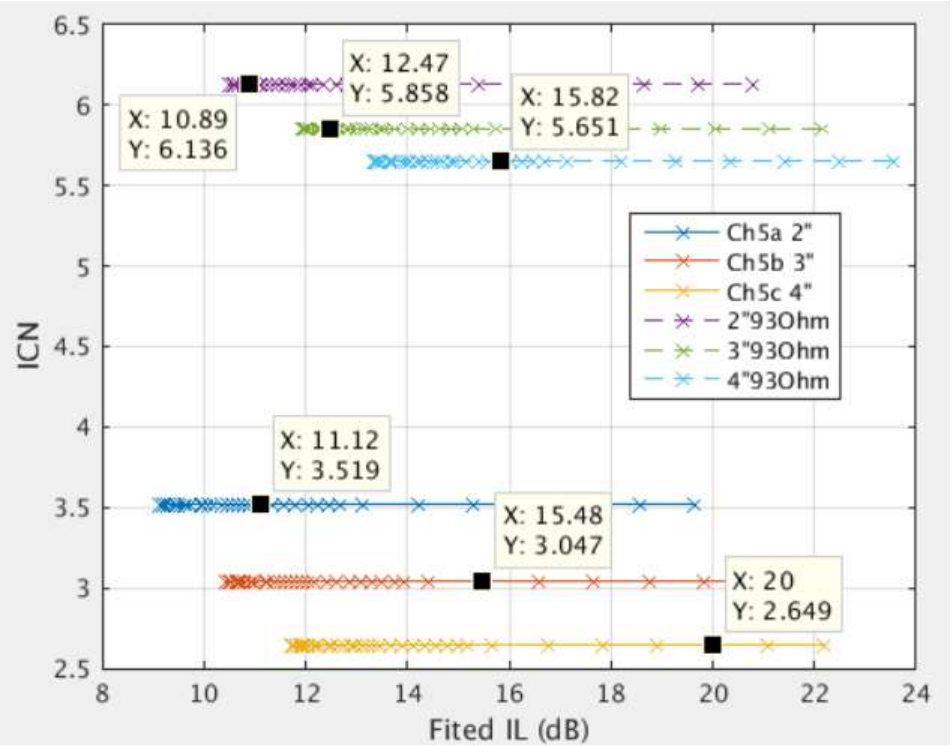


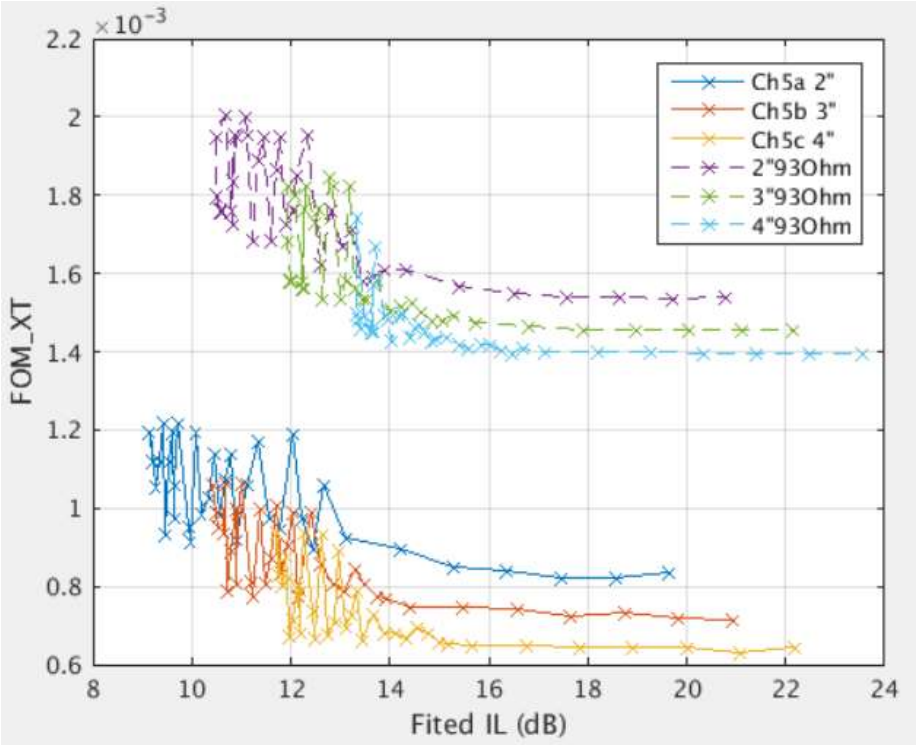
- ERL11 are similar & higher than ERL22
- ERL22
  - Jane's set have 2 ~ 3 dB smaller than Femi's set
- Q: is it possible to improve ERL22?

ERL11 (dB)

Channel Set	2"	3"	4"
Lim19Jul	14.08	15.45	16.62
Femi19Aug	14.65	15.75	16.88

ICN (mV) Comparisons





ICN (mV)			
Channel Set	**2”**	**3”**	**4”**
Lim19Jul	3.52	3.05	2.65
Femi19Aug	6.14	5.86	5.65

- Jane’s set have much smaller ICN (mV) than Femi’s
  - Jane: 2.65 ~ 3.52 mV
  - Femi’s: 5.65 ~ 6.14 mV, nearly double
  - Q: Is it possible to improve ICN of Femi’s channels?

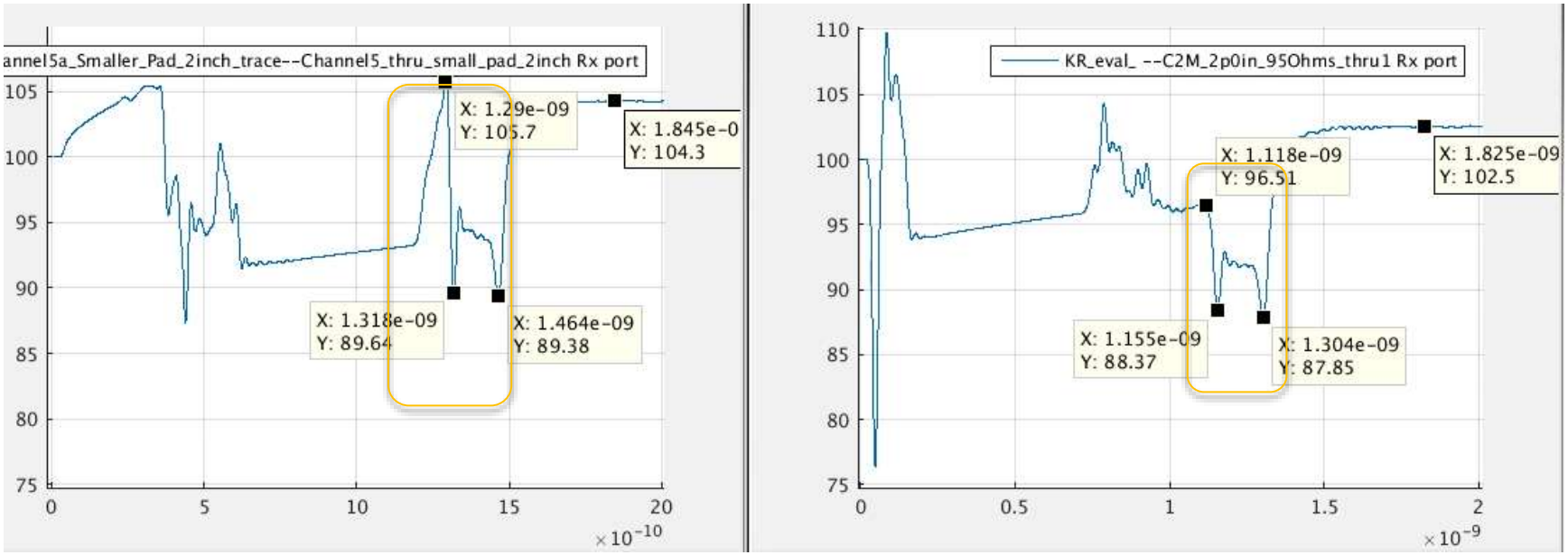
Channel Parameters Comparison

PCB length	2”		3”		4”	
Channel Set	Jane	Femi	Jane	Femi	Jane	Femi
Fitted IL (dB)	9.7	11.1	11.1	12.5	12.5	13.9
ILD (dB)	0.14	0.35	0.15	0.36	0.16	0.36
ICN (mV)	3.52	6.14	3.05	5.86	2.65	5.65
ERL11 (dB)	14.08	14.65	15.45	15.75	16.62	16.88
ERL (dB)	11.1	12.78	12.0	15.0	13.63	16.33

PS: 1. Show values of TX ZP1 = 10 mm
2. The fitted IL is bump-to-bump

- Possible improvements in Jane’s channels – root cause for COM’s sensitivity to TX PKG trace length
  - Smaller ERL due to ‘impedance discontinuous junction’ between ASIC foot-print and ‘C_p’ in PKG
  - Short channel issue may be mitigated after channel improvement
- Possible improvements in Femi’s channels
  - Reduce IL and crosstalk

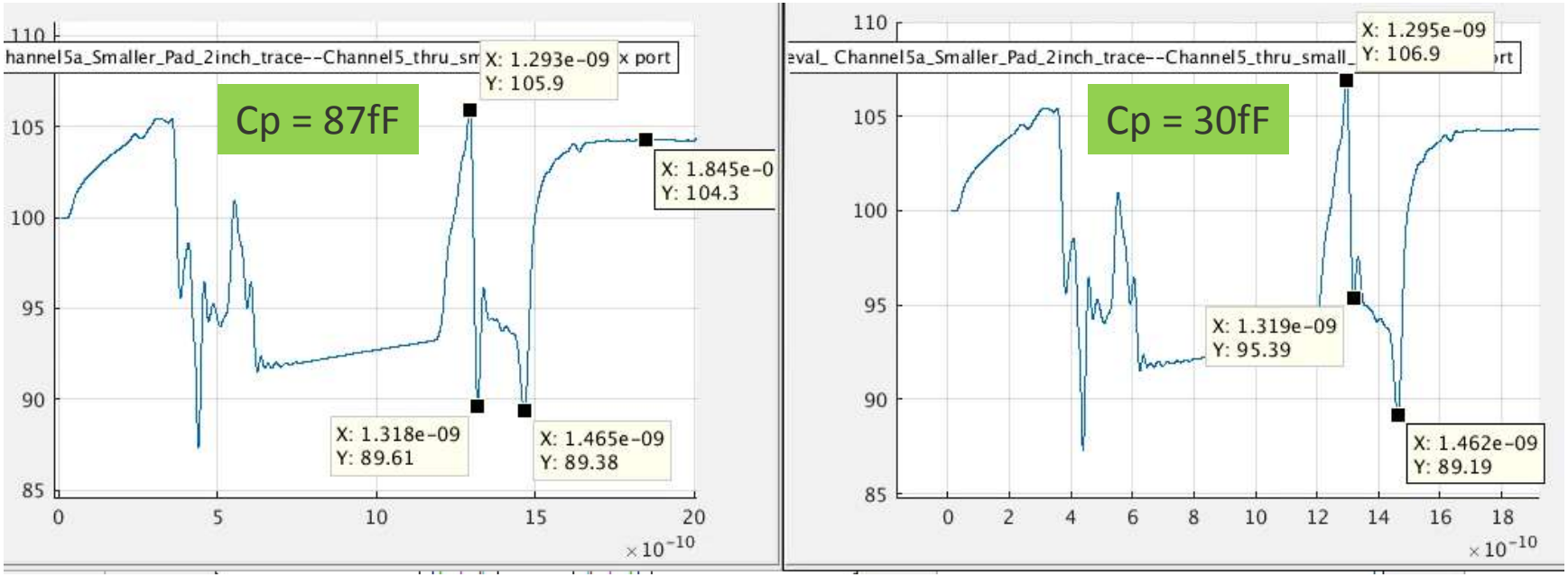
Ch5a_2in vs. 2in_93Ohm : 10mm, TDR RX



- Two impedance discontinuity junctions in Jane's channel cause reflection around 9th post-cursor
  - Left-handed side is junction of ASIC foot print & 'C_p' → is it possible to reduce impedance of "ASIC foot print"?
  - Right-handed side: "on-die" and "C_b"
- Impedance of "ASIC foot print" is closer to 'C_p' → better ERL22
  - Not so sensitive to TX PKG trace length

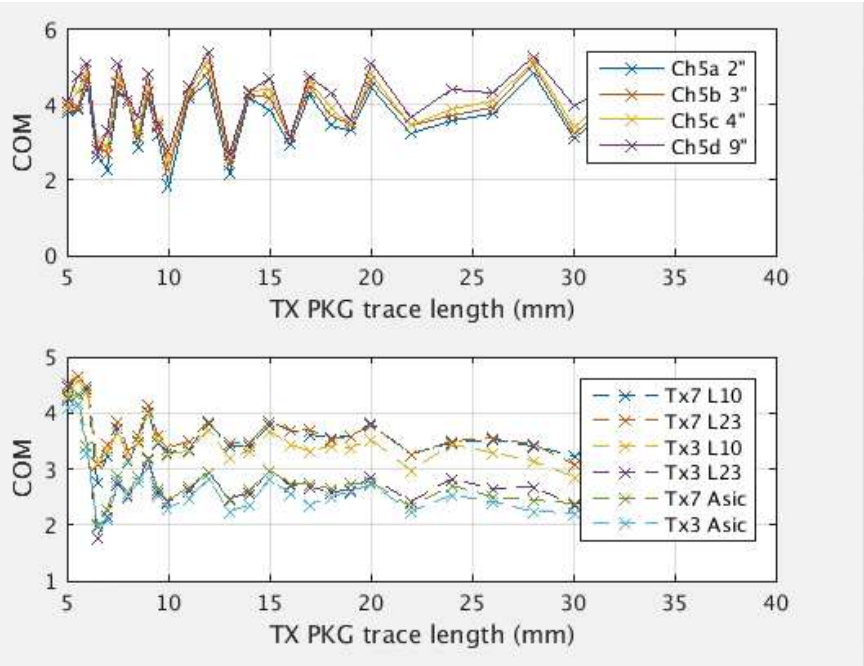
Observe SBRs

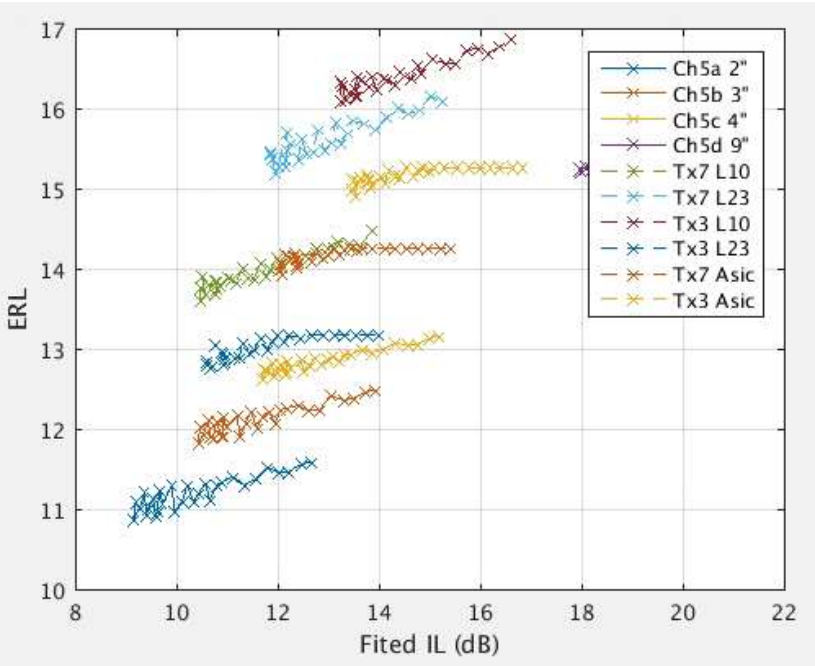
Improve ERL by reducing C_p



- The discontinuous junction of impedance from ASIC BGA footprint to PKG C_p is obviously reduced when C_p is reducing from 87fF to 30fF
  - It doesn't mean that we can reduce C_p in COM or real PKG design
  - This is just the experiment to observe the COM & ERL impact if we improve impedance matching
- Evaluate the gain by improving the impedance discontinuity at host-side C_p [106 Ohm vs. 90 Ohm]
  - Experiments: by reducing C_p from 87fF
  - PS: the feasible solution shall be taken by reducing impedance of ASIC BGA footprint

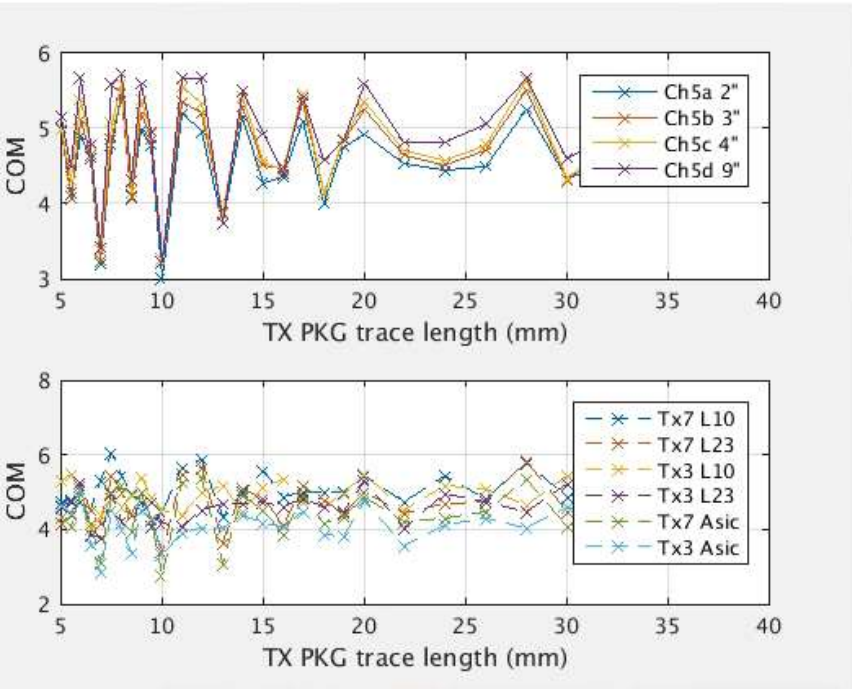
COM & ERL: Original C_p = 87fF

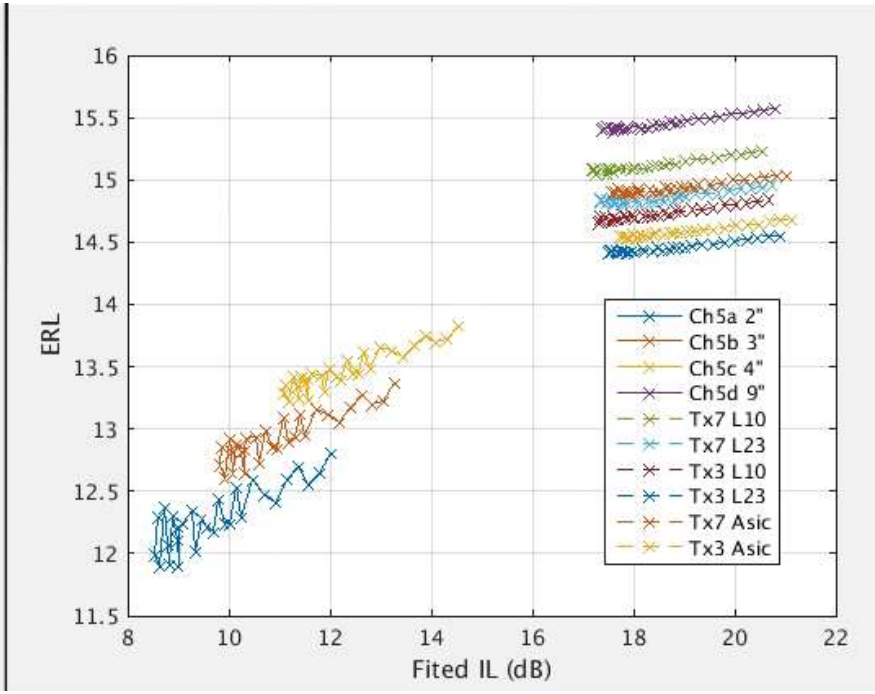




- Check whether "short channel issue" had been solved by this improvement
  - Check both of Lim_2019_Jul (short) & Lim_2019_Mar (long) channels
  - Check COM & ERL
- This is the original results
  - Short channels have COM values ranging from 2.0 to 5.0 dB
  - Long channels have COM value as low as 1.8 dB
  - ERL of short channels are as low as 11 dB for 2in case

COM & ERL: Reducing C_p to 35fF





- By reducing C_p, ERL & COM improves, but COM still fluctuates a lot
  - Most of channels are with ERL > 12 dB
  - Channels under all TX PKG trace length > 3 dB
  - It seems that C2M channel design need to consider all possible TX PKG trace lengths to make sure the impact from 'short channel effect' can be tolerant

Summary

- Exploring H2M ‘short channel issue’ for channels of Jane and Femi
- Jane’s is more sensitive to TX PKG trace length
  - Root cause is the big impedance discontinuity among ASIC BGA footprint & TX PKG
  - Improve impedance matching will improve COM & ERL in general, but don’t mitigate “short channel issue”
  - However, it still deserve to improve “impedance matching”
- Femi’s is more sensitive to host trace length & have worse COM in general, due to
  - Larger IL & ICN
  - However, the short channel issue is less sever

Call to Action

- C2M short channel improvement
  - Jane's
    - Improve ASIC BGA footprint impedance matching with Host PKG impedance
  - Femi's
    - Improve IL & ICN
  - After channel improvement, the impact from "short channel" effect is reduced
  - We may only require simple reference RX as 4-tap DFE or 5-tap FFE
- Make sure TP1a spec to cover short channel issue
  - Whether VEC & Eye height, Eye width are enough?
  - Can ERL help?

everyday genius

COM Settings – Whole Link

Table 93A-1 parameters					I/O control				Table 93A3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_KR_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 0.85e-4]	nF	[TX RX]		SAVE_FIGURES	1	logical				
L_s	[0.12, 0.12]	nH	[TX RX]		Port Order	[2 1 4 3]			Table 92E2 parameters 5.2dB at 26.56GHz		
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]		RUNTAG	KR_eval_			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	1.286 dB/in or 0.0506 dB/mm at 100 ohms
z_p (TX)	[12 16; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[2 5; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[12 16; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	102.7	mm
z_p (RX)	[2 5; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	102.7	mm
C_p	[0.87e-4 0.65e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	102.7	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	102.7	mm
R_d	[50 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.39	V	vp/vf=.694		TDR and ERL options						
A_fe	0.39	V	vp/vf=.694		TDR	1	logical		Floating Tap Control		
A_ne	0.578	V			ERL	1	logical		N_bg	0	0 1 2 or 3 groups
L	4				ERL_ONLY	0	logical		N_bf	0	taps per group
M	32				TR_TDR	0.01	ns		N_f	40	UI span for floating taps
filter and Eq					N	3000			bmaxg	0.2	max DFE value for floating taps
f_r	0.75	*fb			beta_x	2.53E+09					
c(0)	0.54		min		rho_x	0.25					
c(-1)	[-0.26:0.02:0]		[min:step:max]		fixture delay time	0	s				
c(-2)	[0:0.02:0.10]		[min:step:max]		TDR_W_TXPKG	1					
c(-3)	[-0.04:0.02:0]		[min:step:max]		N_bx	24	UI		yellow indicates WIP		
c(1)	[-0.2:0.05:0]		[min:step:max]		Receiver testing						
N_b	4	UI			RX_CALIBRATION	0	logical				
b_max(1)	0.5				Sigma BBN step	5.00E-03	V				
b_max(2..N_b)	0.2				Noise, jitter						
g_DC	[-14:1:0]	dB	[min:step:max]		sigma_RJ	0.01	UI				
f_z	21.25	GHz			A_DD	0.02	UI				
f_p1	21.25	GHz			eta_0	8.20E-09	V^2/GHz				
f_p2	53.125	GHz			SNR_TX	33	dB				
g_DC_HP	[-3:1:0]		[min:step:max]		R_LM	0.95					
f_HP_PZ	0.6640625	GHz									

PS: Ran for test case 2 only

COM Settings – TP1a

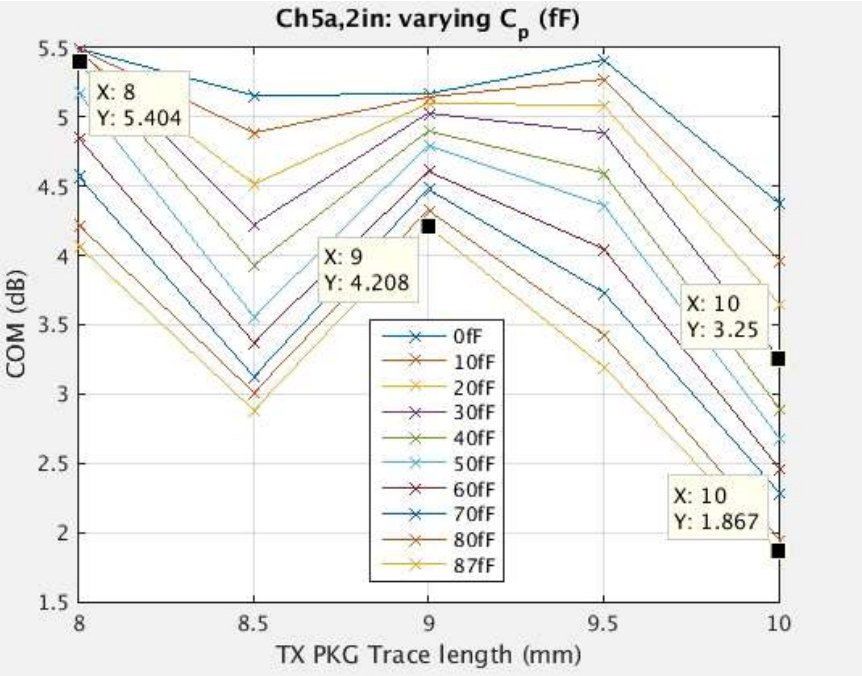
Table 93A-1 parameters					I/O control				Table 93A~~3~~ parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\results\100GEL_KR_{date}\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 0]	nF	[TX RX]		SAVE_FIGURES	1	logical				
L_s	[0.12, 0]	nH	[TX RX]		Port Order	[2 1 4 3]			Table 92~~1~~2 parameters 5.2dB at 26.56GHz		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	KR_eval_			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	1.286 dB/in or 0.0506 dB/mm at 100 ohms
z_p (TX)	[12 16; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	6.200E-03	ns/mm
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[12 16; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10	dB		z_bp (TX)	102.7	mm
z_p (RX)	[0 0; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	102.7	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	102.7	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	102.7	mm
R_d	[50 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.39	V	vp/vf=.694		TDR and ERL options						
A_fe	0.39	V	vp/vf=.694		TDR	1	logical		Floating Tap Control		
A_ne	0.578	V			ERL	1	logical		N_bg	0	0 1 2 or 3 groups
L	4				ERL_ONLY	0	logical		N_bf	0	taps per group
M	32				TR_TDR	0.01	ns		N_f	40	UI span for floating taps
filter and Eq					N	3000			bmaxg	0.2	max DFE value for floating taps
f_r	0.75	*fb			beta_x	2.53E+09					
c(0)	0.54		min		rho_x	0.25					
c(-1)	[-0.26:0.02:0]		[min:step:max]		fixture delay time	0	s				
c(-2)	[0:0.02:0.10]		[min:step:max]		TDR_W_TXPKG	1					
c(-3)	[-0.04:0.02:0]		[min:step:max]		N_bx	24	UI		yellow indicates WIP		
c(1)	[-0.2:0.05:0]		[min:step:max]		Receiver testing						
N_b	4	UI			RX_CALIBRATION	0	logical				
b_max(1)	0.5				Sigma BBN step	5.00E-03	V				
b_max(2..N_b)	0.2				Noise, jitter						
g_DC	[-14:1:0]	dB	[min:step:max]		sigma_RJ	0.01	UI				
f_z	21.25	GHz			A_DD	0.02	UI				
f_p1	21.25	GHz			eta_0	8.20E-09	V^2/GHz				
f_p2	53.125	GHz			SNR_TX	33	dB				
g_DC_HP	[-3:1:0]		[min:step:max]		R_LM	0.95					
f_HP_PZ	0.6640625	GHz									

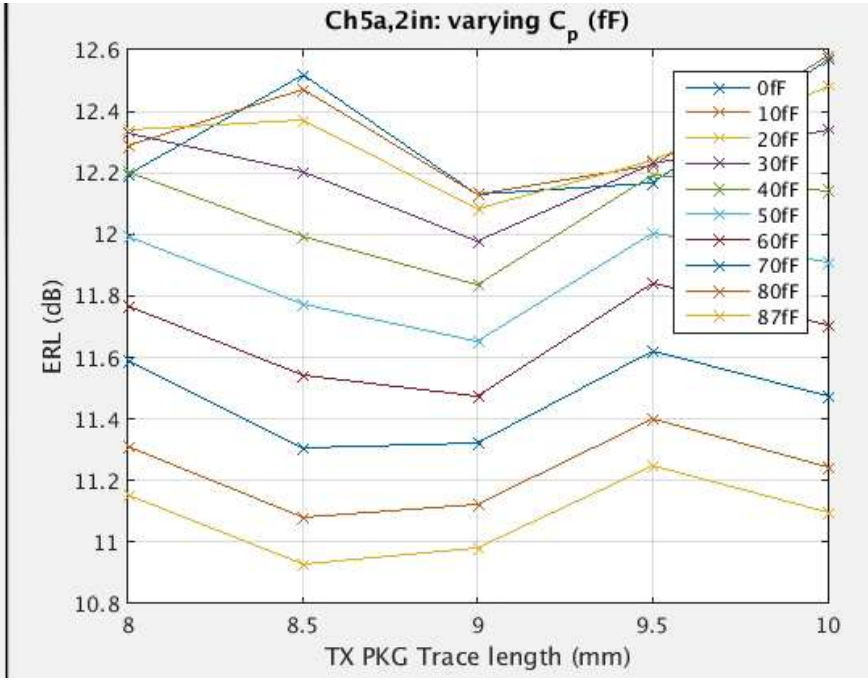
PS: Ran for test case 2 only

C2M Channels for Analysis

Contribution	Zip files	Channel	SxP Files
lim_3ck_adhoc_01_073119	lim_3ck_adhoc_02_073119.zip	Ch5a_2"	Channel5a_Smaller_Pad_2inch_trace
		Ch5b_3"	Channel5b_Smaller_Pad_3inch_trace
		Ch5c_4"	Channel5c_Smaller_Pad_4inch_trace
akinwale_3ck_adhoc_01a_08282019	akinwale_3ck_C2M_channels_TP0a_100ohms_08222019.zip	2''100Ohm	C2M_2p0in_100Ohm_thru1.s4p
		3''100Ohm	C2M_3p0in_100Ohm_thru1.s4p
		4''100Ohm	C2M_4p0in_100Ohm_thru1.s4p
	akinwale_3ck_C2M_channels_TP0a_85ohms_08222019.zip	2''85Ohm	C2M_2p0in_85Ohm_thru1.s4p
		3''85Ohm	C2M_3p0in_85Ohm_thru1.s4p
		4''85Ohm	C2M_4p0in_85Ohm_thru1.s4p
	akinwale_3ck_C2M_channels_TP0a_93Ohms_08222019.zip	2''93Ohm	C2M_2p0in_93Ohm_thru1.s4p
		3''93Ohm	C2M_3p0in_93Ohm_thru1.s4p
		4"93Ohm	C2M_4p0in_93Ohm_thru1.s4p

COM & ERL Improvements

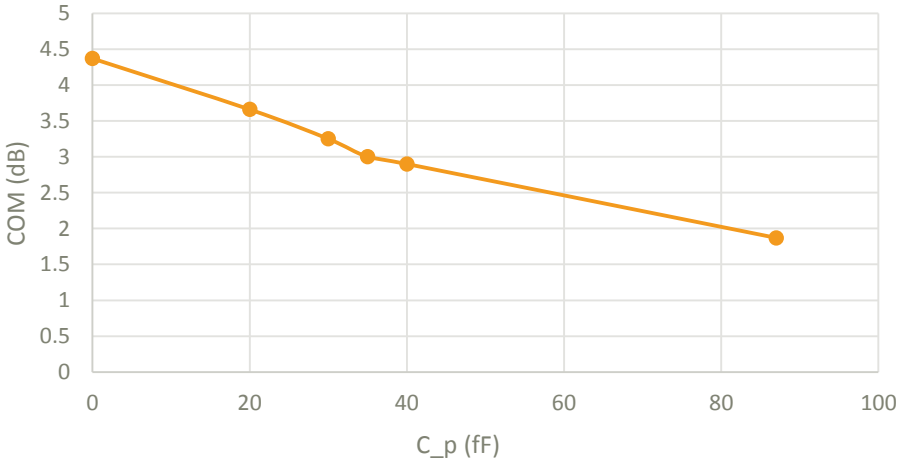




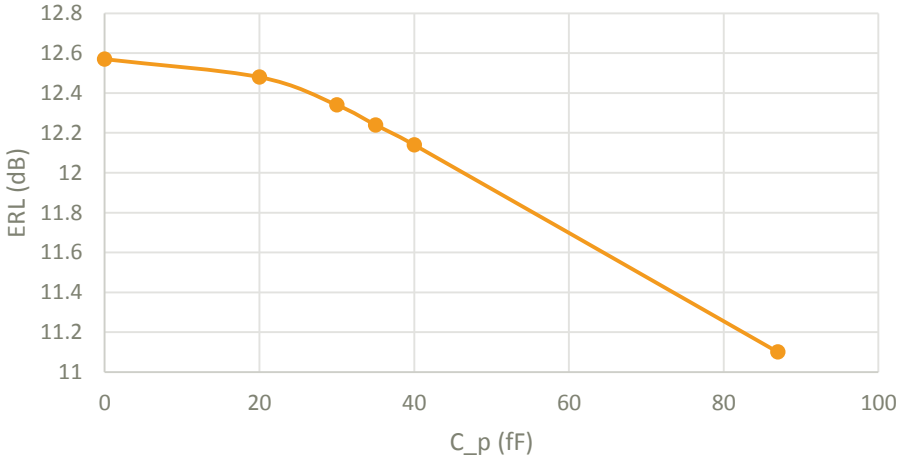
Ch5a_2in: Improvement Evaluation

- Evaluate the gain by improving the impedance discontinuity at host-side C_p [106 Ohm vs. 90 Ohm]
  - Experiments: by reducing C_p from 87fF
  - PS: the feasible solution shall be taken by reducing impedance of ASIC BGA footprint
- Results
  - COM improves when “impedance discontinuity” improves
  - ERL improves as well
  - When C_p = 35 fF, COM = 3.00 dB & ERL = 12.24 dB
  - ERL could be an indicator to check channel quality in impedance discontinuity

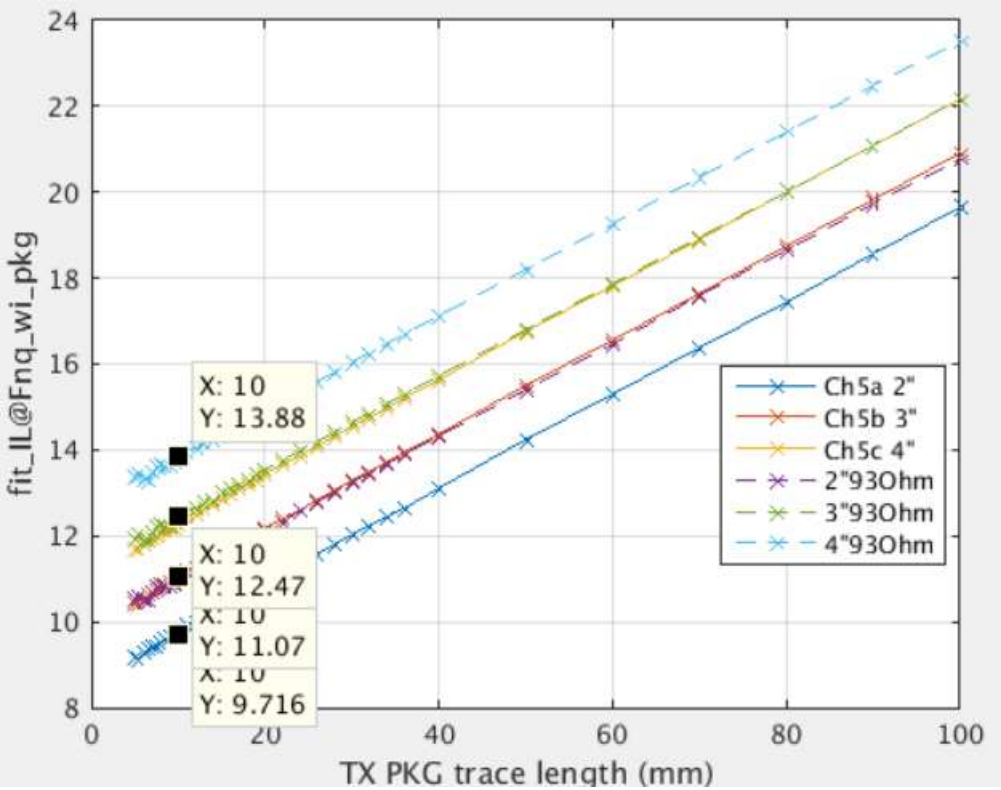
COM, 10mm



ERL, 10mm

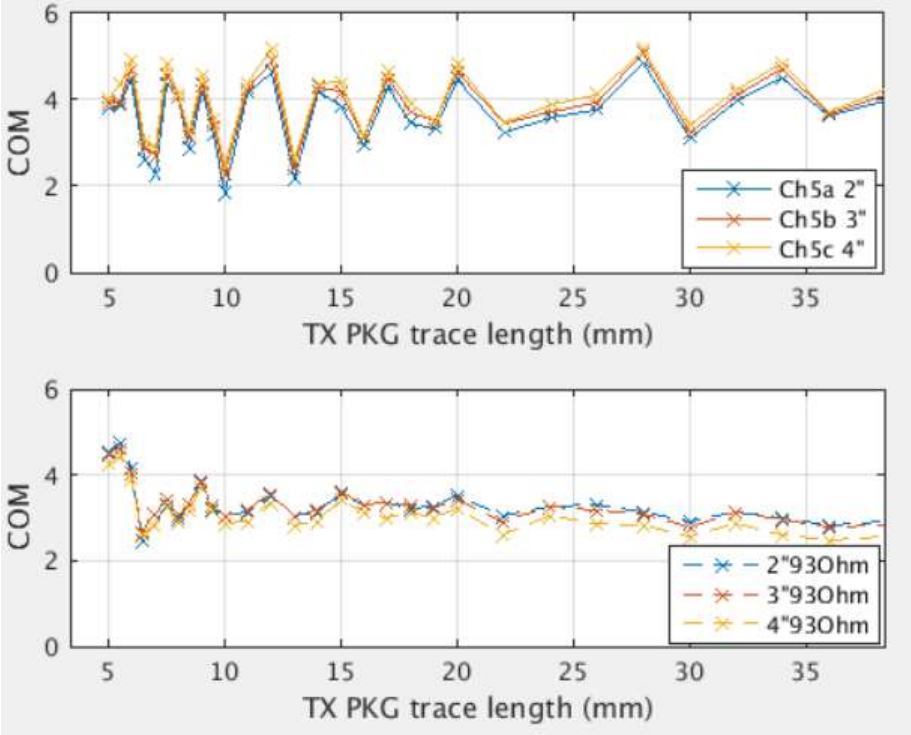


IL Comparisons



- Jane's channels have smaller IL than Femi's – comparing by the same host PCB trace length
  - IL differences of 2in: ~1.4 dB
  - 3in: ~1.4 dB
  - 4in: ~1.4 dB
- Both channel sets show that IL increases linearly by TX PKG trace length

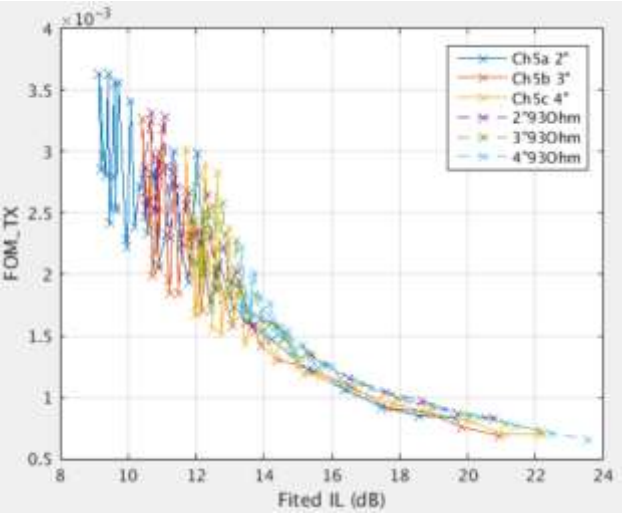
COM Comparisons

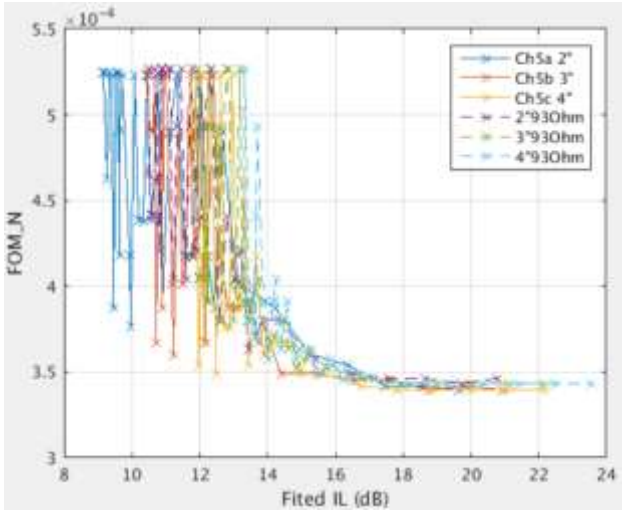


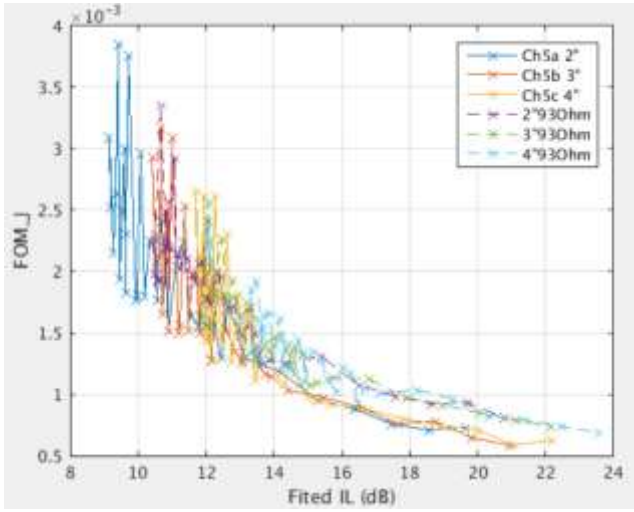
- Jane's channels are more sensitive to TX PKG trace length
  - > 2.0 dB in the range of 6 ~ 14 mm
  - Root cause?
  - Femi's channels: around 1 dB variation after 6.5 mm
- Next: observing SBR & TDR

FOM Analysis – Noise Distributions

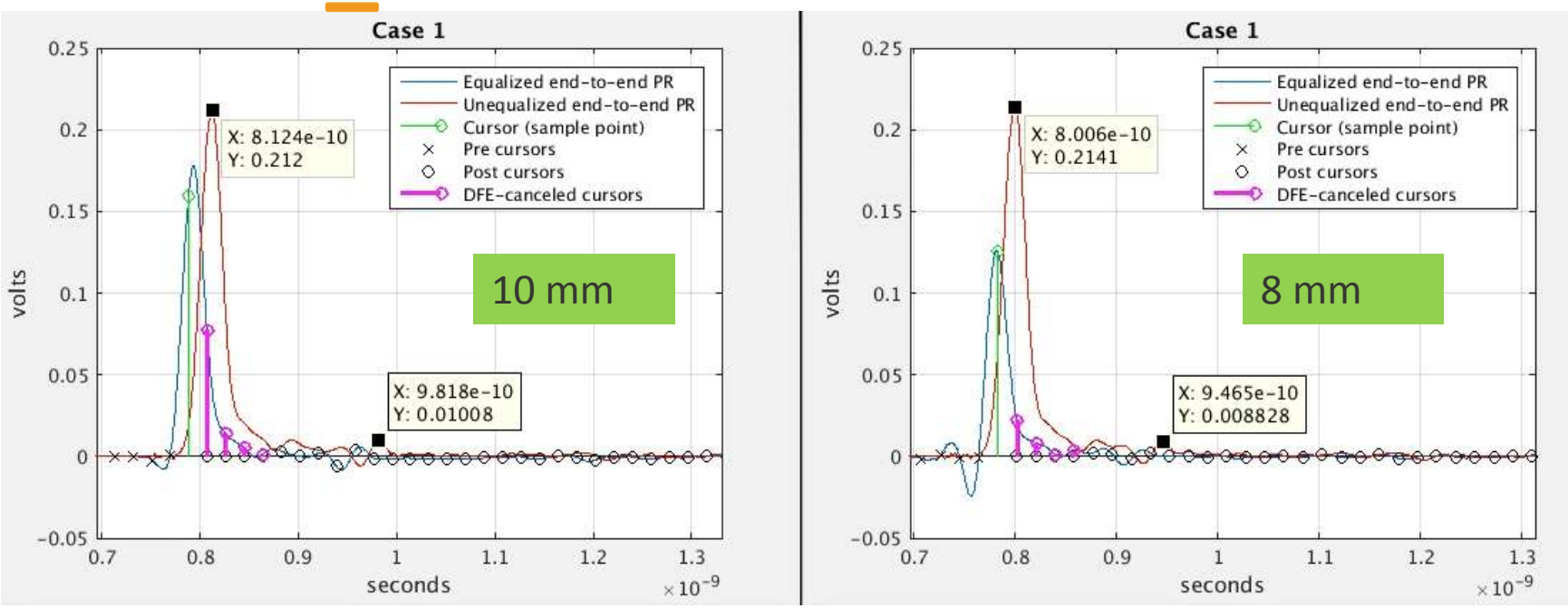
- For the following noise sources in FOM, they are similar in both channel sets
  - FOM_TX, FOM_N, FOM_J
  - They are all small values in FOM noise distribution







Ch5a_2in: SBR of 10mm vs. 8mm



- There is obvious reflection at 0.2 nS after main cursor in “Unequalized end-to-end PR” curve
  - No matter 10 mm or 8 mm cases
  - Majorly due to channel impedance mismatch to TX PKG
- Q: Is it possible to improve this?

- For 10 mm case
  - Reflection is still large at “Equalized end-to-end PR”
- For 8 mm case
  - TX EQ + CTLE reduce ‘reflection’ at sampling points
  - COM improves a lot (>2 dB)