DFE-based model vs FFE-based model for Reference Rx of COM

IEEE P802.3ck Task Force Ad Hoc, 10/24/2018

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Background

- There has been discussion on DFE-based model vs FFE-based model for reference Rx of COM

  - DFE-based model
    - CTLE (3 poles + 2 zeros) + many-tap DFE
    - Represents analog-based Rx implementations
    - Conventional model, well-established experience of 3dB COM criteria in the past
      - We had consensus in the past standards to include quantization effect of DFE taps as part of 3dB COM budget

  - FFE-based model
    - CTLE (3 poles + 2 zeros) + 1-tap DFE + many-tap Rx FFE
    - Represents ADC-based Rx implementations
    - A new model, no experience of COM value criteria
      - There is no consensus on how to include quantization effect of Rx-FFE taps as well as quantization effect of ADC

- We have studied which model is relevant for reference Rx in COM

Pre-cursor taps in FFE (a.k.a. FIR filter)

- Have a capability to adjust phase characteristics of system response
  - Sampling phase
  - Non-causal (a.k.a. non-minimum-phase) response
    - E.g. large intra-pair skew

- DFE-based model
  - Pre-cursor taps are only in Tx

- FFE-based model
  - Pre-cursor taps may be in Rx as well as Tx
  - Pre-cursor taps in Rx may cause a problem for DFE-based solutions
    - DFE-based Rx implementation may rely on capability of pre-cursor taps in Tx
    - COM must check if channel has phase characteristics within capability of pre-cursor taps in Tx

Simulation conditions and COM parameters

- Two sets of simulations
  - Sim1 : check the effects of pre-cursor taps in Rx in FFE-based model
  - Sim2 : check the effects of step and constraints of taps and compare two models

Simulation		Sim1: Effects of pre-cursor taps in Rx		Sim2: Effects of step and constraints	
Model		FFE-based	DFE-based	FFE-based	DFE-based
Tx FFE	pre taps (step)	3/1/0 (2.5, 4, 1%)	3 taps (2.5%)	3 taps (2.5%)	3 taps (2.5%)
	post taps (step)	1 tap (5%)			
Rx FFE	pre taps (step)	3 / 0 taps (0%)	N / A	0 taps	N / A
	post taps (step)	16 taps (0%)	N / A	16 taps (0, 1, 2.5%)	N / A
Rx DFE taps (step)		1 tap (0%)	16 taps (0%)	1 tap (0, 1, 2.5%)	16 taps (0, 1, 2.5%)
Rx FFE max pre1 / post1 / tapn		0.7 / 0.7 / 0.7	N / A	(0.7) / 0.7 / 0.7 or (0.3) / 0.3 / 0.125	N / A
Rx DFE max b1 / bn		0.7 / (0.2)	0.7 / 0.2	0.7 / (0.2) or 0.95 / (0.2)	0.7 / 0.2 or 0.95 / 0.2
Package model		30mm@87.5Ω+1.8mm@92.5Ω, C_d=110fF, C_p=70fF			
Noise, jitter		η_0=8.20E-9V^2/GHz, SNR_{TX}=32.5dB, σ_{RJ}=0.01UI, A_{DD}=0.02UI, R_{LM}=0.95			

Other COM parameter values are shown in a backup slide.

Channels used in this study

	Datafile pathname	Model	IL@26.6GHz	ICN
CH1	mellitz_...072518_…meg6…	Ideal PCB trace	28.0dB	0mV
CH2	mellitz_...072518_…twinax26…	Ideal Twinax cable	28.0dB	0mV
CH3	mellitz_...081518_...CaBP_BGAVia_Opt1_24dB…	Cabled backplane w/ instrumented micro via	23.3dB	0.755mV
CH4	mellitz_...081518_...CaBP_BGAVia_Opt1_28dB…		27.2dB	0.565mV
CH5	mellitz_...081518_...CaBP_BGAVia_Opt1_32dB…		31.0dB	0.437mV
CH6	mellitz_...081518_...CaBP_BGAVia_Opt2_24dB…	Cabled backplane w/ BGA region via	22.6dB	0.880mV
CH7	mellitz_...081518_...CaBP_BGAVia_Opt2_28dB…		26.3dB	0.652mV
CH8	mellitz_...081518_...CaBP_BGAVia_Opt2_32dB…		30.1dB	0.498mV
CH9	mellitz_3ck_01_0518_C2M…Z100_IL10_WC…	C2M channels using FLYOVER cable	9.96dB	4.5289mV
CH10	mellitz_3ck_01_0518_C2M…Z100_IL14_WC…		13.87dB	3.1934mV

All channel data are taken from IEEE P802.3ck Task Force – Tools and Channels page.
http://www.ieee802.org/3/ck/public/tools/index.html

Sim1 Results

- Capability of Tx-FFE pre-taps is mostly hidden by Rx-FFE pre-taps
- FFE based with no Rx pre-tap shows COM values similar to DFE based

Model		FFE based						DFE based
		Baseline	Low reso Tx pre-tap	High reso Tx pre-tap	1 Tx pre-tap	No Tx pre-tap	No Rx pre-tap	Baseline
Tx FFE	pre-taps (step)	3 taps (2.5%)	3 taps (4%)	3 taps (1%)	1 taps (2.5%)	0 taps	3 taps (2.5%)	3 taps (2.5%)
	post-taps (step)	1 tap (5%)						
Rx FFE	pre-taps (step)	3 taps (0%)					0 taps	0 taps
	post-taps (step)	16 taps (0%)						0 taps
Rx DFE	DFE taps (step)	1 tap (0%)						16 taps (0%)
COM value (dB)	CH1	4.5389	4.5389	4.5389	4.5389	sim failed†	3.8493	3.4011
	CH2	4.0824	4.0546		4.0824	sim failed†	3.5305	3.2230
	CH3	5.0053	5.0053		5.0053	sim failed†	4.4225	4.4370
	CH4	4.0132	4.0132		4.0132	sim failed†	3.3116	3.2230
	CH5	2.3609	2.3268		2.3609	sim failed†	1.6184	1.1897
	CH6	5.4167	5.4005		5.4167	sim failed†	4.7916	4.6272
	CH7	4.5243	4.4370	4.5243	4.5243	sim failed†	3.7017	3.4915
	CH8	3.0485	3.0362		3.0485	sim failed†	2.0915	1.7026
	CH9	3.9260	3.9260		3.9260	sim failed†	3.6738	3.8334
	CH10	4.4772	4.4772		4.4772	sim failed†	4.1899	4.3462
	AVG	4.1393	4.1216		4.1393		3.5181	3.3475

FFE tap constraints: pre1max=0.7, post1max=0.7, tapnmax=0.7 DFE tap constraints: b1max=0.7, bnmax=0.2

†: The algorithm in COM Tool v2.52 was unable to find the sampling phase where all constraints of coefficients are satisfied.

Discussion on Sim1 Results

- Why capability of Tx-FFE pre-taps is hidden by Rx-FFE pre-taps ?
  - Tx-FFE pre-taps have limited resolution
  - Rx-FFE pre-taps have unlimited resolution
    - It achieves high-precision adjustment of phase characteristics
  - As a result, phase characteristics are adjusted always in high precision by high capability of Rx-FFE pre-taps regardless of limited capability of Tx-FFE pre-taps

- Can we use limited resolution of Rx-FFE pre-taps as a work around?
  - No. Even with limited resolution, Rx-FFE pre-taps will obscure requirements for channel phase characteristics in the COM test.

- As a reference Rx model, FFE-based model should NOT have pre-cursor taps to support broader implementations (including DFE-based solutions)
  - Because channels which needs extra adjustment of phase characteristics beyond capability of Tx-FFE (e.g. too much intra-pair skew) should fail COM test
    - DFE-based Rx implementation without Rx-FFE pre-taps cannot support such channels

Sim2 Results (1/2) (b1≤0.7)

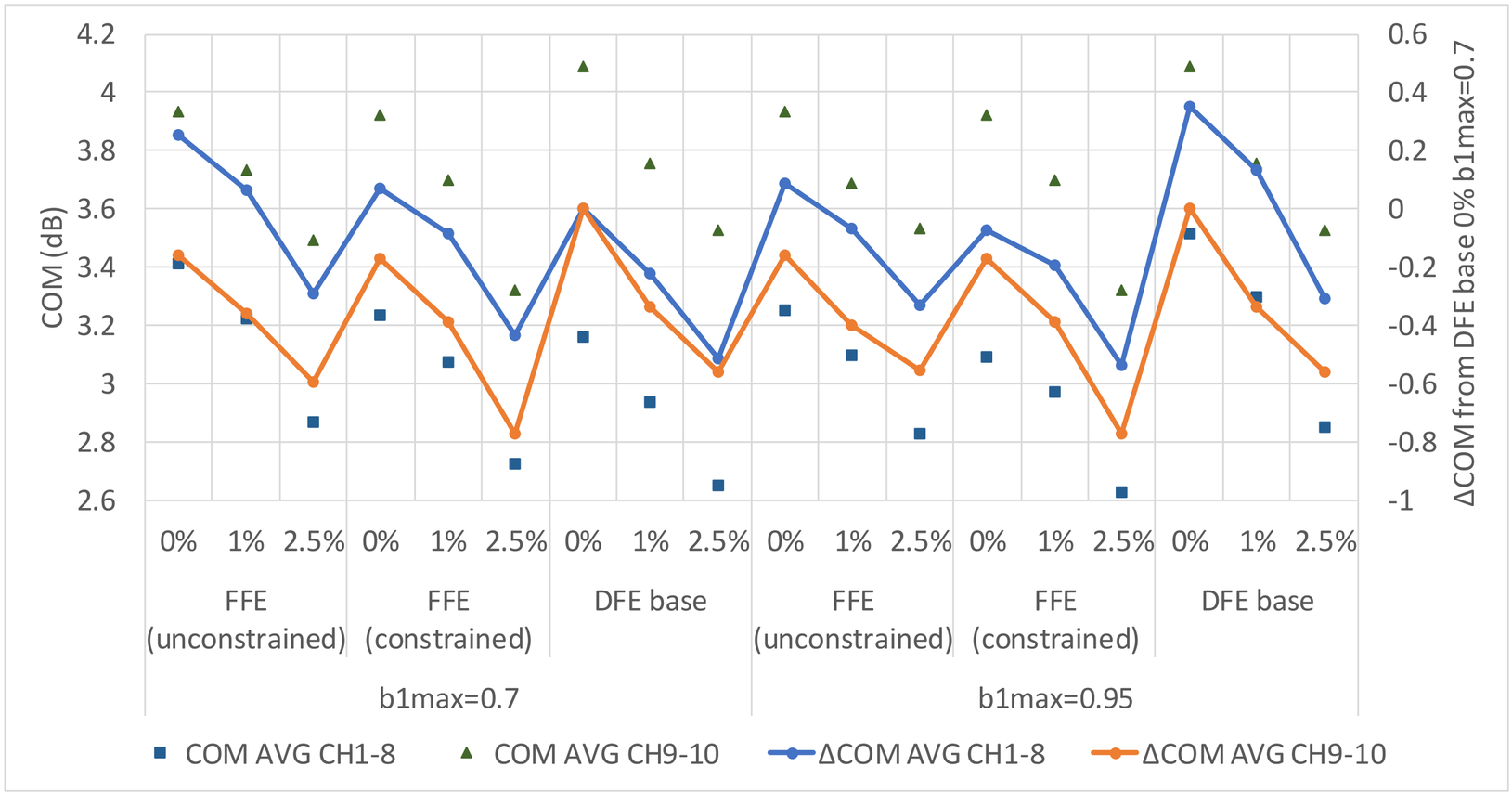
Model		FFE-based (unconstrained FFE)			FFE-based (constrained FFE)			DFE based		
		0% step	1% step	2.5% step	0% step	1% step	2.5% step	0% step	1% step	2.5% step
Rx FFE	# of taps	pre-cursor 0, post-cursor 16			pre-cursor 0, post-cursor 16			N/A		
	tap max	unconstrained (post1:0.7, tapn:0.7)			constrained (post1:0.3, tapn:0.125)			N/A		
	tap step	0%	1%	2.5%	0%	1%	2.5%	N/A		
Rx DFE	# of taps	1 tap			1 tap			16 taps		
	tap max	constrained (b1:0.7, bn:0.2)			constrained (b1:0.7, bn:0.2)			constrained (b1:0.7, bn:0.2)		
	tap step	0%	1%	2.5%	0%	1%	2.5%	0%	1%	2.5%
COM (dB)	CH1	3.8493	3.7017	3.4785	3.6752	3.5697	2.9626	3.4011	3.2609	2.6743
	CH2	3.5305	3.3754	2.9748	3.3626	3.2356	2.8413	3.2230	3.0362	2.8654
	CH3	4.4225	4.2508	3.6091	4.3793	4.2084	3.9582	4.4370	4.2366	4.1943
	CH4	3.3116	3.0733	2.9139	3.1229	2.9382	2.8413	3.2230	2.9139	2.7335
	CH5	1.6184	1.5041	1.1897	1.3505	1.1996	0.7716	1.1897	1.0415	0.9055
	CH6	4.7916	4.5683	3.8628	4.5830	4.2934	4.2225	4.6272	4.2366	3.5305
	CH7	3.7017	3.4268	3.0856	3.5045	3.3754	2.7335	3.4915	3.2356	3.1105
	CH8	2.0915	1.8949	1.8410	1.8733	1.7768	1.4732	1.7026	1.5351	1.1598
	CH9	3.6738	3.4691	3.3874	3.6793	3.4994	3.3874	3.8334	3.6444	3.3980
	CH10	4.1899	3.9912	3.5990	4.1639	3.9010	3.2482	4.3462	3.8654	3.6555
	AVG:CH1-8	3.4146	3.2244	2.8694	3.2314	3.0746	2.7255	3.1619	2.9371	2.6467
	AVG:CH9-10	3.9319	3.7302	3.4932	3.9216	3.7002	3.3178	4.0898	3.7549	3.5268

Sim2 Results (2/2) (b1≤0.95)

Model		FFE-based (unconstrained FFE)			FFE-based (constrained FFE)			DFE based		
		0% step	1% step	2.5% step	0% step	1% step	2.5% step	0% step	1% step	2.5% step
Rx FFE	# of taps	pre-cursor 0, post-cursor 16			pre-cursor 0, post-cursor 16			N/A		
	tap max	unconstrained (post1:0.7, tapn:0.7)			constrained (post1:0.3, tapn:0.125)			N/A		
	tap step	0%	1%	2.5%	0%	1%	2.5%	N/A		
Rx DFE	# of taps	1 tap			1 tap			16 taps		
	tap max	unconstrained (b1:0.95, bn:0.2)			unconstrained (b1:0.95, bn:0.2)			unconstrained (b1:0.95, bn:0.2)		
	tap step	0%	1%	2.5%	0%	1%	2.5%	0%	1%	2.5%
COM (dB)	CH1	3.6487	3.5045	3.2609	3.4785	3.3754	3.0980	4.1522	3.9857	3.3116
	CH2	3.3371	3.2735	2.8654	3.0362	2.9017	2.7574	3.7150	3.5305	3.3371
	CH3	4.3649	4.2084	3.9172	4.3649	4.1802	3.9172	4.6125	4.1943	3.5045
	CH4	3.1229	2.9871	2.8293	3.0116	2.9382	2.6389	3.4526	3.3116	3.1229
	CH5	1.3607	1.2396	1.1499	1.0415	1.0024	0.50056	1.6080	1.4732	1.2296
	CH6	4.6420	4.2934	3.7819	4.5830	4.3505	4.2225	4.6717	4.3505	3.5305
	CH7	3.5566	3.4526	3.1478	3.5305	3.4139	2.7335	3.7017	3.4526	3.1105
	CH8	1.9708	1.7982	1.6815	1.6604	1.5871	1.1400	2.2028	2.0695	1.6604
	CH9	3.6738	3.4691	3.3874	3.6793	3.4994	3.3874	3.8334	3.6444	3.3980
	CH10	4.1899	3.9064	3.6778	4.1639	3.9010	3.2482	4.3462	3.8654	3.6555
	AVG:CH1-8	3.2505	3.0947	2.8292	3.0883	2.9687	2.6260	3.5146	3.2960	2.8509
	AVG:CH9-10	3.9319	3.6878	3.5326	3.9216	3.7002	3.3178	4.0898	3.7549	3.5268

Summary of Sim2 Results

- Performance of FFE-based and DFE-based are often similar
  - Detail difference depends on the channel and the detail conditions
- Behavior of FFE-based is contradictory to change of b1max
  - If b1max is reduced (i.e. more constrained), COM is improved
- COM is significantly affected by step size of DFE and FFE taps



Conclusions

- Reference receiver should not have pre-cursor taps to support the development of Tx FIR
  - Channel phase characteristics must be checked if it is within capability of Tx pre-cursor resolution and length to support broader implementations
  - Pre-cursor taps of Rx FFE obscures requirements for channel phase characteristics

- Some mismatches are observed between DFE- and FFE-based models
  - A channel marginally passing one model might fails on the other model
    - Expected although not observed in the simulated channel sets
  - DFE does not amplify noise, but FFE does
  - Additional constraints, e.g. ICN limit, may be studied to reduce the COM pass/fail mismatch

- Quantization noise, circuit distortion, circuit noise in Rx are implementation trade off
  - In the past standards, we had consensus to include them as part of 3dB COM
  - If we decide to add those factors to the reference Rx model, it will result in 3dB COM threshold change
    - Efforts are needed to build consensus on what to include and what the threshold should be

- If we choose one model, DFE-based model is recommended
  - More studies are needed whether to add an additional FFE-based model

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Back up

COM Parameters (DFE-based, baseline)

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.1e-4 1.1e-4]	nF	[TX RX]
z_p select	2		[test cases to run]
z_p (TX)	[12 30; 1.8 1.8; 0 0 ; 0 0]	mm	[test cases]
z_p (NEXT)	[12 30; 1.8 1.8; 0 0 ; 0 0]	mm	[test cases]
z_p (FEXT)	[12 30; 1.8 1.8; 0 0 ; 0 0]	mm	[test cases]
z_p (RX)	[12 30; 1.8 1.8; 0 0 ; 0 0]	mm	[test cases]
C_p	[0.7e-4 0.7e-4]	nF	[TX RX]
C_v	[0 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.41	V	
A_fe	0.41	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.025:0]		[min:step:max]
c(-2)	[0:.025:0.1]		[min:step:max]
c(-3)	[-0.1:0.025:0]		[min:step:max]
c(-4)	[0]		[min:step:max]
c(1)	[-0.3:0.05:0]		[min:step:max]
N_b	16	UI	
b_max(1)	0.7		
b_max(2..N_b)	0.2		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	
ffe_pre_tap_len	**0**	UI	
ffe_post_tap_len	0	UI	
Include PCB	0	logical	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	\results\100GEL_WG_{date}\	
SAVE_FIGURES	1	logical
Port Order	[1 3 2 4]	
RUNTAG	KR2_ev al1_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
DER_0	1.00E-04	
T_r	6.16E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	**0.18**	
fixture delay time	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 1.0404e-3 4.201e-4]	
package_tl_tau	6.325E-03	ns/mm
package_Z_c	[87.5 87.5; 92.5 92.5; 100 100; 100 100]	Ohm (tdr sel)

Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 3.8206e-04 9.5909e-05]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*115*	mm
z_bp (NEXT)	*115*	mm
z_bp (FEXT)	*115*	mm
z_bp (RX)	*115*	mm