C2M Simulation with Proposed Reference Receivers

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Objective

- Introduce EVEC (Effective Vertical Eye Closure) to solve short channel issue.

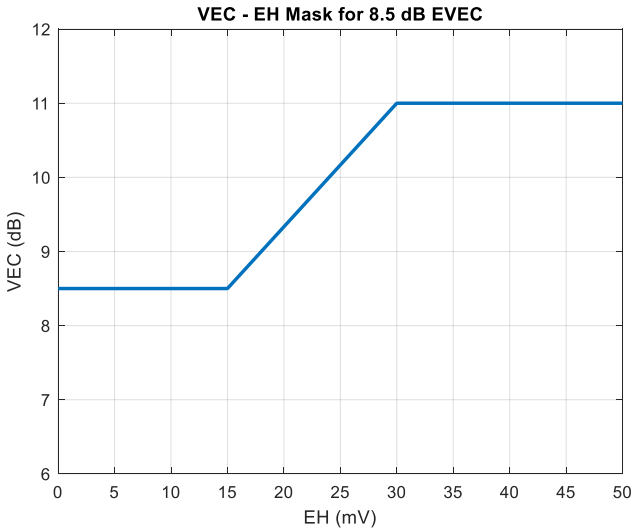
- Derive test point parameters for proposed reference receivers.
- TP1a
- TP4 near and far end.

- Verify performance of the receivers under discussion.

EVEC

EVEC is proposed in sun_3ck_01_1019 for TP1a measurement. It is a function of VEC and EH.

$$\text{EVEC} = \begin{cases} VEC, & if\ EH < 15\ mV \\ VEC\ -\ 0.1667 * (EH\ -15)\ dB, & if\ EH\ is\ between\ 15\ and\ 30\ mV \\ VEC - 2.5\ dB\ , & if\ EH > 30\ mV \end{cases}$$



TP1a Simulation Channels – Long Channel Set

ID	Channel Description	Vote in May	IL (dB)	ERL11 (dB)	ERL22 (dB)	ICN (mV)	ILD (dB)
8	mellitz_3ck_01_0518_C2M\9dB	Pass	8.95	16.35	13.56	2.10	0.10
9	mellitz_3ck_01_0518_C2M\10dB	Fail	9.96	7.79	10.91	4.27	0.48
10	mellitz_3ck_01_0518_C2M\11dB	Pass	11.16	18.28	14.64	1.75	0.09
11	mellitz_3ck_01_0518_C2M\12dB	Fail	12.18	8.39	11.64	3.75	0.46
12	mellitz_3ck_01_0518_C2M\13dB	Pass	13.12	20.09	15.25	1.50	0.09
13	mellitz_3ck_01_0518_C2M\14dB	Fail	13.87	8.73	12.80	2.98	0.47
14	tracy_100GEL_02_0118\long_barrel_via\TX5	TBD	16.48	14.98	11.75	0.86	0.28
15	tracy_100GEL_02_0118\long_barrel_via\TX6	TBD	16.08	14.35	12.82	0.86	0.37
16	tracy_100GEL_06_0118\Microvia\RX6	Pass	14.59	15.71	12.74	0.79	0.21
17	tracy_100GEL_06_0118\Microvia\RX5	TBD	14.57	16.20	13.76	0.89	0.23
18	lim_3ck_01_0319_QDD_new_pad\ch1	Pass	14.40	15.83	21.66	0.73	0.20
19	lim_3ck_01_0319_QDD_new_pad\ch2	Pass	14.60	14.51	21.02	0.76	0.19
20	lim_3ck_01_0319_QDD_legacy_pad\ch3	Pass	14.69	16.04	16.42	0.72	0.20
21	llim_3ck_01_0319_QDD_legacy_pad\ch4	Pass	14.84	14.77	16.11	0.81	0.18
22	llim_3ck_01_0319_QDD_new_pad\ch5	TBD	14.77	14.70	21.42	1.34	0.16
23	llim_3ck_01_0319_QDD_legacy_pad\ch6	Pass	15.02	15.01	16.30	1.47	0.17
24	ito_3ck_01\QSFP \bottom normal\	Pass	15.10	12.79	10.92	1.14	0.18
25	ito_3ck_01\QSFP \bottom worst\	TBD	15.58	12.49	10.48	1.09	0.32
26	ito_3ck_01\QSFP \top normal\	Pass	14.53	12.76	11.03	1.19	0.18
27	ito_3ck_01\QSFP \top worst\	TBD	14.49	12.43	10.52	1.14	0.31

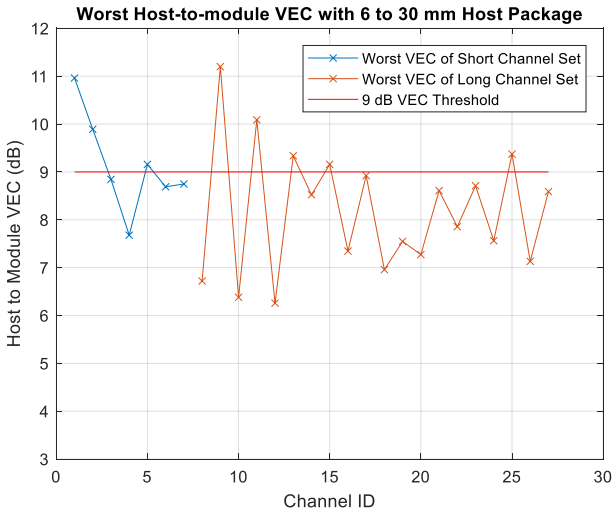
- Channels are from sun_3ck_01_0519.

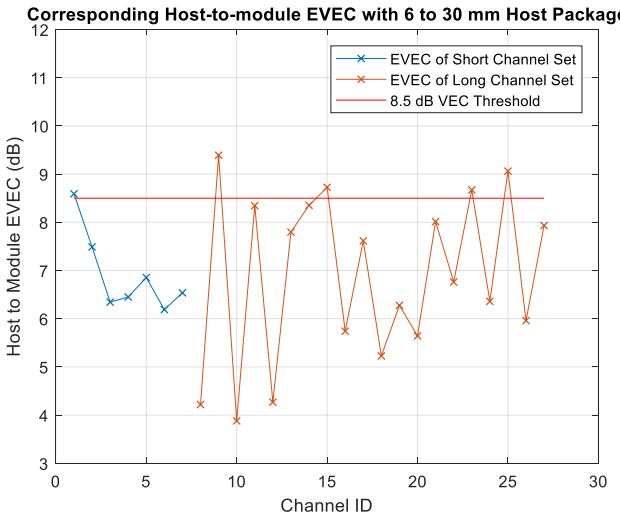
TP1a Simulation Channels – Short Channel Set

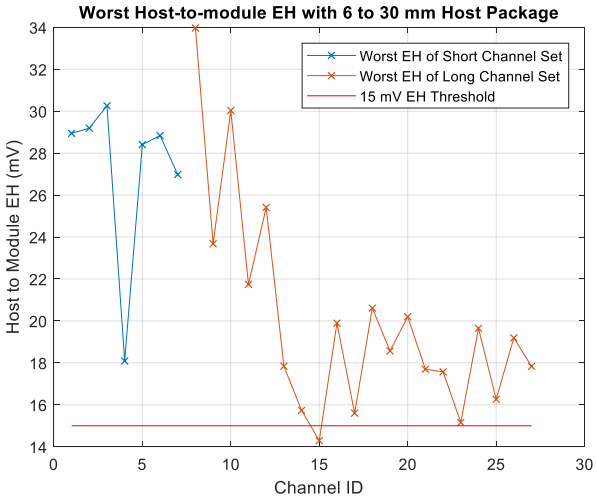
ID	Channel Description	IL (dB)	ERL11 (dB)	ERL22 (dB)	ICN (mV)	ILD (dB)
1	lim_3ck_adhoc_01_073119\2inch	5.67	11.93	13.31	3.52	0.16
2	lim_3ck_adhoc_01_073119\3inch	6.94	12.69	14.91	3.05	0.15
3	lim_3ck_adhoc_01_073119\4inch	8.22	13.31	16.36	2.65	0.14
4	lim_3ck_adhoc_01_073119\9inch	14.55	15.17	21.37	1.34	0.13
5	akinwale_3ck_adhoc_01a_08282019\2inch	7.15	12.61	15.48	5.54	0.36
6	akinwale_3ck_adhoc_01a_08282019\3inch	8.37	13.89	17.26	5.24	0.36
7	akinwale_3ck_adhoc_01a_08282019\4inch	9.70	14.11	18.88	5.01	0.36

- This is a new set of channels to study short channel performance.

VEC, EH, and EVEC

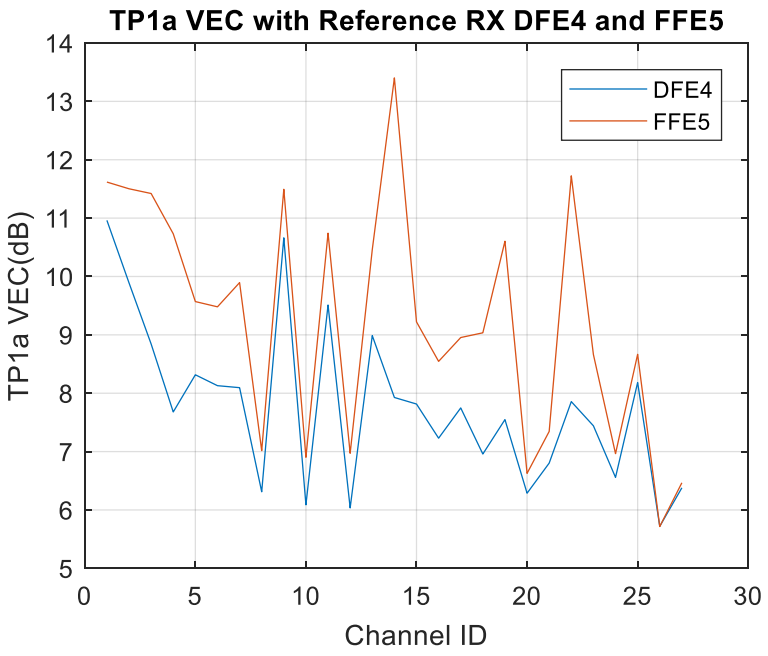






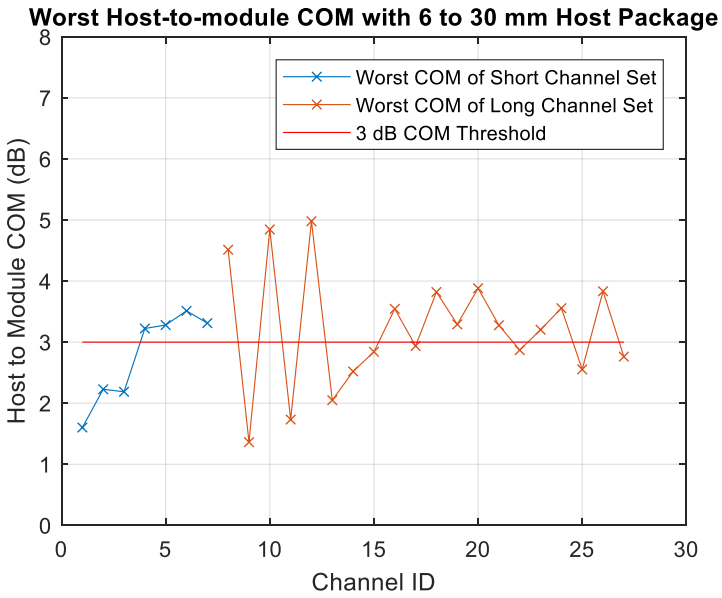
- Each channel is simulated with 2 to 30 mm packages. For each channel, VEC with the worst package trace is plotted.
- EVEC and VEC difference are bigger for short channels.
- Possible thresholds: 8.5 dB EVEC and 15 mV EH.

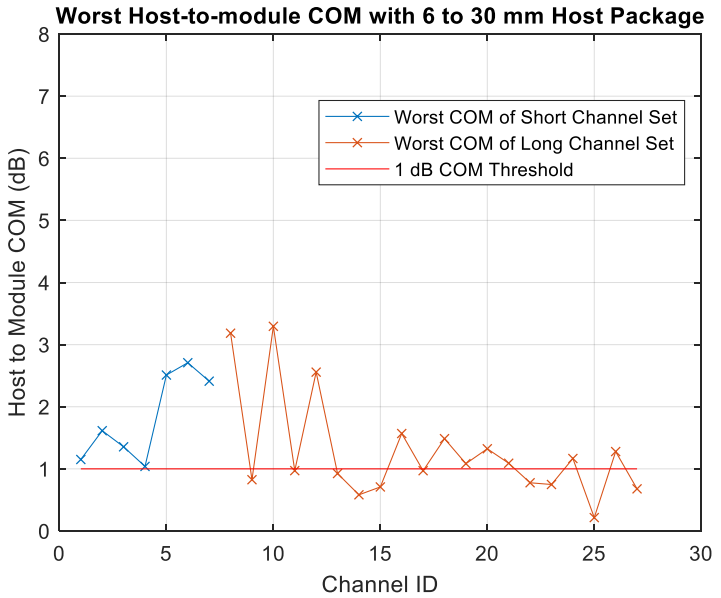
TP1a VEC Simulation with DFE 4 and FFE 5



- TP1a VEC with DFE4 is consistently lower than FFE5.
- VEC of FFE 5 has some big spikes as FFE5 is more sensitive to channel impairment.
- With 13 mm host pkg

Whole Link COM with DFE4

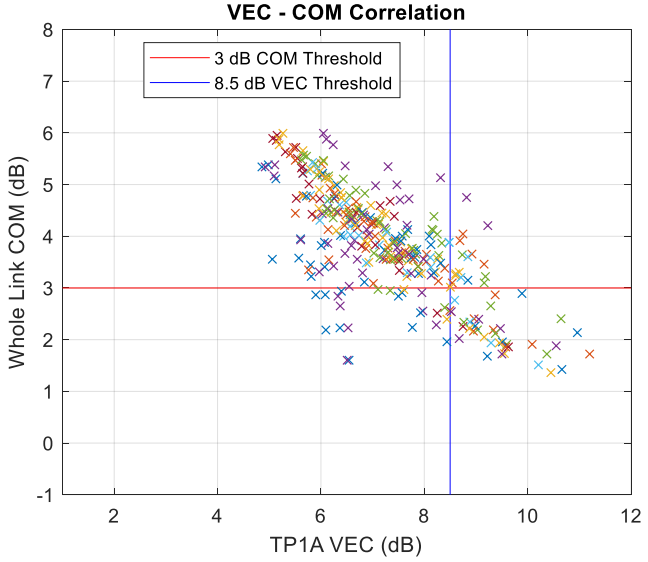


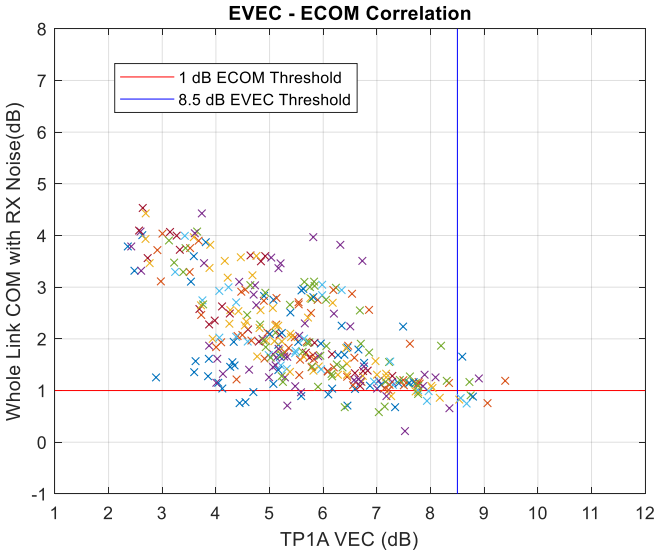


- w/o Implementation impairment
- w/ Implementation noise lumped at CTLE Input

- Performance with implementation impairment is evaluated by adding 2.6 mV RMS noise lumped at CTLE input.
- Short channels are not harder than the 9” long channel when implementation noise is considered.
- Receiver is DFE4. This confirms DFE4 is a minimum performance receiver (enough but w/o much margin) for whole link.

VEC/EH and Whole-Link COM Correlation



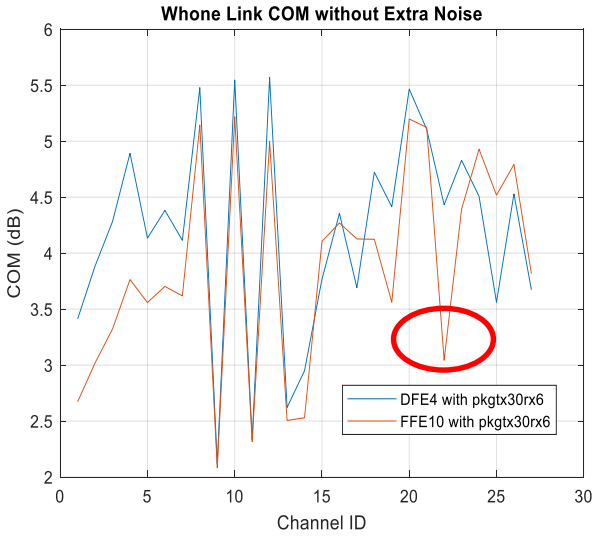


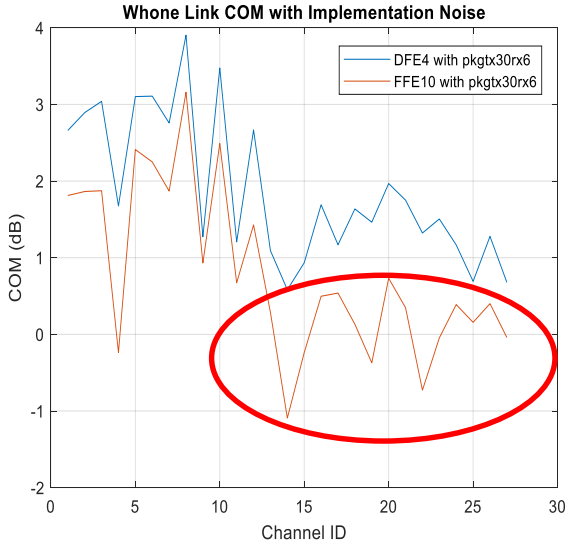
No Implementation Impairment

COM with RX noise

- ECOM (effective COM is COM with noise) is COM with 2.6 mV RMS noise lumped at CTLE input.
- Reference and whole link receiver are both DFE4 with b1max=0.5.

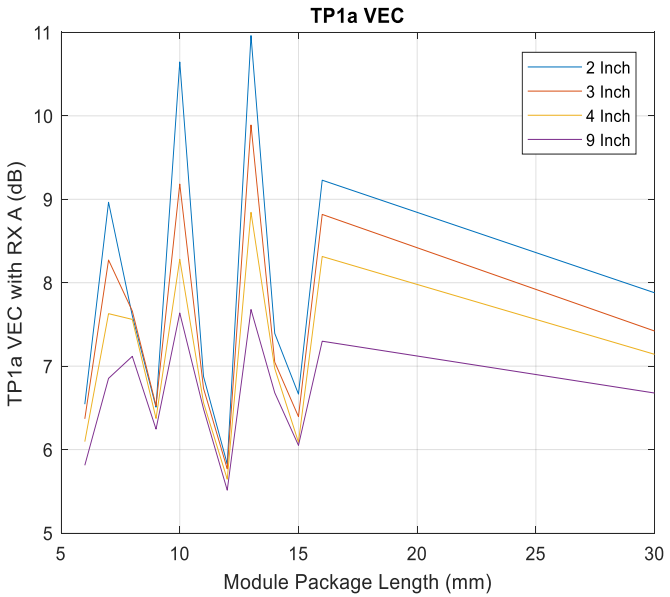
Whole Link COM with FFE10

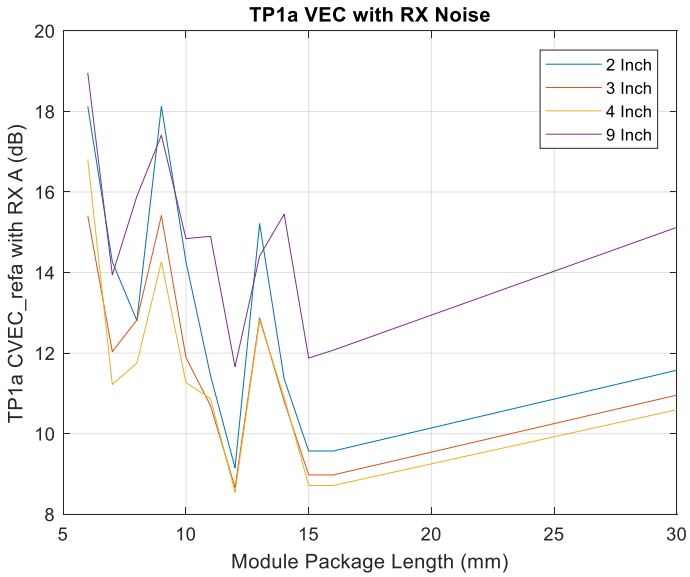




- Studies in this group show FFE5 cannot cover whole link.
- Even 10-tap FFE has sharp performance degradation if reflection cannot be covered by FFE taps.
- If add 2.6 mV RMS noise at CTLE input, FFE 10 cannot achieve 1dB COM for many channels. Less receiver noise can be tolerated.

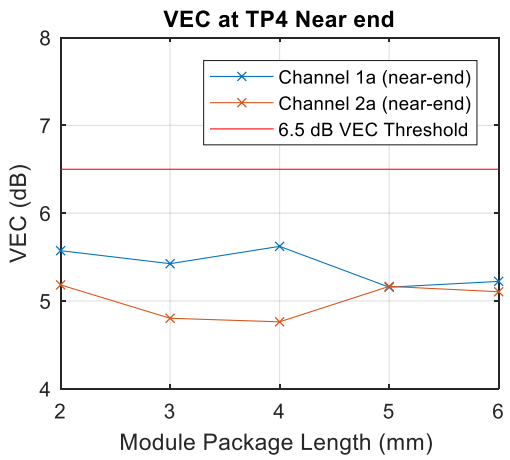
What if adding RX Noise for Test Point Measurement

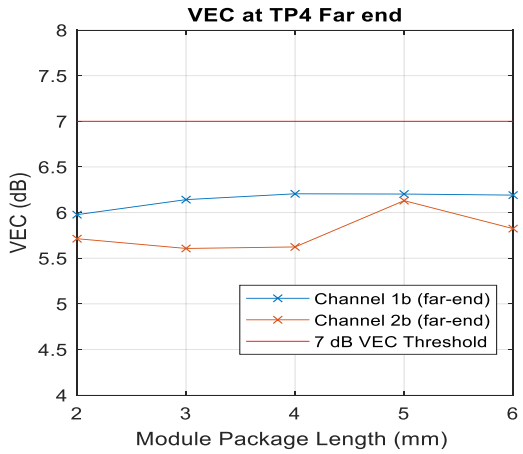


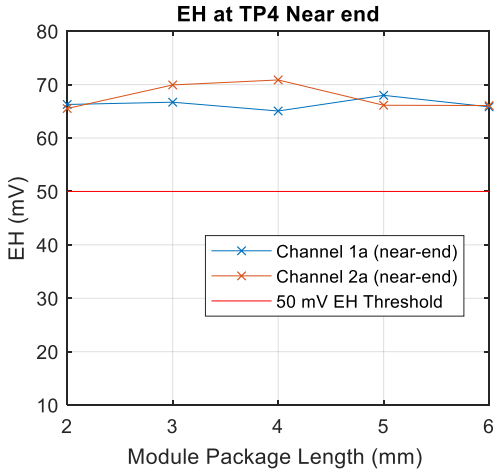


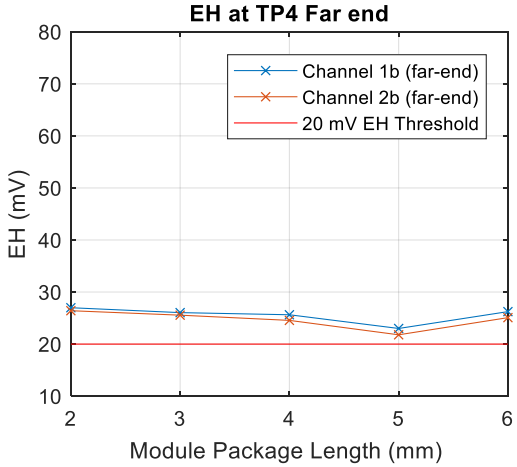
- 2.6 mV RMS noise lumped at CTLE input is added.
- VEC of short channels is not worse than the 9” long channel if RX noise is included for TP1a measurement.

TP4 Near- and Far End









- Channels are described in lim_3ck_02_0719.

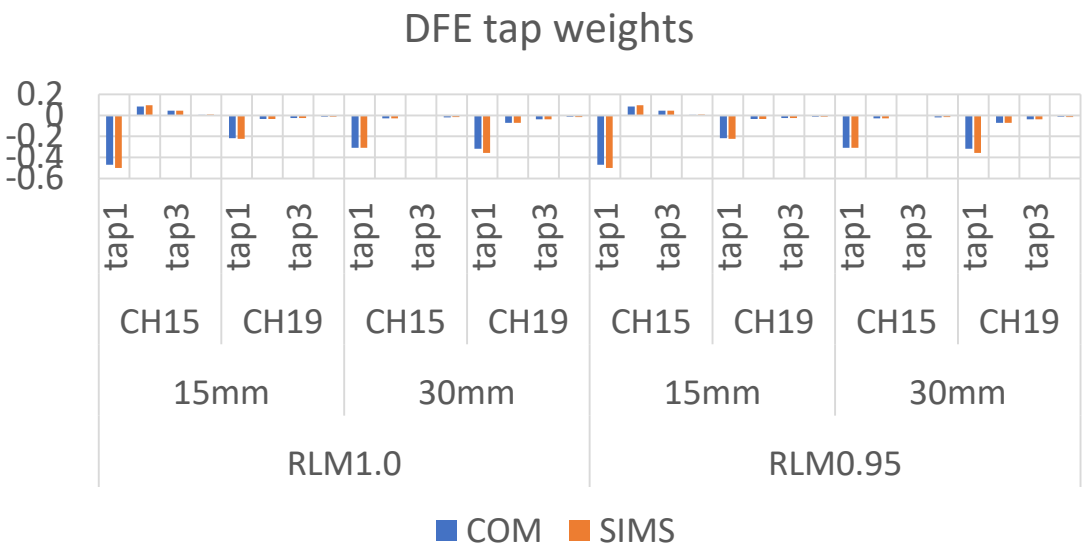
Summary

- TP1a and TP4 thresholds are proposed for the C2M baseline proposal with a 4-tap DFE receiver.
  - EVEC is introduced to qualify TP1a signal quality. Only a single value is needed.
- A short reference receiver is preferred because a long reference receiver is insensitive to reflections in its tap coverage and forces all implementations to include high power long equalizer.
- Simulation confirms 4-tap DFE is sufficient for the whole link.
  - 4-tap DFE is more robust than a 10-tap FFE.
- VEC value is better with a 4-tap DFE than with a 5-tap FFE for all the simulated channels.

Backup Slides

Ref RX Methodology I – Leverage Annex 93A and 120E

- Pulse fitting to extract pulse response.
- Leverage Annex 93A for optimal phase and DFE tap weight.
- Apply phase and DFE weight on measured waveforms. Noise and distortion are all kept. Reuse Annex 120E for test point measurement.
- Pros: simple algorithm. Reliable and fast. Similarity with COM tool.
- Existing Annex 93A is well documented for receivers that have only DFE taps.

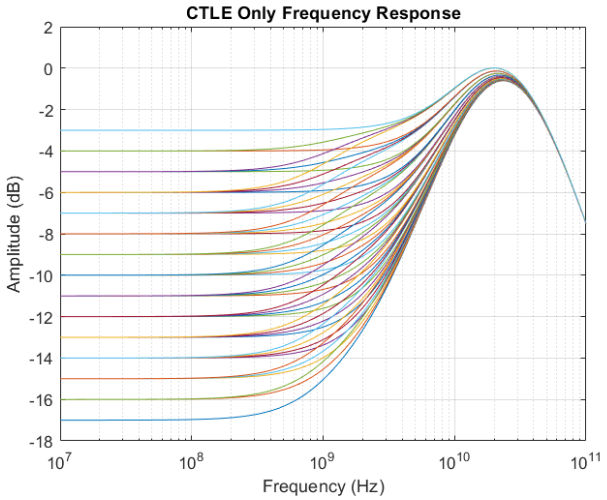


Good correlation is observed for DFE coefficients by waveform simulation and COM tool. This helps to use COM tool for system study.

Alternative Approach – Adding Receiver Noise

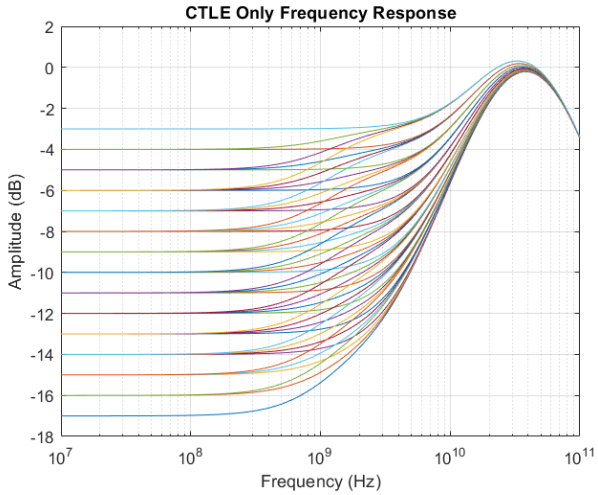
- Adding receiver noise for TP1a measurement and increase VEC threshold accordingly.
- After considering receiver impairment, VEC of short and long channels are more balanced.
- VEC threshold at TP1a is set to 19 dB (equivalent to about 1dB COM).

CTLE



CTLE and Noise Filter for Receivers A, A2, and B		
g_{DC}	[-14:1:-3]	dB
f_z	12.58	GHz
f_{p1}	20	GHz
f_{p2}	28	GHz
g_{DC2}	[-3:1:0]	dB
f_{LF}	1.328125	GHz

CTLE for b_max(1) > 0



CTLE and Noise Filter for Receivers C and D		
g_{DC}	[-14:1:-3]	dB
f_z	18.88	GHz
f_{p1}	28	GHz
f_{p2}	53.125	GHz
g_{DC2}	[-3:1:0]	dB
f_{LF}	1.328125	GHz

CTLE for b_max(1) = 0

TP1a COM Spread Sheet

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	1	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	1	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\TestCaseFloatingBank\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 , 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12, 0]	nH	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	C2M TP1a			Parameter	Setting	
z_p select	[1]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (TX)	[13 30; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	5.790E-03	ns/mm
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[13 30; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10.5	dB		z_bp (TX)	119	mm
z_p (RX)	[0 0; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	119	mm
C_p	[0.87e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	119	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	119	mm
R_d	[45, 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.391	V	vp/vf=.694		TDR and ERL options						
A_fe	0.391	V	vp/vf=.694		TDR	1	logical				
A_ne	0.489	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	400					
f_r	0.75	*fb			TDR_Butterworth	1	logical				
c(0)	0.6		min		beta_x	0.00E+00					
c(-1)	[-0.3:0.02:0]		[min:step:max]		rho_x	0.32					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0	enter sec				
c(-3)	[-0.04:.02:0.0]		[min:step:max]		TDR_W_TXPKG	1					
c(1)	[-0.1:0.05:0]		[min:step:max]		N_bx	4	UI				
N_b	4	UI			Receiver testing						
b_max(1)	0.5				RX_CALIBRATION	0	logical				
b_max(2..N_b)	0.2				Sigma BBN step	5.00E-03	V				
g_DC	[-14:1:-3]	dB	[min:step:max]		Noise, jitter						
f_z	12.58	GHz			sigma_RJ	0.01	UI				
f_p1	20	GHz			A_DD	0.02	UI				
f_p2	28	GHz			eta_0	8.20E-09	V^2/GHz				
g_DC_HP	[-3:1:0]		[min:step:max]		SNR_TX	33	dB				
f_HP_PZ	1.328125	GHz			R_LM	0.95					
ffe_pre_tap_len	0	UI									
ffe_post_tap_len	0	UI									
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.125										
ffe_backoff	0										
Floating Tap Control											
N_bg	0		0 1 2 or 3 groups								
N_bf	0		taps per group								
N_f	40		UI span for floating taps								
bmaxg	0.05		max DFE value for floating taps								

Whole-link COM Spread Sheet

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	0	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\TestCaseFloatingBank\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 , 0.85e-4]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12, 0.12]	nH	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]		RUNTAG	C2M end-to-end			Parameter	Setting	
z_p select	[1]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (TX)	[13 30; 1.8 1.8]	mm	[test cases]		Operational				board_tl_tau	5.790E-03	ns/mm
z_p (NEXT)	[6 2; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[13 30; 1.8 1.8]	mm	[test cases]		ERL Pass threshold	10.5	dB		z_bp (TX)	119	mm
z_p (RX)	[6 2; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	119	mm
C_p	[0.87e-4 0.75e-4]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	119	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	119	mm
R_d	[45, 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.391	V	vp/vf=.694		TDR and ERL options						
A_fe	0.391	V	vp/vf=.694		TDR	1	logical				
A_ne	0.489	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	400					
f_r	0.75	*fb			TDR_Butterworth	1	logical				
c(0)	0.6		min		beta_x	0.00E+00					
c(-1)	[-0.3:0.02:0]		[min:step:max]		rho_x	0.32					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0	enter sec				
c(-3)	[-0.04:.02:0.0]		[min:step:max]		TDR_W_TXPKG	1					
c(1)	[-0.1:0.05:0]		[min:step:max]		N_bx	4	UI				
N_b	4	UI			Receiver testing						
b_max(1)	0.5				RX_CALIBRATION	0	logical				
b_max(2..N_b)	0.2				Sigma BBN step	5.00E-03	V				
g_DC	[-14:1:-3]	dB	[min:step:max]		Noise, jitter						
f_z	12.58	GHz			sigma_RJ	0.01	UI				
f_p1	20	GHz			A_DD	0.02	UI				
f_p2	28	GHz			eta_0	8.20E-09	V^2/GHz				
g_DC_HP	[-3:1:0]		[min:step:max]		SNR_TX	33	dB				
f_HP_PZ	1.328125	GHz			R_LM	0.95					
ffe_pre_tap_len	0	UI									
ffe_post_tap_len	0	UI									
ffe_tap_step_size	0										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.125										
ffe_backoff	0										
Floating Tap Control											
N_bg	0		0 1 2 or 3 groups								
N_bf	4		taps per group								
N_f	40		UI span for floating taps								
bmaxg	0.05		max DFE value for floating taps								

TP4 COM Spread Sheet

Table 93A-1 parameters					I/O control				Table 93A–3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	0	logical		Parameter	Setting	Units
f_b	53.125	GBd			DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz			CSV_REPORT	1	logical		package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz			RESULT_DIR	.\TestCaseFloatingBank\			package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[0.85e-4 , 0]	nF	[TX RX]		SAVE_FIGURES	0	logical				
L_s	[0.12, 0]	nH	[TX RX]		Port Order	[1 3 2 4]			Table 92–12 parameters		
C_b	[0.3e-4 0]	nF	[TX RX]		RUNTAG	testPkg			Parameter	Setting	
z_p select	[1 2]		[test cases to run]		COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p (TX)	[6 8; 0 0]	mm	[test cases]		Operational				board_tl_tau	5.790E-03	ns/mm
z_p (NEXT)	[0 0; 0 0]	mm	[test cases]		COM Pass threshold	3	dB		board_Z_c	90	Ohm
z_p (FEXT)	[6 8; 0 0]	mm	[test cases]		ERL Pass threshold	10.5	dB		z_bp (TX)	119	mm
z_p (RX)	[0 0; 0 0]	mm	[test cases]		DER_0	1.00E-05			z_bp (NEXT)	119	mm
C_p	[0.75e-4 0]	nF	[TX RX]		T_r	6.16E-03	ns		z_bp (FEXT)	119	mm
R_0	50	Ohm			FORCE_TR	1	logical		z_bp (RX)	119	mm
R_d	[45, 50]	Ohm	[TX RX]		Include PCB	0	logical				
A_v	0.391	V	vp/vf=.694		TDR and ERL options						
A_fe	0.391	V	vp/vf=.694		TDR	1	logical				
A_ne	0.489	V			ERL	1	logical				
L	4				ERL_ONLY	0	logical				
M	32				TR_TDR	0.01	ns				
filter and Eq					N	400					
f_r	0.75	*fb			TDR_Butterworth	1	logical				
c(0)	0.6		min		beta_x	0.00E+00					
c(-1)	[-0.3:0.02:0]		[min:step:max]		rho_x	0.32					
c(-2)	[0:.02:0.1]		[min:step:max]		fixture delay time	0	enter sec				
c(-3)	[-0.04:.02:0.0]		[min:step:max]		TDR_W_TXPKG	1					
c(1)	[-0.1:0.05:0]		[min:step:max]		N_bx	4	UI				
N_b	4	UI			Receiver testing						
b_max(1)	0.5				RX_CALIBRATION	0	logical				
b_max(2..N_b)	0.2				Sigma BBN step	5.00E-03	V				
g_DC	[-14:1:-3]	dB	[min:step:max]		Noise, jitter						
f_z	12.58	GHz			sigma_RJ	0.01	UI				
f_p1	20	GHz			A_DD	0.02	UI				
f_p2	28	GHz			eta_0	8.20E-09	V^2/GHz				
g_DC_HP	[-3:1:0]		[min:step:max]		SNR_TX	33	dB				
f_HP_PZ	1.328125	GHz			R_LM	0.95					