TP2 J3u value

Contribution to support comment # 86 .3ck D2.2 Review Cycle

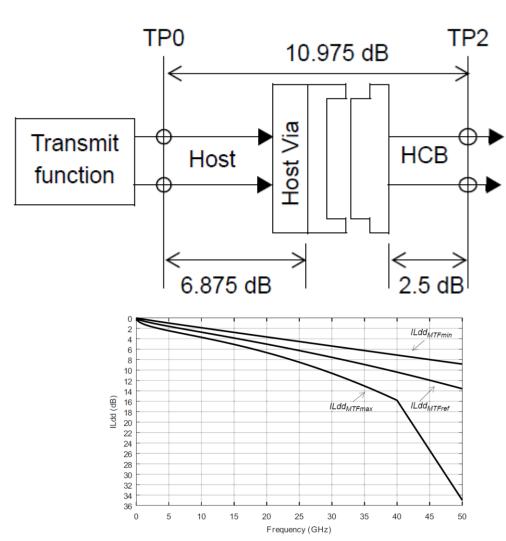
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TP2 measurement use-case is important



From the standpoint of being able to confirm electrical interoperability of a CR Transmitter Port by inserting an HCB and evaluating the signal properties, TP2 is kind of important. The Jitter values at TP2 are currently based on an unlikely set of minimum values (0dB package loss and 4.1dB MTF loss). Under these conditions 10.975dB net loss, the current J3u value of 110mUI <u>is</u> nominally attainable.

Bert output Total Path Loss (dB)	Bert FIR	J3U (mUI)	JRMS (mUI)
8	0/ 0.03/ -0.15/ 0.7/-0.08	75	10
15	-0.01/0.05/ -0.18/ 0.55/ -0.21	120	16

Figure 162B–3—Mated test fixtures differential-mode to differential-mode insertion loss



TP2 Problem statement

THE PUBLISHED J3U SPEC (115MUI) CAN'T BE REACHED DUE TO CHANNEL LOSS INDUCED NOISE CONTENT IN THE SIGNAL AT TP2.

TP0v jitter specs (output of the transmitter)

Residual intersymbol interference, ISI_RES (max)	163.9.2.6	-31	dB
Output jitter J _{RMS} (max) J4u (max) Even-odd jitter (max)	120F.3.1.3	0.023	UI
	120F.3.1.3	0.118	UI
	120F.3.1.3	0.025	UI

^aFor a PMA in the same package as the PCS sublayer. In other cases, the signaling rate is derived from the signaling rate presented to the input lanes (see Figure 135–3 and Figure 120–3) by the adjacent PMD, PMA, or FEC sublayers.

		(TP0) (TF
Device	Device package	2.8dB Pg 325: Eqn 163B-1
		SL <i>i</i>
Packago to		SL <i>i</i> <n></n>
Package-to-´ board interface	,	
	Transmitte	er test fixture

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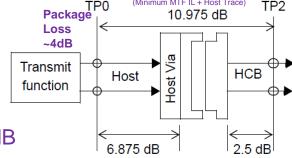
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Figure 163-3—Transmitter test fixture and test points

BERT Output

Output jitter (max) J _{RMS} We should focus on Jitter here by J3u compensating for slew rate limiting effects Even-odd jitter, pk-pk	162.9.3.4	0.023	UI
	162.9.3.4	0.115	UI
	162.9.3.4	0.025	UI





Proposed Solution:

.3ck (162.9.3) should permit edge compensation (equalization) at TP2 to allow better focus on measuring uncorrelated jitter, rather than the effects of slew rate limits and noise.



Proposed Change

Output jitter (max)			
$ m J_{RMS}$	162.9.3.4	0.023	UI
J3u ^C	162.9.3.4	0.115	UI
Even-odd jitter, pk-pk	162.9.3.4	0.025	UI

^aFor a PMD in the same package as the PCS sublayer. In other cases, the signaling rate is derived from the input to the PMD transmit function provided by the adjacent PMA sublayer.

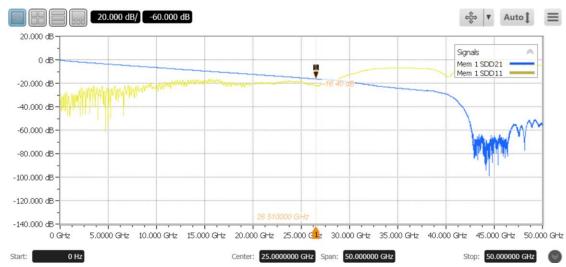


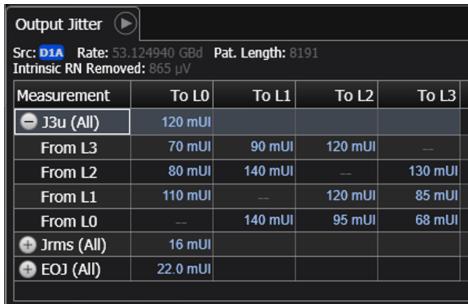
^bMeasurement uses the method described in 93.8.1.3 with the exception that the PRBS13Q test pattern is used.

^CNoise compensation methods or equalization are allowed to correct for slew rate limiting effects encountered at TP2.

Experimental Setup









TP2 J3u value: 802.3ck D2.2 Comments

Mated Test Fixture ILdd

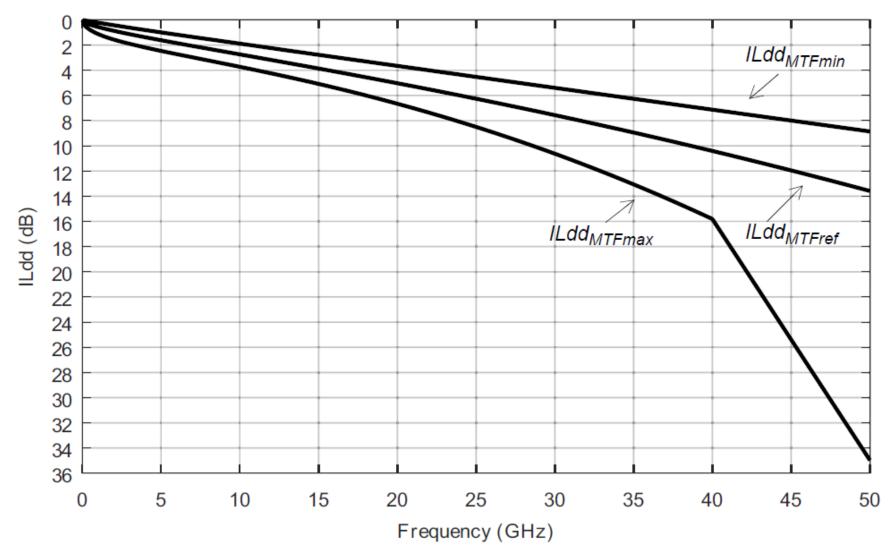


Figure 162B-3—Mated test fixtures differential-mode to differential-mode insertion loss

