# Concerns with stressed input tests in Annex 120G 8023ck_D1p3


John Calvin, Hadrien Louchet, Varun Garg | 2020.22.09

All employed by Keysight Technologies, Inc.


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# IEEE 802.3ck Receiver Input Test First Results

## AGENDA

- Near-end host input test and module input test setups
  - Overview
  - Tx characterization
  - Channel characterization
- Methodology
- Results
- Discussion/Recommendations

# Experimental setup – stressed input test

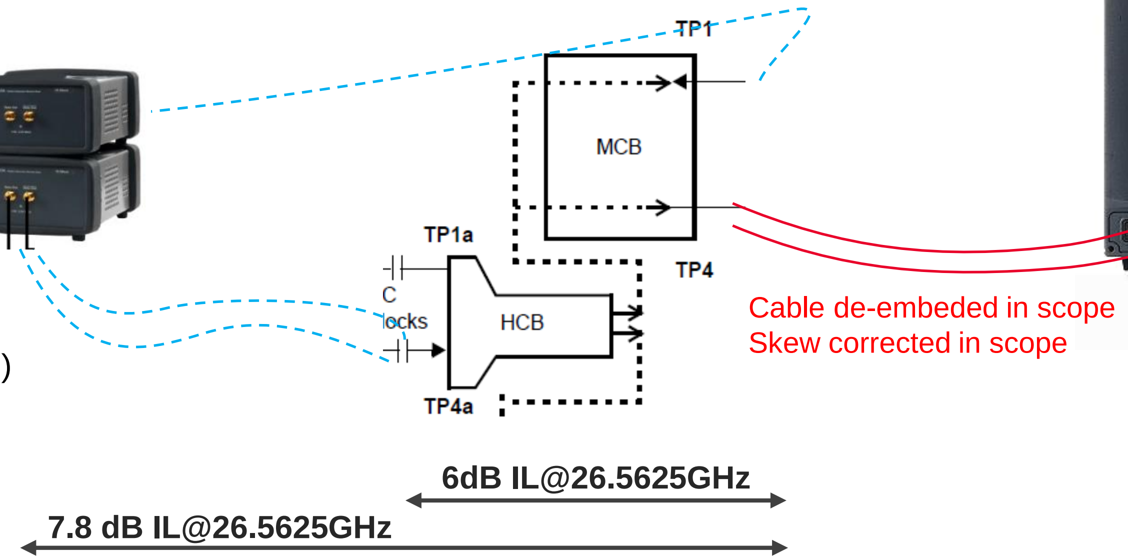
## HOST INPUT NEAR-END TEST

Stress signal and equipment **calibration**

M8045A PG

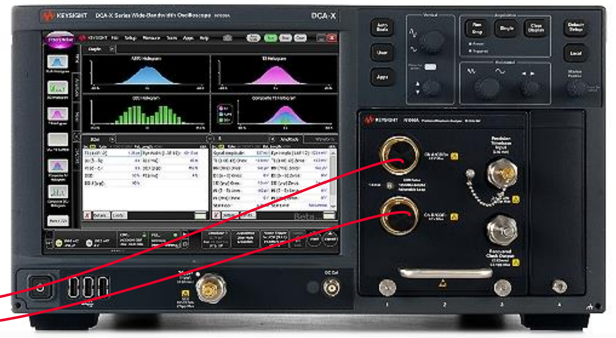
**2** or **3 pre-cursors**, 1 post-cursor
53.125Gbaud PAM4 (max 1.8V diff pp)
Inject SJ, RJ

**Mated MCB-HCB** (vendor **B**)




Cable de-embeded in scope
Skew corrected in scope

N1000A+N1060A



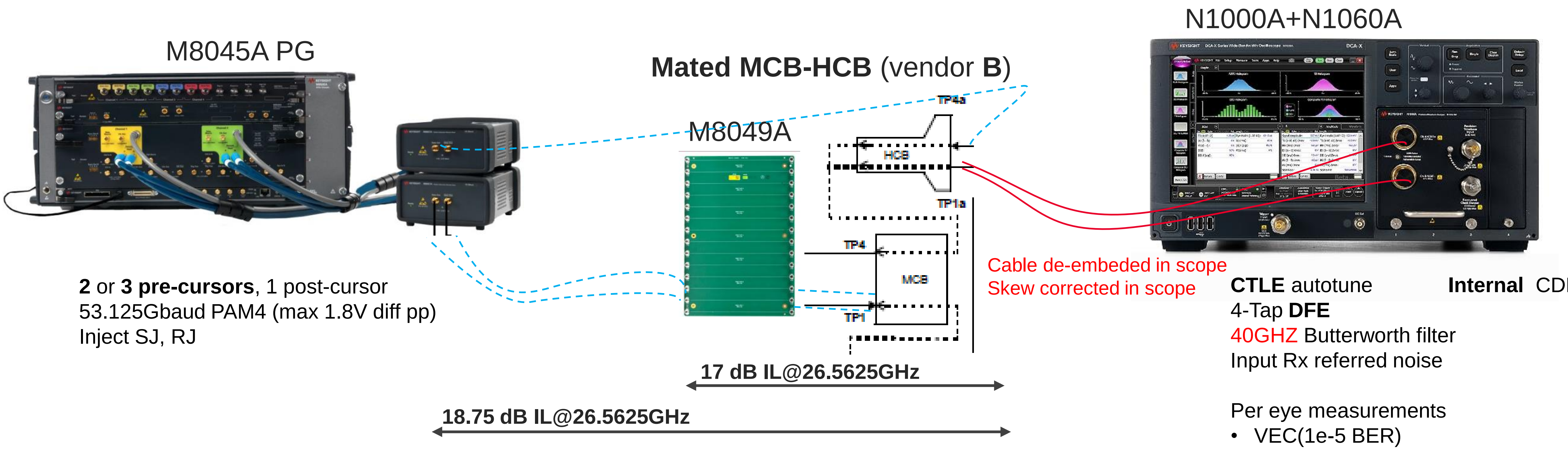
**CTLE** autotune **Internal** CDR
4-Tap **DFE**
40GHZ Butterworth filter
Input Rx referred noise

Per eye measurements
- VEC(1e-5 BER)
- EH, EW (1e-5 BER)

# Rx input test

## MODULE INPUT HIGH-LOSS TEST

Stress signal and equipment **calibration**




**2** or **3 pre-cursors**, 1 post-cursor
53.125Gbaud PAM4 (max 1.8V diff pp)
Inject SJ, RJ

**CTLE** autotune
4-Tap **DFE**
40GHZ Butterworth filter
Input Rx referred noise

**Internal** CDR

Per eye measurements

- VEC(1e-5 BER)
- EH, EW (1e-5 BER

# Tx Characterization

## @TP0V WITH 50MUI SJ @ 40MHZ

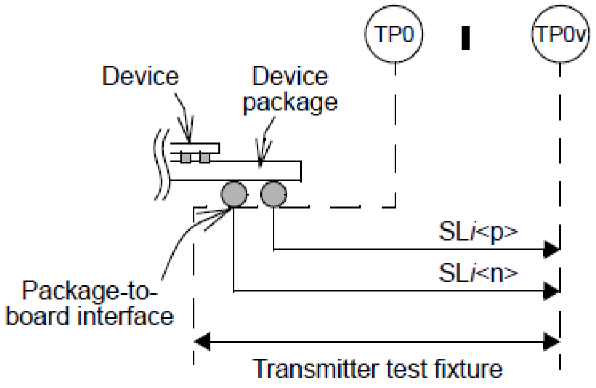



**Figure 163–3—Transmitter test fixture and test points**

**TP0** to **TP0v** replica trace embedded in the scope for Tx measurement

**Table 23-13. Host-to-Module Electrical Recommendations at TP0a**

| Parameter | Symbol | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| Baud Rate | | 36.0 | 58.0 | Gsym/s | |
| Differential Voltage, pk-pk | T_Vdiff | 750 | - | mV | See Note 1 |
| DC Common Mode Voltage | T_Vcm | -0.3 | 2.8 | V | See Note 2 |
| Differential Termination Resistance Mismatch | T_Rdm | - | 10 | % | at 1 MHz |
| Differential Return Loss | T_SDD22 | - | Equation 17-4 | dB | at TP0 |
| Transition Time: 20% to 80% | T_tr, T_tf | 6.5 | - | ps | With emphasis off |
| Common-mode return loss | T_SCC22 | -6 + 3*f/f$_b$ | - | dB | |
| Common Mode Noise, RMS | T_Ncm | - | 12 | mV | |
| Uncorrelated Jitter RMS (standard deviation of the probability distribution) | T_J$_{RMS}$ | | 0.023 | UI$_{RMS}$ | See Note 3 |
| Uncorrelated Jitter (time interval from 0.005% to 99.995% of the probability distribution) | T_J$_{4u}$ | | 0.118 | UI | See Note 3 |
| Even-Odd Jitter (EOJ) | T_EOJ | | 0.019 | UI | |
| | | 32.5 | - | dB | See Section 17.3.1.6.4 for definition |

...t TP1a. Minimum voltage can be lower for low loss

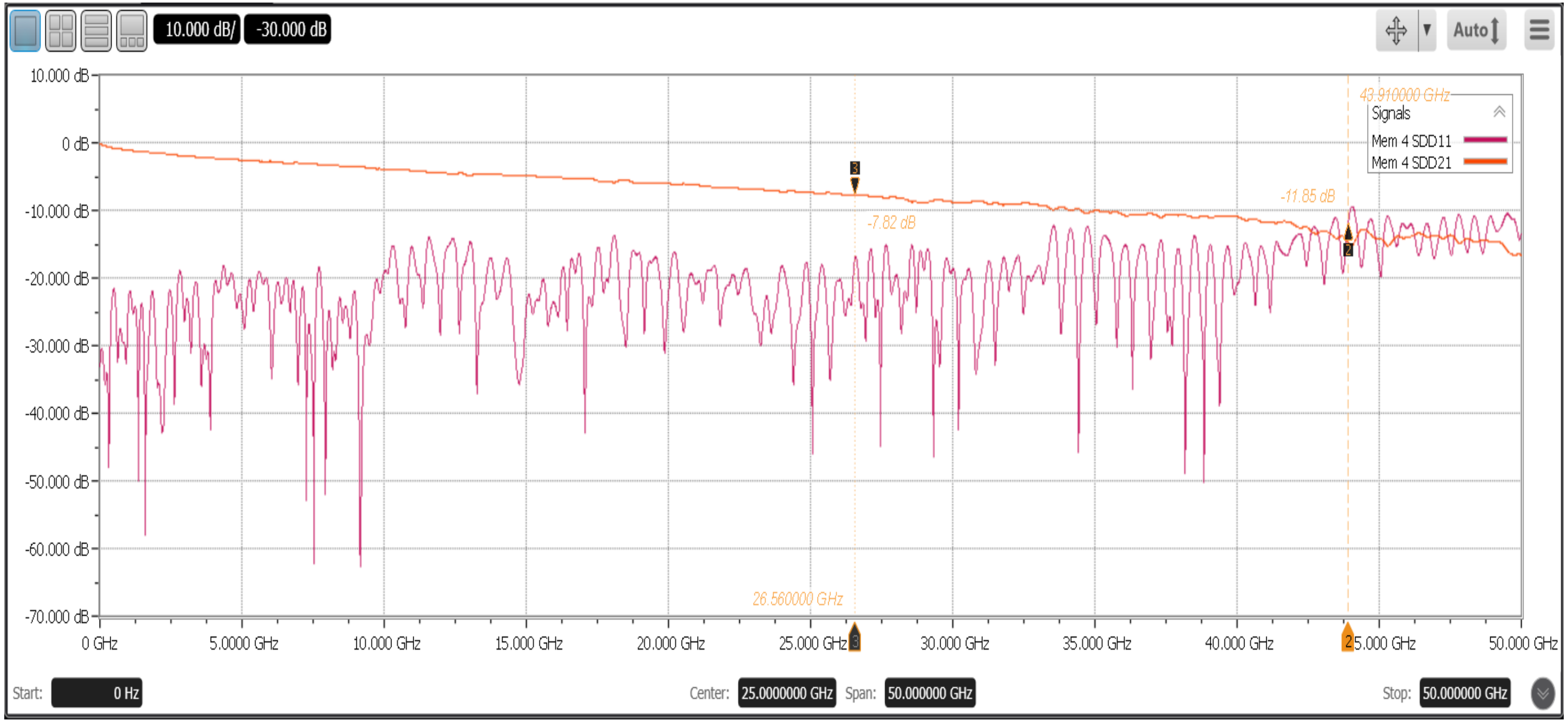
...ng or floating load.

...PAM4 Section 17.3.1.7

| Parameters | Reference to Table 23-13 | comments |
|---|---|---|
| **Transition time** | within spec | |
| **J4u** | within spec | include 50mUI sinusoidal jitter @40MHZ |
| **Jrms** | within spec | |
| **$R_{LM}$** | within Spec | |
| **SNDR** | > 31dB | |

# Channel Characterization

## HOST INPUT NEAR-END TEST

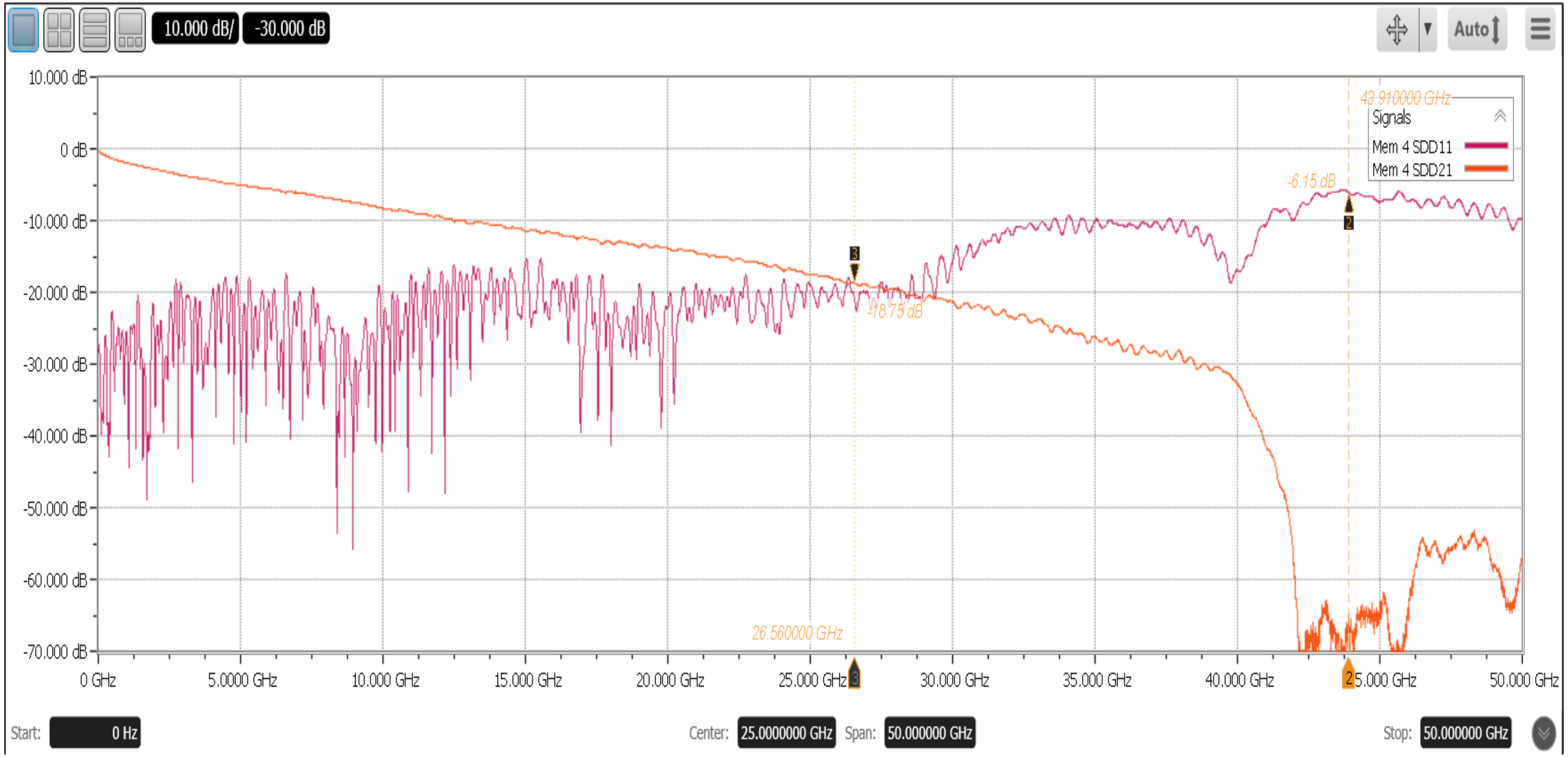



**COM Output** (ver 2.93):

- FOM_ILD: 0.0742
- COM(dB): 6.0293
- ERL22(dB): 13.5598
- ERL11(dB): 12.5234

# Channel Characterization

## MODULE INPUT HIGH-LOSS TEST




**COM Output** (ver 2.93):

- FOM_ILD: 0.1816
- COM: 3.736 dB
- ERL22(dB): 13.2508
- ERL11(dB): 13.2508

# Methodology

## FOLLOWING 802.3CK D1P3 ANNEX 120G RECIPE

### I. Signal generation

1. Inject **Sinusoidal Jitter** 50mUI @ 40MHz to the clean signal
2. **Characterize Tx** at TP0v
3. Run **COM**(ver 2.93) with excel sheet and s-parameter file of the thru channel
   - Take over calculated Tx de-emphasis
4. **Digital equalizer** optimization
   - CTLE autotune
   - DFE optimized for each configuration
   - Metric: min VEC

### II. Stress signal calibration

1. Adjust amplitude & inject RJ
   - Metric: **EH**@1e-5 (D1.3 values), **EW**@1e-5
   - Target values: **EH** following D1.3, **EW** 190mUI (Host input) (TBD in D1.3)

# Results

## STRESSED HOST INPUT, NEAR-END CALIBRATION


**Stressed Eye Setting**:

- Amplitude: 229 mV
- Tx taps: (0.0, 0.05, -0.20, 0.74, -0.01)
- CTLE: -2 dB, -0.5 dB
- SJ: 57.4 mUI (for maximum J4u and maximum Jrms)
- RJ: 5.66 mUI

**Stressed Eye Output**

- Eye Height: 24 mV
- Eye Width: 190 mUI
- VEC: 8.30 dB > 7.5dB

# Results

## STRESSED MODULE INPUT, HIGH-LOSS CALIBRATION


**Stressed Eye Setting**:

- Amplitude: 900 mV
- Tx taps: (-0.01, 0.06, -0.22, 0.68, 0.03)
- CTLE: -5.5dB, -2 dB
- SJ: 57.4 mUI (for maximum J4u and maximum Jrms)
- RJ: 0mUI

**Stressed Eye Output**

- Eye Height: 14.2mV
- Eye Width: 76 mUI
- VEC: 16.6 dB > 9.5dB

# Looking for the Bottleneck

## STRESSED MODULE INPUT, HIGH-LOSS CALIBRATION – „IDEAL EQUALIZER“#1

### De-embedded channel S4p on DCA

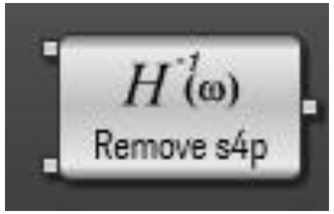

### Stressed Eye Setting:

- Amplitude: 800 mV
- Tx taps: (0, 0., 0, **1**, 0)
- **No CTLE**
- SJ: 57.4 mUI

### Stressed Eye Output

- Eye Height: 113mV
- Eye Width: 138 mUI
- VEC: 13 dB > 9.5dB

**→ Residual ISI closing the eye**



# Looking for the Bottleneck

## STRESSED MODULE INPUT, HIGH-LOSS CALIBRATION – „IDEALEQUALIZER“ #2

### De-embedded channel S4p + 4-taps DFE

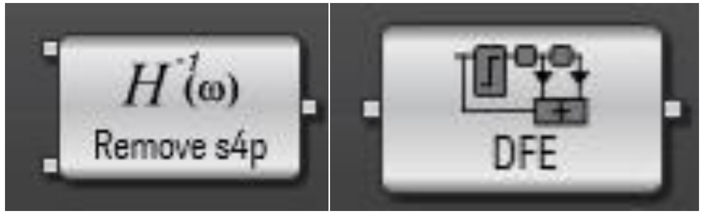

### Stressed Eye Setting:

- Amplitude: 800 mV
- Tx taps: (0, 0., 0, **1**, 0)
- **No CTLE**
- SJ: 57.4 mUI

### Stressed Eye Output

- Eye Height: 150mV
- Eye Width: 130 mUI
- VEC: 10.3 dB > 9.5dB

**→ Getting closer to the standard**



# Looking for the Bottleneck

## STRESSED MODULE INPUT, HIGH-LOSS CALIBRATION – „IDEAL EQUALIZER“ #3

### De-embedded channel S4p + 5-taps FFE (3 pre)

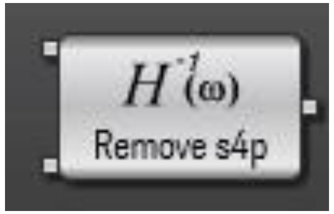

**Stressed Eye Setting**:

- Amplitude: 800 mV
- Tx taps: (0, 0., 0, **1**, 0)
- **No CTLE**
- SJ: 57.4 mUI

**Stressed Eye Output**

- Eye Height: 18mV
- Eye Width: 90 mUI
- VEC: 11 dB > 9.5dB

**→ No improvement vs. DFE**




# Discussion/Recomendations

## STRESSED INPUT TEST – RESULTS OVERVIEW

### I. Facts

- ❑ Mismatched with standard requirements even though channel & Tx are compliant
- ❑ Injected Sinusoidal Jitter affect
  - ❑ Eye Width (~50mUI reduction)
  - ❑ VEC (from 1.5-4dB degradation observed depending on channel)

### II. Open questions

- ❑ Any assumptions made for simulation than cannot hold in experiment
  - ❑ Does COM take refection into consideration?
  - ❑ **Anything else?**
- ❑ Do VEC targets includes impact of 50mUI SJ?

# Discussion/Recomendations

## STRESSED INPUT TEST – RESULTS OVERVIEW

### I. Recommendations

- ❑ **perform simulation with this same test channel to compare results to empirical data.**
- ❑ Host stressed input VEC changed from 7.5dB to 9.5dB to allow acceptable margin.

Draft Amendment to IEEE Std 802.3-2018
IEEE P802.3ck Task Force name Task Force

IEEE *Draft* P802.3ck/D1.3
1st September 2020

**Table 120G–6—Host stressed input parameters**

| Parameter | Value |
|---|---|
| Far-end ESMW (eye symmetry mask width) | TBD UI |
| Far-end eye width | TBD UI |
| Applied peak-to-peak sinusoidal jitter | Table 120G–7 |
| Far-end eye height | 24 mV |
| Far-end vertical eye closure | 7.5 dB |

- ❑ Module stressed input VEC should be relaxed from 9.5dB to a mean value of 12.5dB

**Table 120G–9—Module stressed input parameters**

| Parameter | Value |
|---|---|
| ESMW (Eye symmetry mask width) | TBD UI |
| Eye width | TBD UI |
| Applied pk-pk sinusoidal jitter | Table 120G–7 |
| Eye height | 15 mV |
| VEC (max) | 9.5 dB |
| VEC (min) | 9.0 dB |

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