Long MPS timings v110

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Problem

T_{MPDO} is the amount of time a PSE maintains power, even when the conditions for MPS are not met. The standard defines this as 300 ms to 400 ms.

When MPS conditions are met for at least T_{MPS}, the PSE must reset the MPS dropout time (T_{MPDO}). The value for T_{MPS} is 60 ms.

There is a discrepancy between a requirement in text (33.2.9.1.2) and the behavior of the state diagrams. The state diagrams alone cause an interoperability issue with the PD MPS timings.

Signify

State diagrams

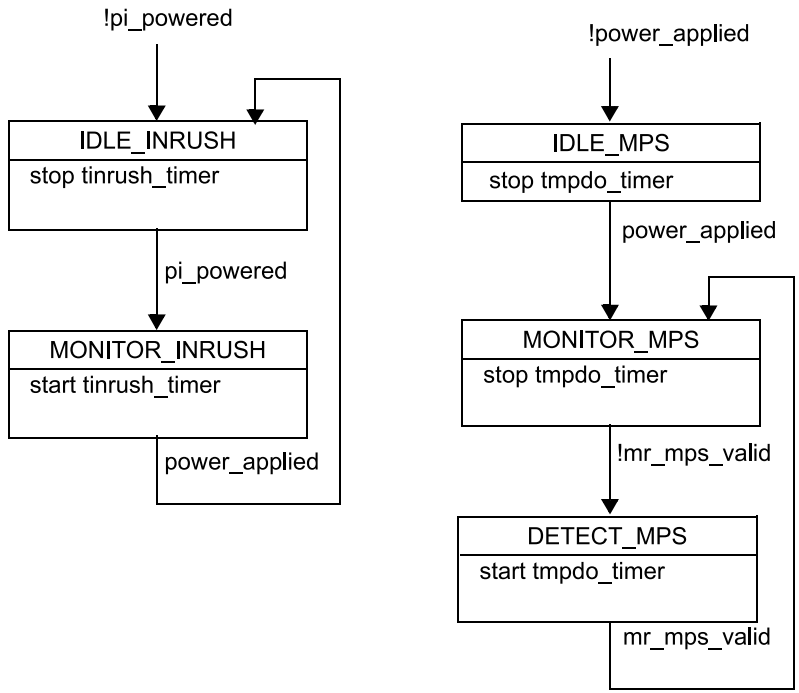


Figure 33–10—PSE monitor inrush and monitor MPS state diagrams

tmpdo_timer: A timer used to monitor the dropout of the MPS; see T_{MPDO} in Table 33–11.

Text

"Power shall be removed from the PI when DC MPS has been absent for a duration greater than T MPDO."

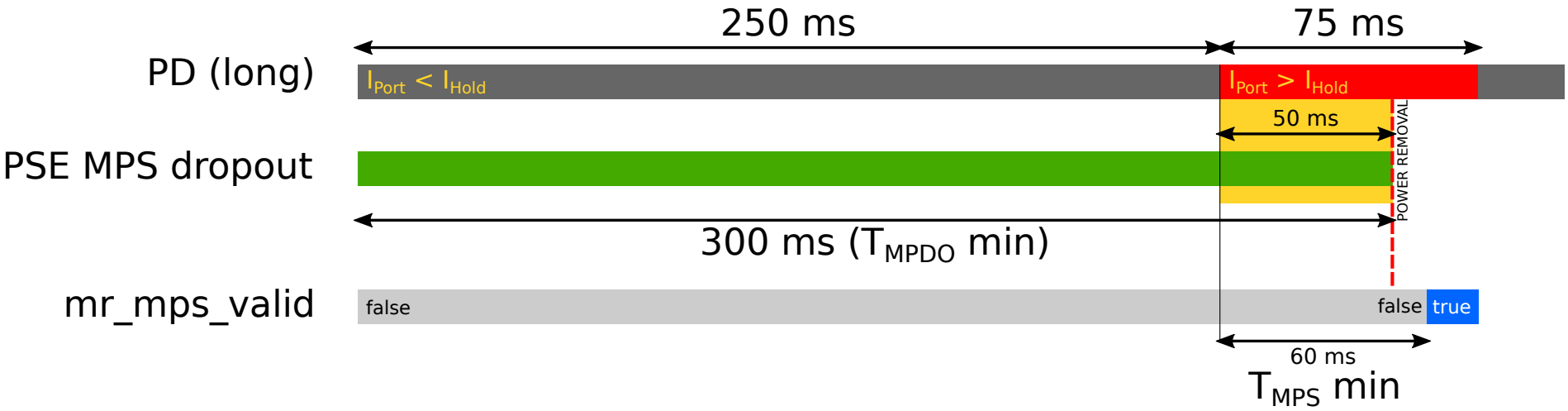
and

"The PSE shall not remove power from the port when I_{Port} is greater than or equal to I_{Hold} max continuously for at least T_{MPS} every T_{MPS} + T_{MPDO}, as defined in Table 33–11. This allows a PD to minimize its power consumption."

The final requirement allows the MPS pulse to be adjacent to the T_{MPDO} window, whereas the the state diagram requires the pulse to reside inside the T_{MPDO} window.

Signify

Timing issue



With an T_{MPDO} of 300 ms and a minimum duty cycle PD, the PSE will only have seen 50 ms worth of $I_{Port} > I_{Hold}$. The state diagram and the text at this point require it to remove power.

Simultaneously, the second text requirement requires power to be maintained for at least $T_{MPDO} + T_{MPS}$.
We need $T_{MPDO\_PD} + T_{MPS} < T_{MPDO\_PD}$ (250 ms + 60 ms < 300 ms) which is currently not the case.

Solution

There are two solution approaches, we can either change the text (and T_{MPDO} timings) to match with the state diagram, or we can make the state diagram agree with the text. This slide is the first option, see David Abramson's presentation for the state diagram solution.

1. Change T_{MPDO} min from 300 ms to 320 ms
   This matches the values in 802.3bt and covers the 10 ms we are short plus another 10 ms for the capacitive effect.
2. Change T_{MPDO} max from 400 ms to 460 ms.
3. "The PSE shall not remove power from the port when I_{Port} is greater than or equal to I_{Hold} max continuously for at least T_{MPS} ~~every T_{MPS} + T_{MPDO}~~ in the T_{MPDO} window, as defined in Table 33–11. This allows a PD to minimize its power consumption."

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About the short timings

There is no issue with the short MPS timings because $T_{MPDO\_PD} + T_{MPS} < T_{MPDO\_PD}$: $310\,\text{ms} + 6\,\text{ms} < 320\,\text{ms}$.

We will still need to address the line that requires power not to be removed in $T_{MPS} + T_{MPDO}$ to be changed in a similar way (or we choose not to change that).


signify