PD inrush baseline v200

Info (not part of baseline)

This baseline addresses MR 1277 which deals with the deficiencies of Clause 33's PD inrush section. Below is the text of Clause 145, modified to match with Clause 33.

Original section:

33.3.7.3 Input inrush current

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with V_{Port_PD} requirements as defined in Table 33–18, and ending when C_{Port} is charged to 99% of its final value. This period should be less than T_{Inrush} min per Table 33–11.

Type 2 PDs with pse_power_type state variable set to 2 prior to power-on shall behave like a Type 1 PD for at least T_{delay} min. T_{delay} starts when V_{PD} crosses the PD power supply turn on voltage, V_{On}. This delay is required so that the Type 2 PD does not enter a high power state before the PSE has had time to switch current limits from I_{Inrush} to I_{LIM}.

Input inrush current at startup is limited by the PSE if $C_{Port} < 180$ µF, as specified in Table 33–11.

If $C_{Port} \geq 180$ µF, input inrush current shall be limited by the PD so that I_{Inrush_PD} max is satisfied.

Replace 33.3.7.3 as follows:

33.3.7.3 Input inrush current

The PD inrush time duration is defined as beginning with the application of input voltage at the PI when V_{PD} crosses the PD power supply turn on voltage, V_{On_PD} as defined in Table 33–18, and ends after T_{delay}.

The inrush current is the initial current drawn by the PD, which is used to charge C_{Port}. A PD may limit the inrush current below I_{Inrush_PD} to allow for large values of C_{Port}.

The PSE either uses the legacy power up method, whereby it limits the inrush current to I_{Inrush} until the PD input voltage reaches 99% of steady state, or it limits the inrush current for a fixed amount of time, T_{Inrush}, as defined in Table 33–11. See legacy_powerup in 33.2.4.4.

PDs shall draw less than I_{Inrush_PD} from T_{Inrush} min until T_{delay}, when connected to a source that meets the requirements of 33.2.7.5. This delay is required so that the PD does not enter a high power state before the PSE has had time to change the available current from the POWER_UP to the POWER_ON limits. A PD can meet this requirement by either having C_{Port} charged within T_{Inrush} min or by limiting the input inrush current.

PDs with pse_power_type set to 1 shall conform to P_{Class_PD} and P_{Peak_PD} requirements within T_{Inrush} min as defined in Table 33–11. PDs with pse_power_type set to 2 shall not exceed Class 3 P_{Peak_PD}, as defined in Table 33–18, from T_{Inrush} min until T_{delay}.