FPGA Verification of CFEC for 400GbE 80km objective

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Outline

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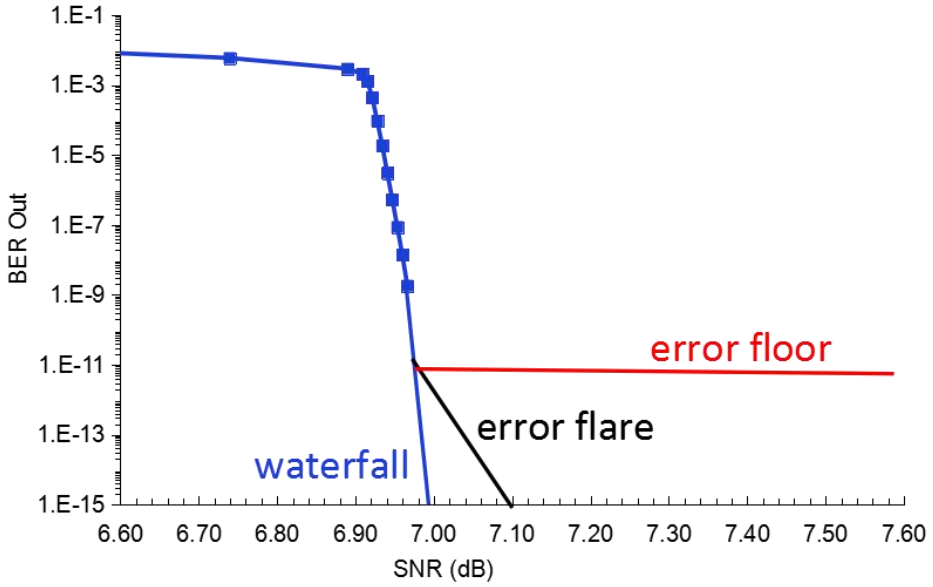
- FPGA Implementation of the CSHC Codec
- CSHC Performance emulations with the FPGA Platform
- Summary

Investigating FEC Performance at Ultra-Low BER

Challenges:

- High-throughput long-term measurement to observe enough error events
- Noise source with stable control of SNR and accurate AWGN statistics
- High confidence level of FEC performance emulations at ultra-low BER



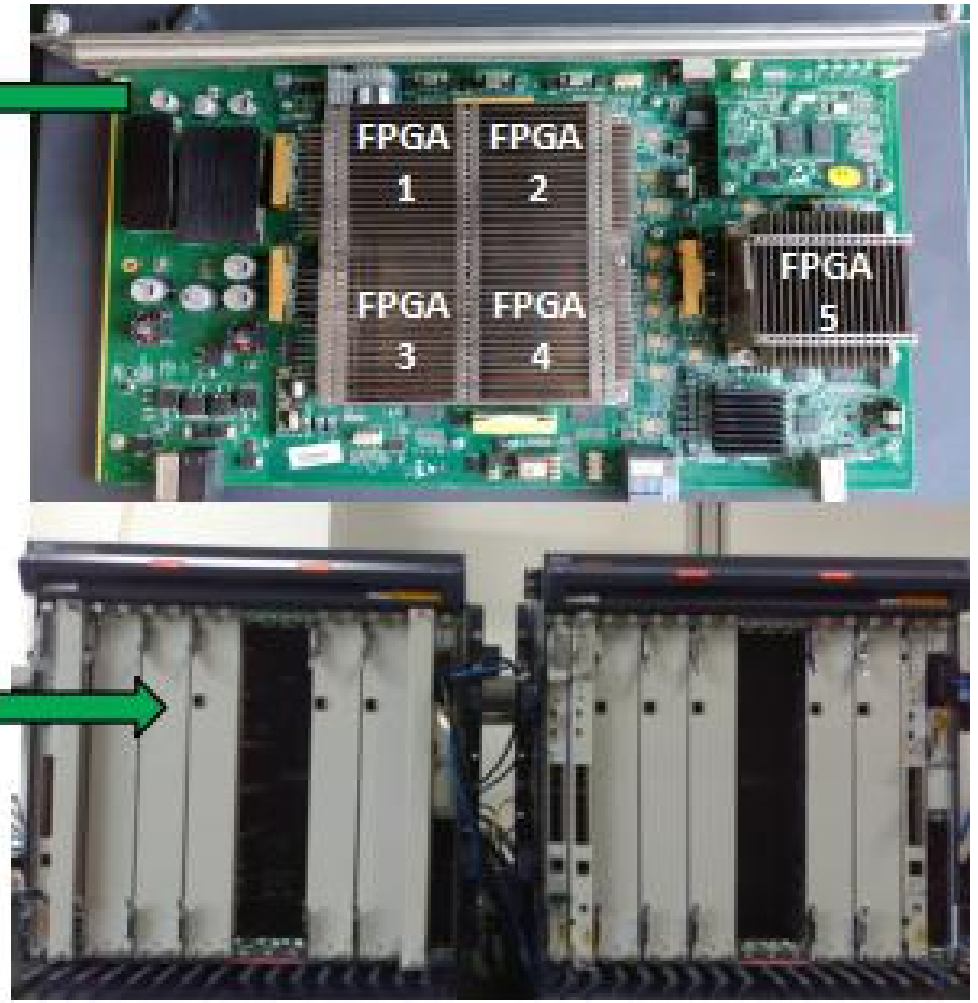
Solutions:

- **200Gbps throughput platform**
- **Digital noise sample generation**
- **Converging criterion**

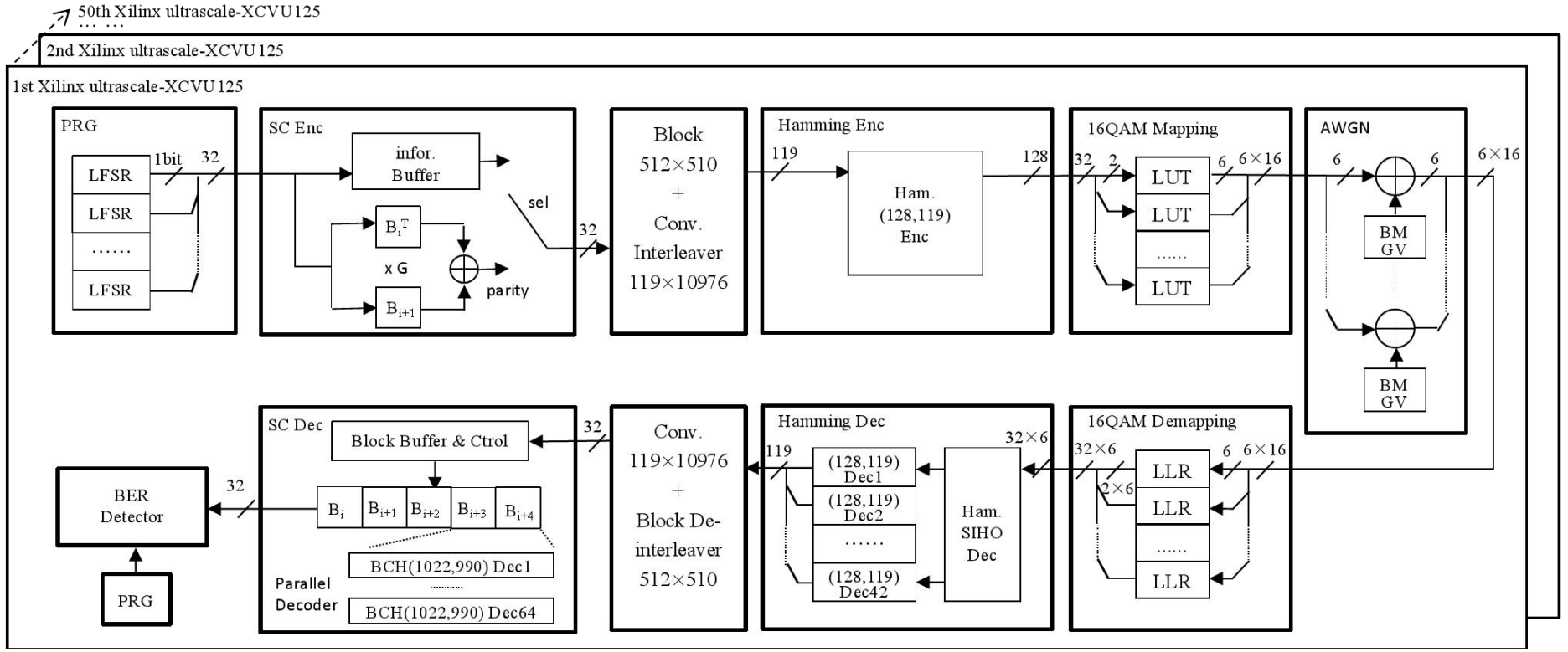
200Gbps FPGA Emulation Platform

5 ultrascale-XCVU125 on each FPGA board provide 20Gbps throughput

10 FPGA boards provide in total 200Gbps throughput



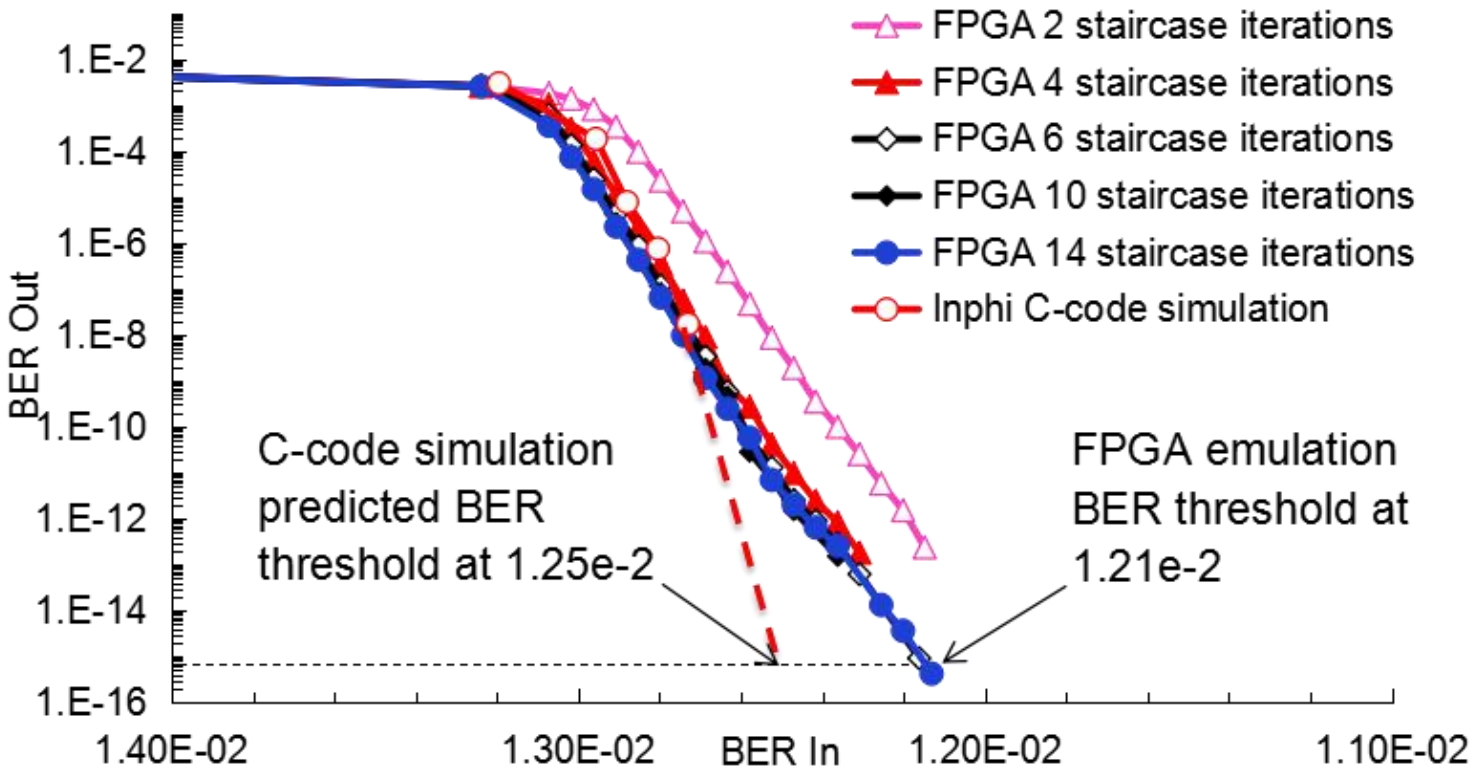
FPGA Implementation of the CSHC Codec



On each of the 50 FPGA chips, the implementation occupies

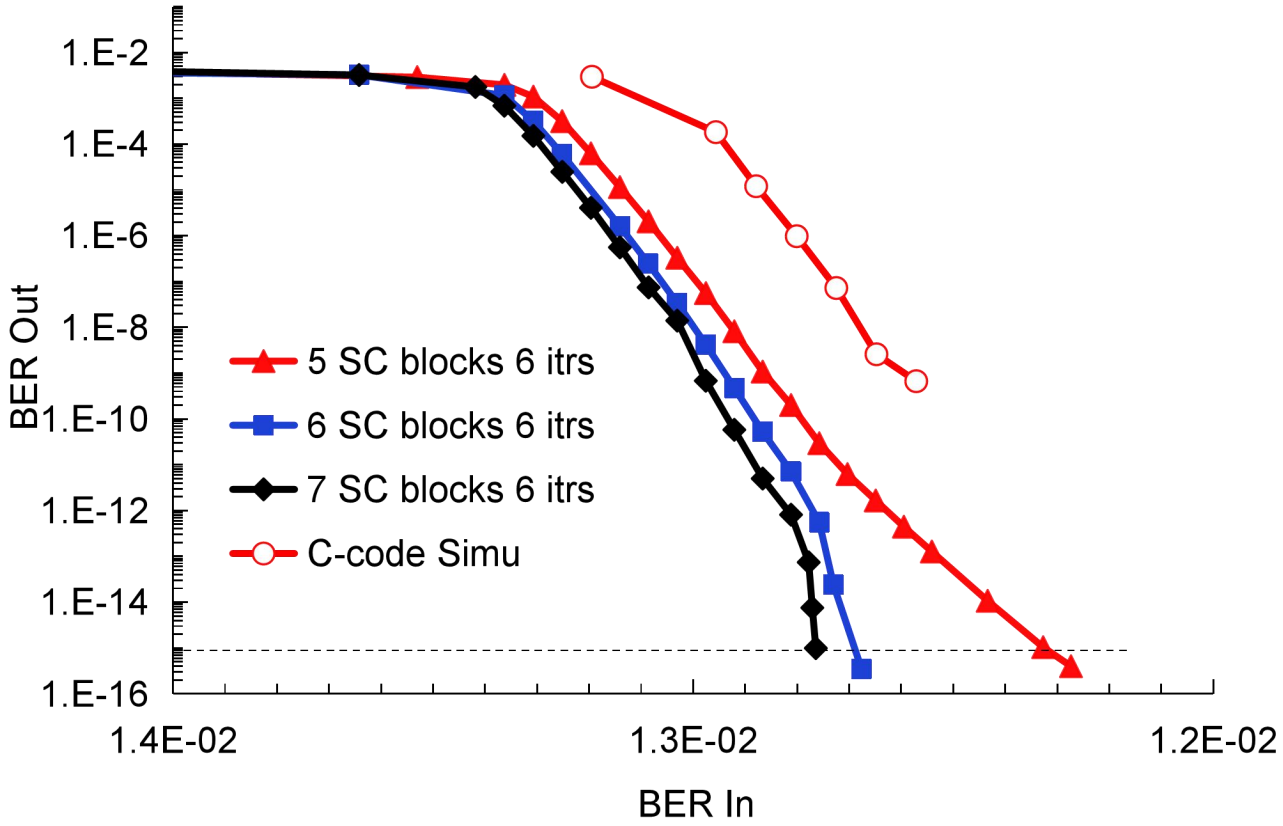
- 405K CLB (8 x 6-input LUT + 16 flip-flops / CLB)
- 1050 on-chip block memories (36K bits/block)
- 64 multipliers

1st Round FPGA Emulations on CSHC Performance



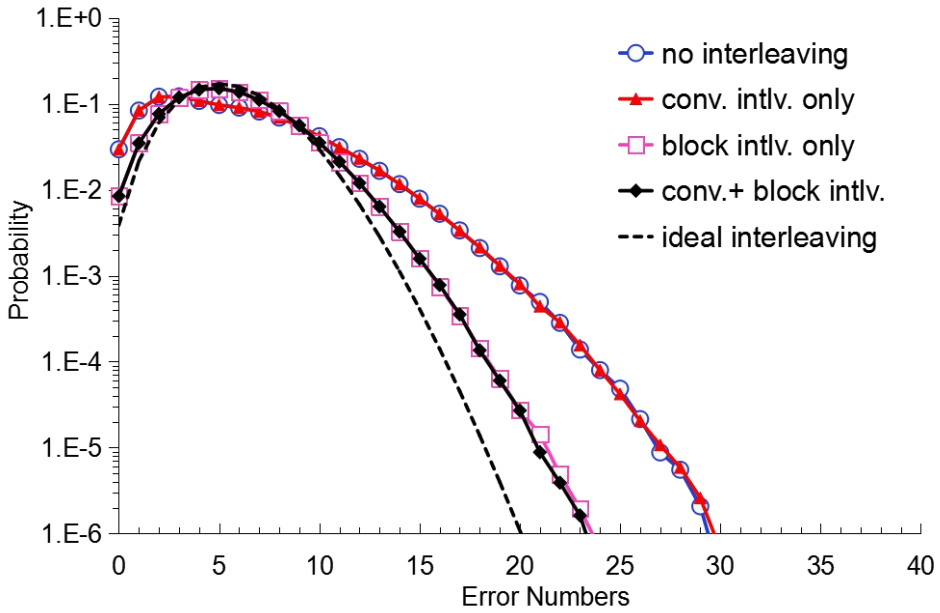
- The optimal number of staircase iterations in the CSHC is 6
- No severe error floor above 10−15 BER
- An error flare around 10−10 BER is revealed

2nd Round FPGA Emulations on CSHC Performance

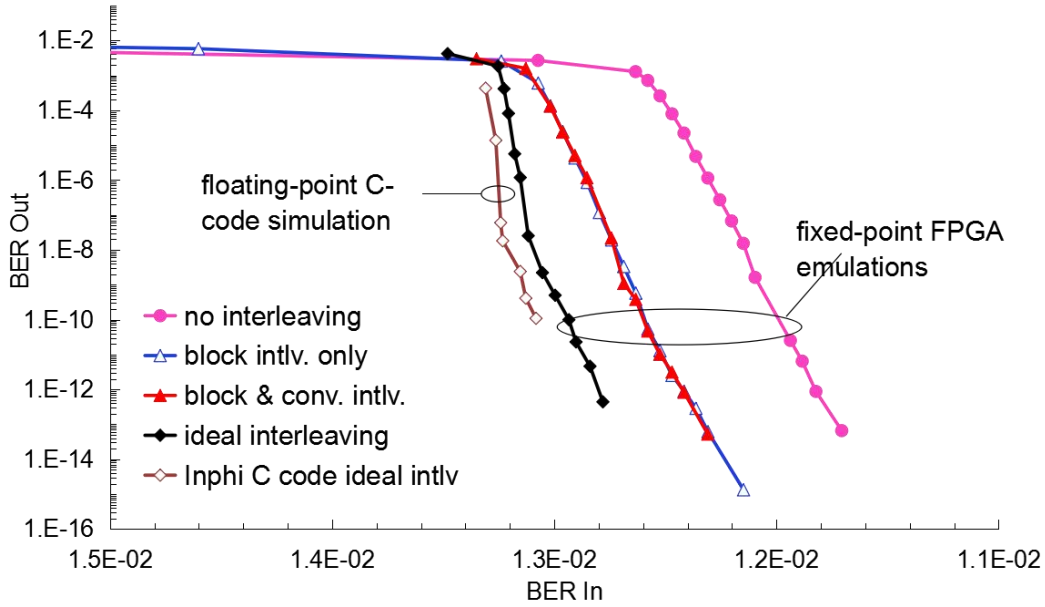


- Limiting fixed-point bit-width of input samples improves CSHC performance
- More staircase blocks in coding buffer improves error flare performance
- It seems a good tradeoff to increase the number of SC blocks from 5 to 6

Investigation on Interleaving and Error Flare



error statistics in ext. BCH (1022, 990)



- The no-interleaving case has the longest tail of error distribution
- The block interleaving is the one that randomizes errors at the decoder input
- Comparison to the ideal case shows margin for further improvement

- Disabling interleaving causes significant degradation
- FPGA emulations reveal an error flare even with ideal interleaving
- C-code simulations show a similar trend assuming ideal interleaving

Summary

- A verification on the to be determined OIF 400G-ZR FEC solution is performed with a 200Gbps FPGA implementation. Since IEEE 802.3ct has chosen CFEC as the selection of 400GbE 80km FEC objective, the emulation results can be used as a reference to improve the performance of CFEC

- The optimal number of iterations in the CSHC outer decoding is shown to be 6

- An error flare at 10^{-10} BER is revealed for the CSHC, lowering its BER threshold from 1.25e−2 to 1.21e−2. An error flare of the outer staircase code in the implementation is also revealed, indicating a direction for further improvement

- 6 SC decoding buffer seems a balanced tradeoff, of which however an optimal framing and latency design is different from the current 5-SC-block proposal

Thanks!