Bit-error monitoring for FEC protected interfaces

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Intro

- Review of Clause 91 & 119 RS FEC Monitoring
- Justification for pre-FEC bit-error ratio monitoring
- Recommendations for FEC monitoring for 100GBASE-ZR

Comments being addressed

Cl **45** *SC* **45.2.1.186** *P* **45** *L* **24** # 14

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Comment Type **T** *Comment Status* **D**

SC-FEC needs counters defined to allow monitoring pre-FEC BER. Counters for corrected bits (pre-Fec bit-errors) and total bits would provide this.

SuggestedRemedy

Add 64 bit counters for these

Proposed Response *Response Status* **O**

Cl **153** *SC* **153.2.5** *P* **93** *L* **30** # 15

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Comment Type **T** *Comment Status* **D**

Table 153-2 should define registers for calculating pre-FEC BER.

SuggestedRemedy

Add corrected bits and total bits to Table 153-2

Proposed Response *Response Status* **O**

Monitoring for RS FEC

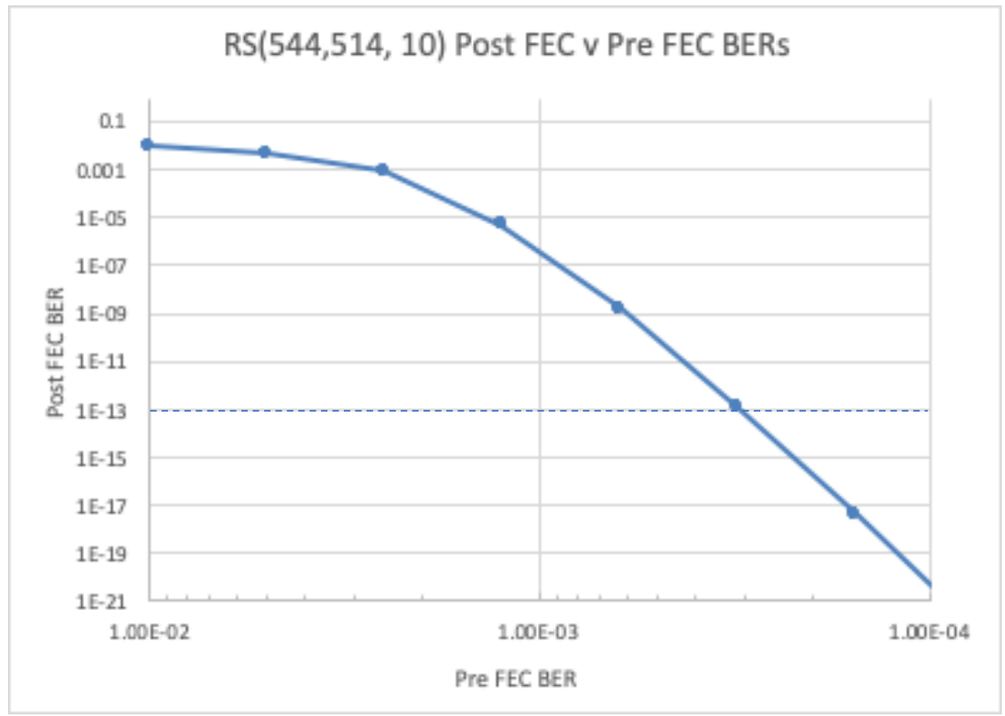
- Clause 91 and 119 included counts for Corrected Codewords, Uncorrected Codewords, and Symbol Errors
- Symbol error counts can be used to measure symbol error ratio
  - Approximation for Bit-error ratio

Table 119–5—MDIO/PCS status variable mapping *(continued)*

MDIO status variable	PCS register name	Register/bit number	PCS status variable
PCS FEC corrected codewords	PCS FEC corrected codewords counter register	3.802, 3.803	FEC_corrected_cw_counter
PCS FEC uncorrected codewords	PCS FEC uncorrected codewords counter register	3.804, 3.805	FEC_uncorrected_cw_counter
PCS FEC symbol errors, PCS lanes 0 to *x*	PCS FEC symbol error counter register, lanes 0 to *x*	3.600 to 3.631	FEC_symbol_error_counter_*i*

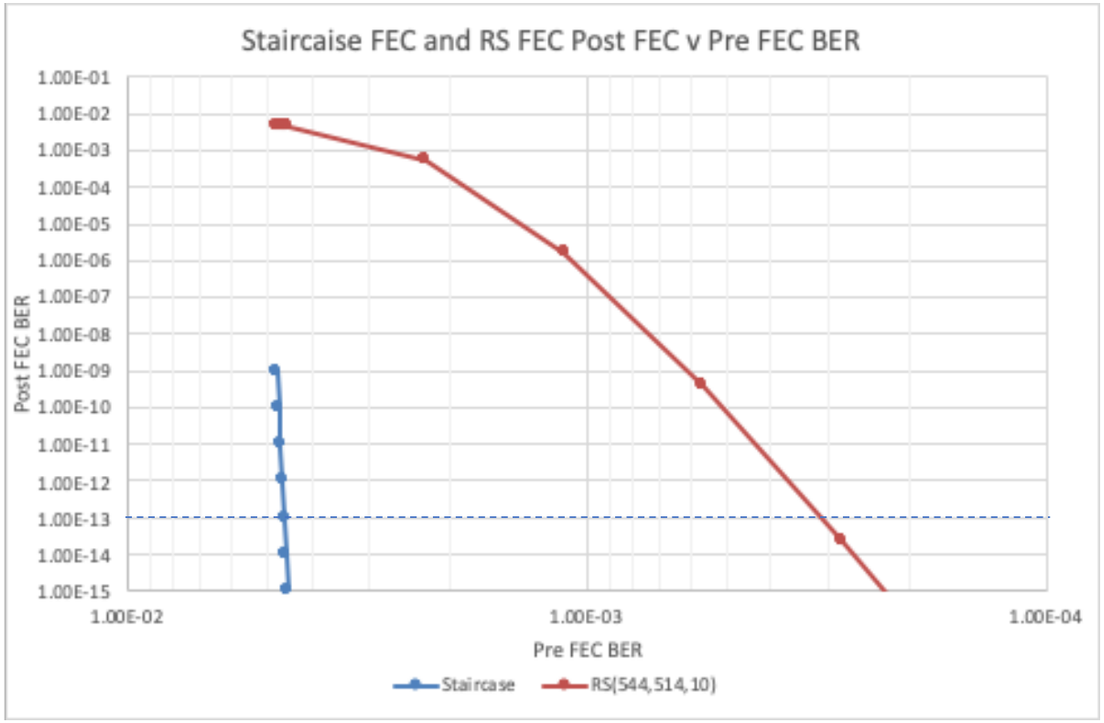
RS(544,514,10) BER

- Post FEC 1E-13 at Pre FEC ~3.1E-4
  - ~24s/bit-error post FEC for 400GbE
- Post FEC 2E-18 at pre FEC ~1.5E-4
  - ~14 days/bit-error post FEC for 400GbE
- < 0.5dBQ difference between these points
- Symbol Error count provides a means to determine operating margin



Staircase FEC performance

- Staircase FEC has a steep FEC threshold
- Monitoring of BER is needed to ensure there is sufficient operating margin
- This is especially important for DWDM systems that may be partially filled start of life



Staircase FEC Data from ITU-T G.709.2/Y.1331.2 (07/2018)

BER calculation

- Counts for corrected bits and total bits can be used for bit-error ratio calculation
  - Minimally corrected bits would be sufficient

- Time to saturate counters (times in seconds):
  - Assumes 1% BER for 100G & 2% BER for 400G

bits	100GBASE-ZR bits	100GBASE-ZR errors
32	0.04	4
48	2513	251317
64	1.65E+08	1.65E+10

bits	400GBASE-ZR bits	400GBASE-ZR errors
32	0.01	0.45
48	586	29320
64	3.84E+07	1.92E+09

Recommended parameters to add

- Table 45-150 includes:
  - FEC corrected codewords (32b) and FEC uncorrected codewords (32b)
- Recommend to add the following counters
  - FEC corrected bit counts (48b or 64b) RO, NR
    - The total number of bits corrected by the FEC algorithm
  - FEC total bit counts (48b or 64b) RO, NR
    - The total number of bits processed by the FEC algorithm