Filling in Clause 153 TBDs

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Staircase FEC Sublayer Delay Constraints

- From G.709.2, sum of FEC encoder/decoder latency is 7×512×510 bit times
- In Table 80-5 for SC-FEC sublayer delay constraints (page 51 line 18), and in clause 153.2.2 (page 82 line 22), replace TBDs with the following values:
  - 1 827 840 bit times
  - 18 278.40 ns
  - 3570 pause quanta

Probability of Undetected Uncorrectable Error

- Not tractable using analytical formula, need simulation analysis
- We ran Monte-Carlo simulation on a realistic implementation of Staircase FEC decoder
- Uncorrectable FEC block errors are detected using 512 syndrome calculations on the output 512x512 block
- Results below show all but one uncorrectable error blocks were detected in simulation

BER_in	Number of Block Errors	BER_out	Undetected Block errors
4.88E-03	4.23E+07	3.04E-05	1
4.80E-03	1.38E+06	2.95E-08	0
4.75E-03	1.21E+05	1.34E-09	0
4.70E-03	4.50E+04	1.69E-10	0
4.65E-03	2.18E+03	2.62E-11	0

- **Probability (undetected block error | block error occurred) < 1e-6**

(assume P=1e-6 => probability one or fewer undetected block errors in sims ~ 3e-18 is very unlikely)

In the last paragraph of 153.2.3.3.4 (page 89 line 22)

- Replace 10^{-TBD} with 10^{-6}

THANKS!