802.3cu D2.0 PMD Spec Proposed Changes

P802.3cu 100 Gb/s and 400 Gb/s over SMF at 100 Gb/s per Wavelength Task Force
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Introduction

- During the 802.3cu January Interim meeting, D1.1 changes were adopted based on proposals in the following:

  http://www.ieee802.org/3/cu/public/Jan20/cole_3cu_01b_0120.pdf
- TDECQ - 10log10(Ceq) was removed from Clause 140 and 151 TX Specifications
- To make the spec consistent, SECQ - 10log10(Ceq) should be removed from Clause 140 and 151 RX specifications
- The reasons are the same as presented in January
  - The spec. is not useful
  - The spec. is redundant
  - The spec. is has poor correlation with real performance
- This deck is in support of related comments against D2.0

100G Clause 140 Receive Characteristics

Table 140–7—100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 receive characteristics

Description	~~Value~~ 100GBASE-DR	100GBASE-FR1	100GBASE-LR1	Unit
Signaling rate (range)	53.125 ± 100 ppm			GBd
Conditions of stressed receiver sensitivity test:[e]				
Stressed eye closure for PAM4 (SECQ)	3.4	3.4	3.4	dB
SECQ – $10\log_{10}(C_{eq})$[f] (max)	3.4	3.4	3.4	dB

[f] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

400G Clause 151 Receive Characteristics

Table 151–8—400GBASE-FR4 and 400GBASE-LR4-6 receive characteristics

Description	400GBASE-FR4	400GBASE-LR4-6	Unit
Signaling rate, each lane (range)	53.125 ± 100 ppm		GBd
Conditions of stressed receiver sensitivity test:[e]			
Stressed eye closure for PAM4 (SECQ), lane under test	3.4	3.5	dB
~~SECQ – $10\log_{10}(C_{eq})$, lane under test (max)~~	~~3.4~~	~~3.5~~	~~dB~~
OMA_{outer} of each aggressor lane	1.5	–0.4	dBm

151.8.11.2 Stressed receiver conformance test signal characteristics and calibration

The stressed receiver conformance test signal characteristics and calibration methods are as described in 121.8.9.2 with the following exceptions:

— The required values of the "Stressed receiver sensitivity (OMA_{outer}), each lane (max)", "Stressed eye closure for PAM4 (SECQ), lane under test", ~~"SECQ – $10\log_{10}(C_{eq})$ (max), lane under test"~~, and "OMAouter of each aggressor lane" are as given in Table 151–8 for 400GBASE-FR4 and 400GBASE-LR4-6.

Appendix

The material on the following pages has **NOT** been reviewed or commented on by the supporters listed on page 2.

There is **NO** support, non-support, or opinion of any kind, implied or otherwise by any of the supporters.

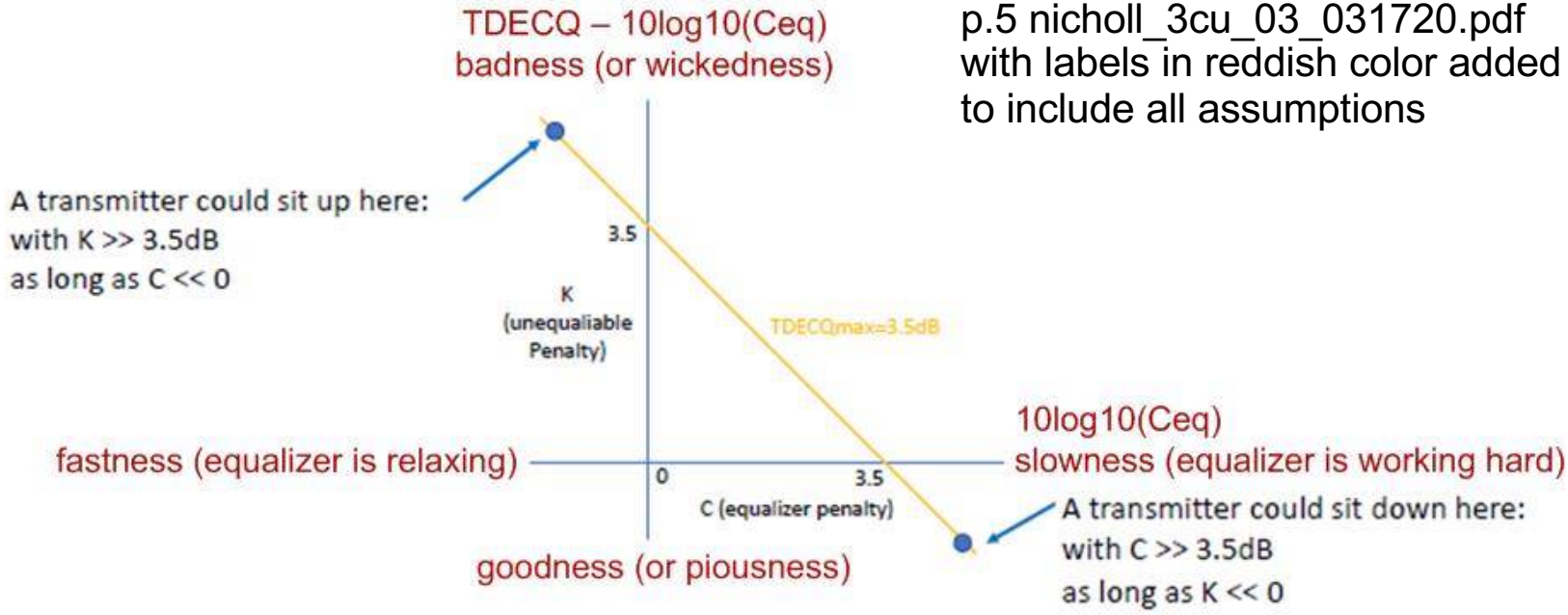
A1: January Interim Presentation Clarification

- One of the conclusions in the 802.3cu January Interim presentation is the following:

  http://www.ieee802.org/3/cu/public/Jan20/cole_3cu_01b_0120.pdf#page=11
- Several comments were received after the meeting pointing out that the heading has a spelling error
- The word “UND” is in the original artwork downloaded from the web, AND is there intentionally as a self-deprecating element in subtle contrast to the categorical tone of the complete statement

A2: TDECQ - 10log10(Ceq) Spec Basis

- Gary's 3/17/20 presentation clarifies the complex arguments used in support of TDECQ - 10log10(Ceq) spec
- It shows that the assumptions are all in the plot of TDECQ - 10log10(Ceq) = K vs. 10log10(Ceq) = C (see below)
- This plot is on nearly every page of every proposal



p.5 nicholl_3cu_03_031720.pdf
with labels in reddish color added
to include all assumptions

A2: TDECQ - 10log10(Ceq)

- Penalty quantifies the difference in device operation at two different operating conditions, as measured by BER, or as correlated to BER.
- No BER based penalty measurements have been presented to support the spec proposal; just hypothesis and simulation
- The K >> 3.5dB “bad” points are in the “fastness” TX, left half plot area, but we don’t have such 100G TXs to measure
- The K << 0dB “great” points are in the “goodness” TX, lower half plot area, but we don’t have such 100G TXs to measure
- Presented 50G PAM4 TX data shows that TDECQ – 10log10(Ceq) has poor correlation to actual performance

A2: 10log10(Ceq)

- At this point, there is broad understanding of Ceq, including its mathematical relation to TX bandwidth and overshoot.
  http://www.ieee802.org/3/cu/public/Jan20/cole_3cu_01b_0120.pdf#page=6
- Historically, slow & fast TX corners have been constrained
  http://www.ieee802.org/3/cu/public/Jan20/cole_3cu_01b_0120.pdf#page=17
- Rise/fall time spec limits the slow corner
- Tap weight spec limits the fast corner insufficiently
  - implementation dependent
  - constrains internal design by inverse transform of taps
  - ex. low-cost integrated TX with no FIR and DAC circuit
- General specification methodology is to limit externally measurable behavior, referred to as black box
- Standard upper/lower “eye” spec limit does this

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Thank You