400GBASE-ZR PCS/PMA Content Overview

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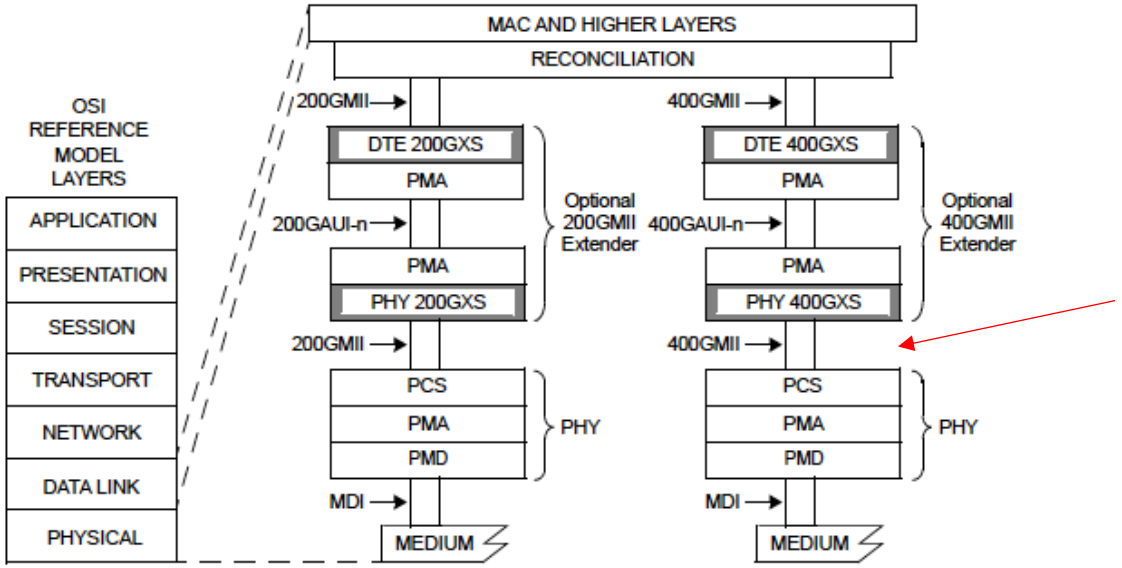
Overview

- A baseline has been adopted for the 400GBASE-ZR PCS/PMA, based on the OIF 400ZR framing
- The adopted baseline is somewhat disconnected from the existing 802.3 clauses.
- The issue and possible methods to address it are discussed

Clause 118 100G XS



XS provides an MII interface into the 400G PCS

The Extender sublayer is based on the 400GBASE-R PCS, to allow an interface between the MAC and a PCS

400GBASE-R PCS

Extender sublayer is based on 400GBASE-R PCS

Blocks are implemented by reference to 400GBASE-R PCS

400GMII

400GAUI

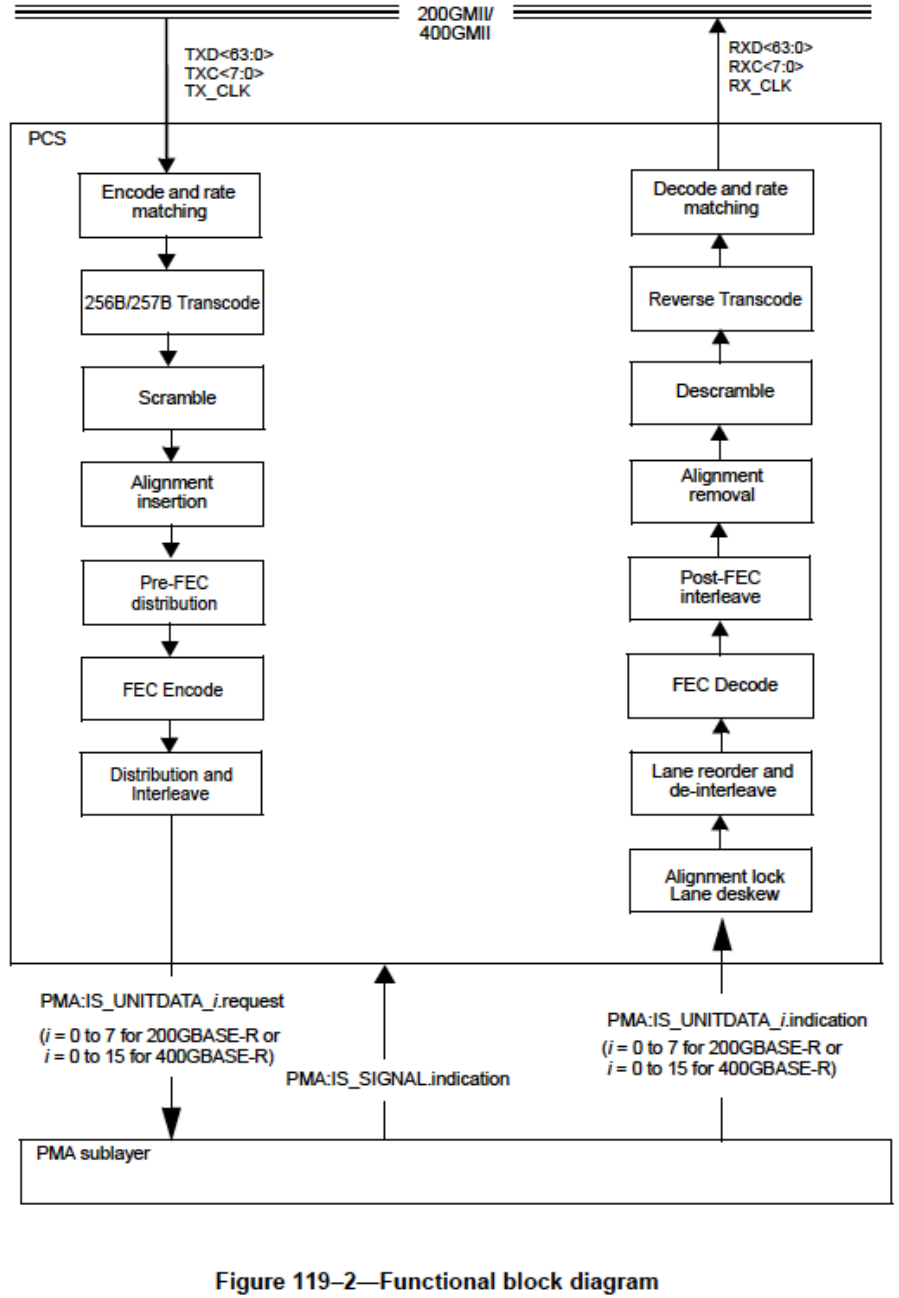
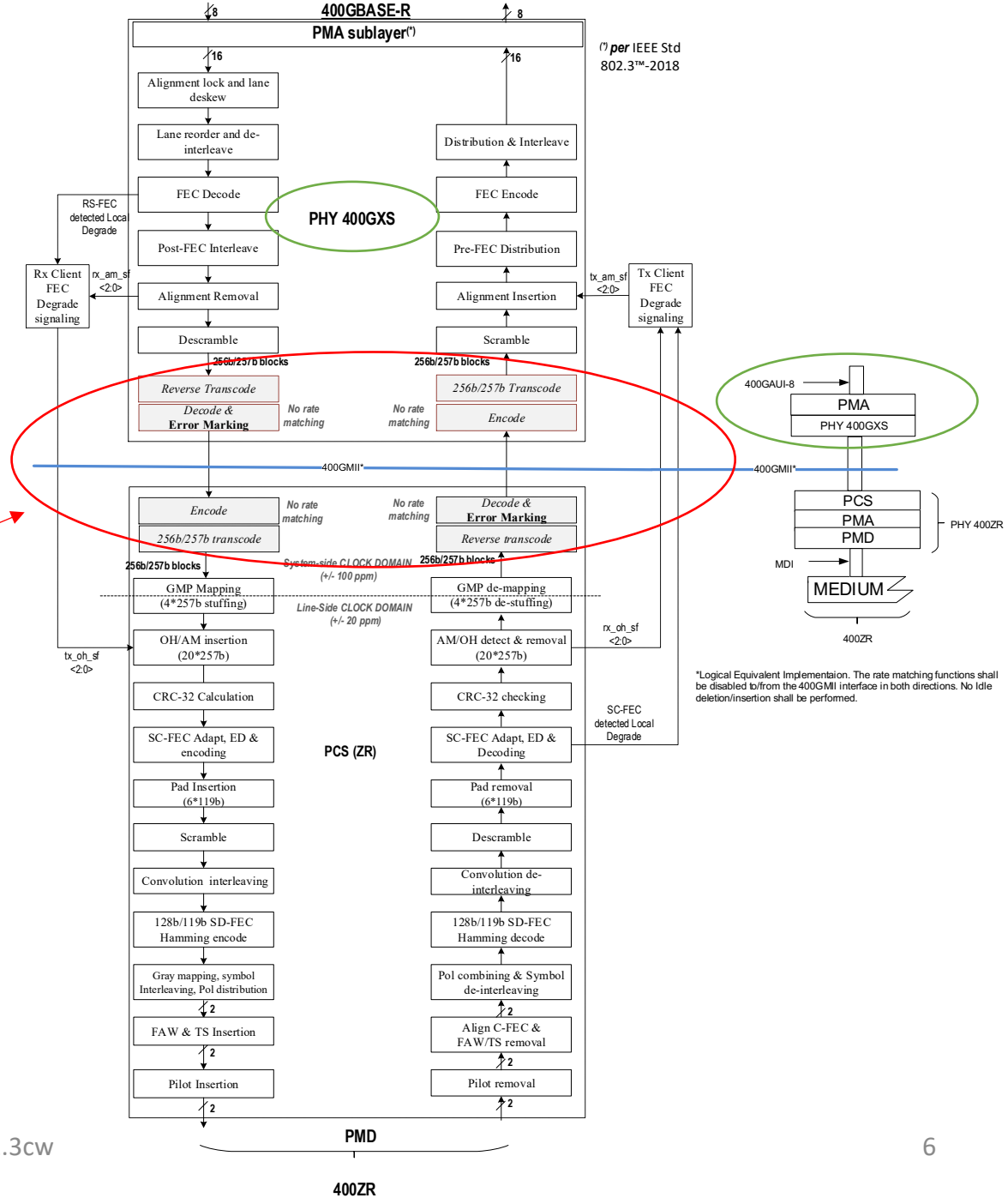


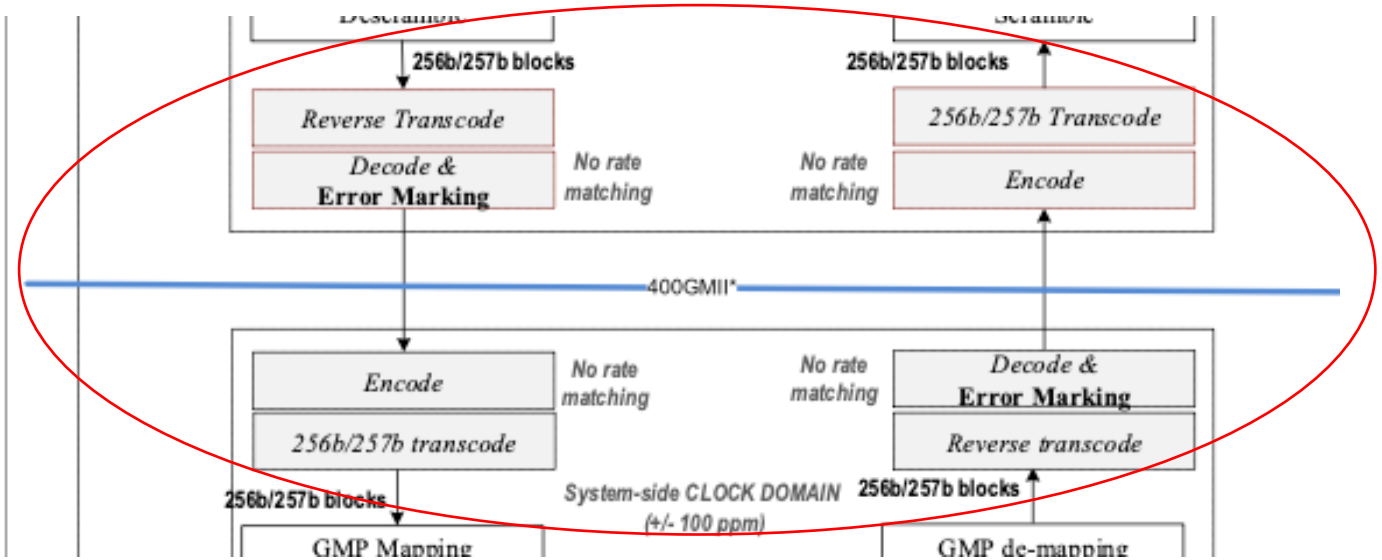
Figure 119–2—Functional block diagram

OIF 400-ZR Logic Flow

- 400ZR performs a partial PHY XS function
- Intersublayer connections are not MII
- Some blocks are not implemented



OIF 400ZR bypassed functions

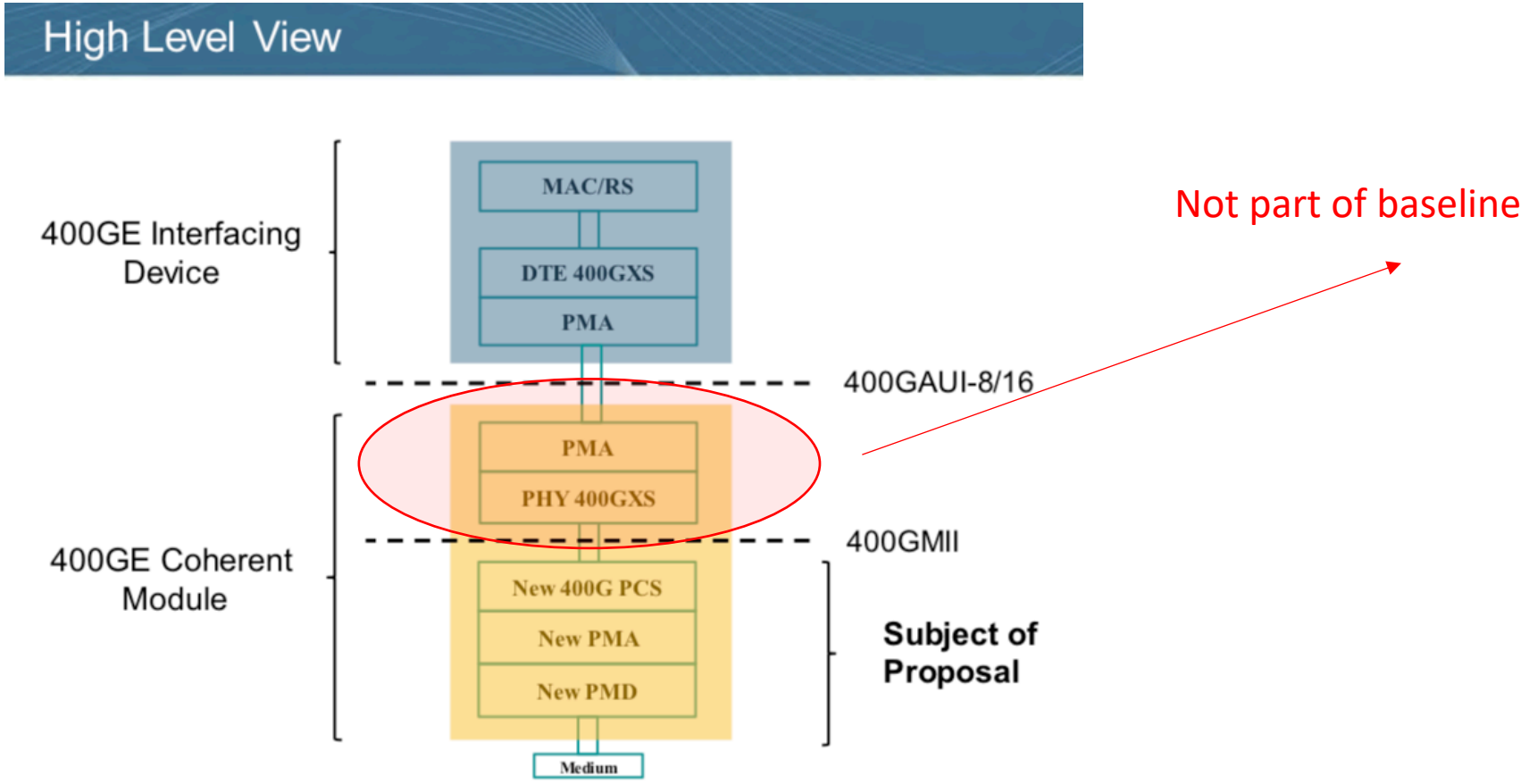


- Functional blocks adjacent to MII are bypassed
- These blocks implement rate adaptation, transcoding, and Error Marking
- Connection from partial XS to PCS is in the 257b domain without FEC
- Error marking is performed elsewhere in the chain, in the 256/257b blocks

Agreement in 802.3cn

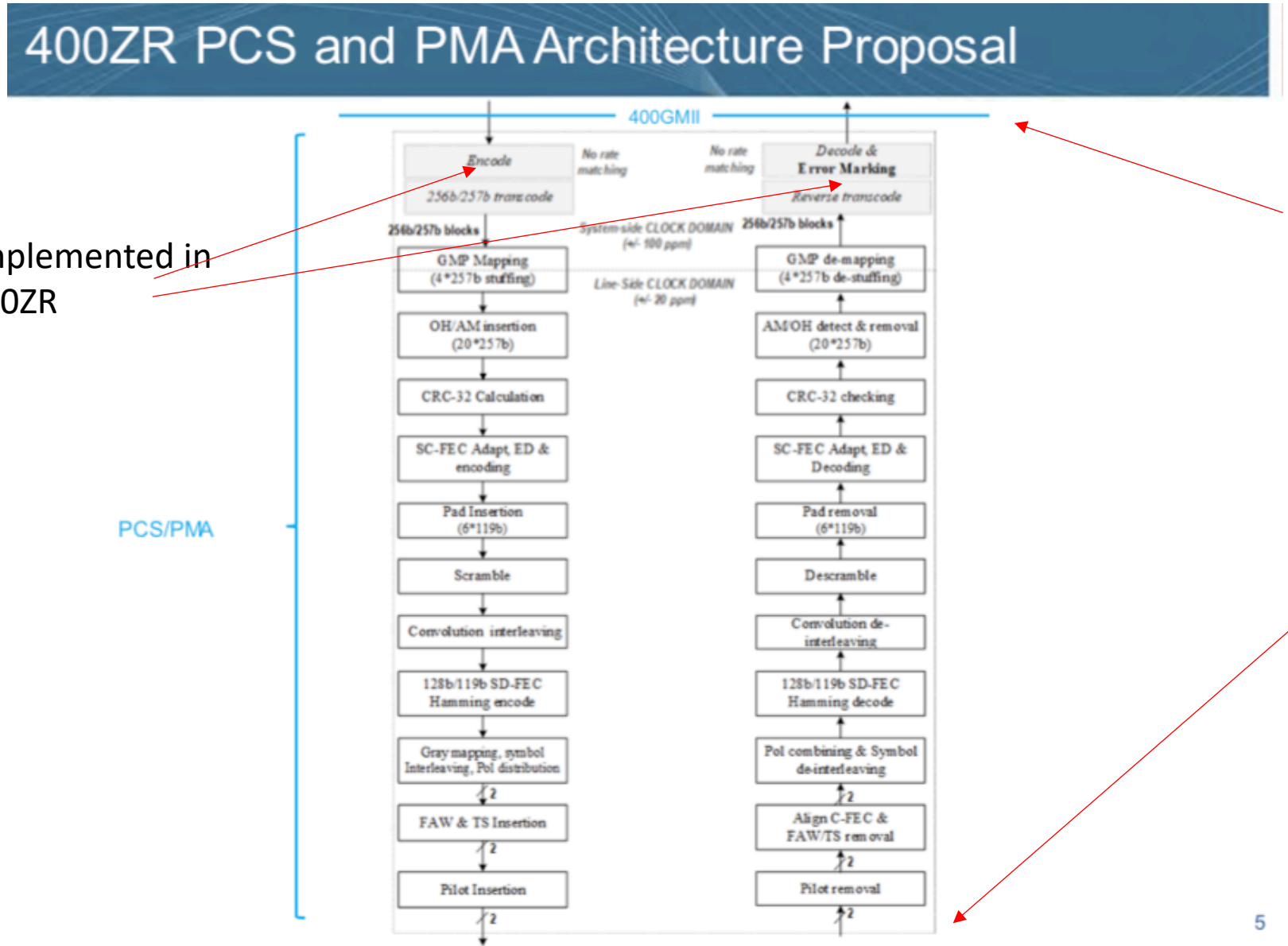
- 400GBASE-ZR PCS/PMA Baseline Proposal was adopted
  - http://www.ieee802.org/3/cn/public/19_01/lyubomirsky_3cn_01b_0119.pdf

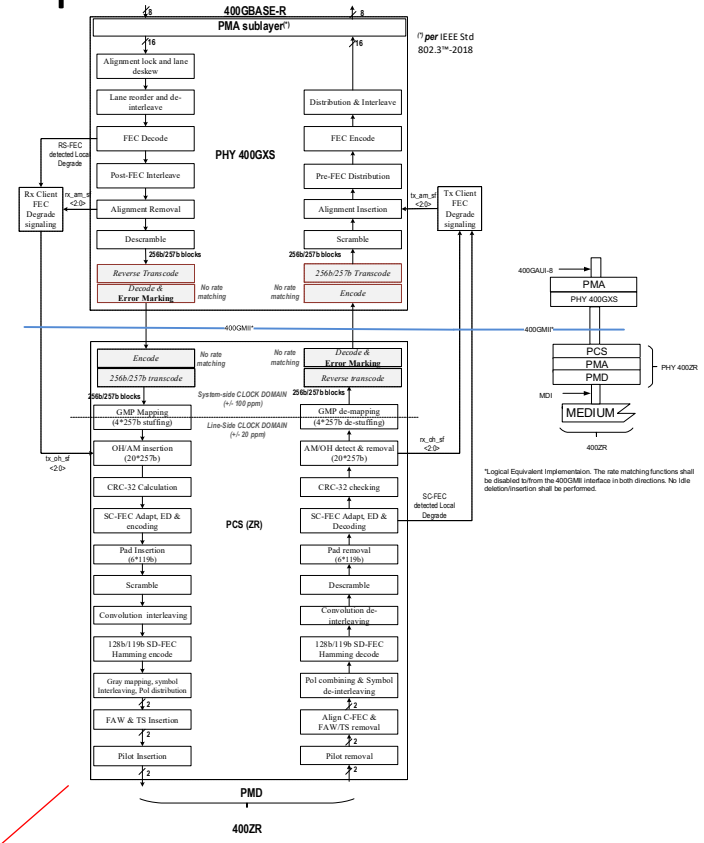
From 400GBASE-ZR Adopted PCS/PMA Baseline Proposal



From 400GBASE-ZR PCS/PMA Adopted Baseline Proposal

Not implemented in OIF 400ZR





Issues with adopted baseline

- The adopted baseline has an inter-sublayer connection at the MII
- The adaptation from the 400GAUI-n to the MII is performed by the clause 118 XS in a module implementing 400GBASE-ZR
- The actual connection used in OIF 400ZR is not at the MII but is instead in the 256/257b transcoded domain
  - The connection from the 400GAUI is performed using a partial XS

Paths forward

1. Adopted approach would require an MII connection

   → While we could continue this approach, it implies the potential for rate adaptation and error marking in the 64/66b blocks

2. An Inverse RS-FEC clause could be created, with a logical intersublayer interface based on 256/257b blocks without FEC

   →This is a new logical interface

   →Similar to approach used for 100GBASE-ZR

3. The 802.3cw clause 155 400GBASE-ZR PCS could begin at the PMA attached to the 400GAUI-n, incorporating all necessary blocks between the 400GAUI-n and the PMD.

   → This is similar to OIF IA and is more of a module view

Discussion

- After some discussion it seems that option 1 would be largely indistinguishable from the OIF implementation
  - An OIF implemented module at one end of a link could interop with a module implementing a full Extender Sublayer / MII connection
- In a module implementation a logical connection at the transcoded rate without FEC would likely be implemented, which differs from the adopted baseline
- The existing baseline would be potentially useful for 400GBASE-ZR implemented in other non-module applications

Thanks!