Laning and OAM - update

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“How to lane”?

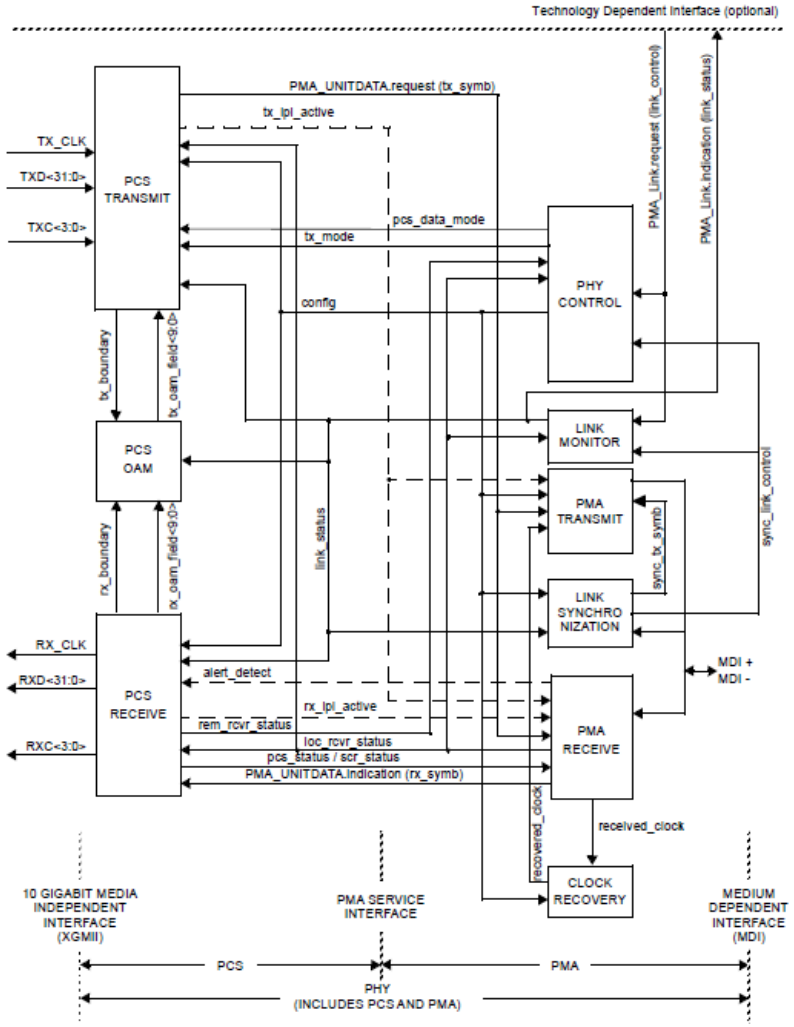
- Several choices:
  - Lane PMA only as a unit? (combine at FEC) (like Cl 55)
    - Similar to BASE-T model, although FEC isn’t separate sublayer
  - Lane PMA & FEC as a unit? (combine at PCS) (like Cl 91 & 94)
    - Allows integration and repetition of a PMA/FEC with independent BER
  - Lane PMA/FEC/PCS as a unit? (combine at RS) (Cl 143)
    - Allows independent PHY units to be bonded
    - PCS & FEC can still be internally laned if needed, independent of PMA

Basic Functional Splits

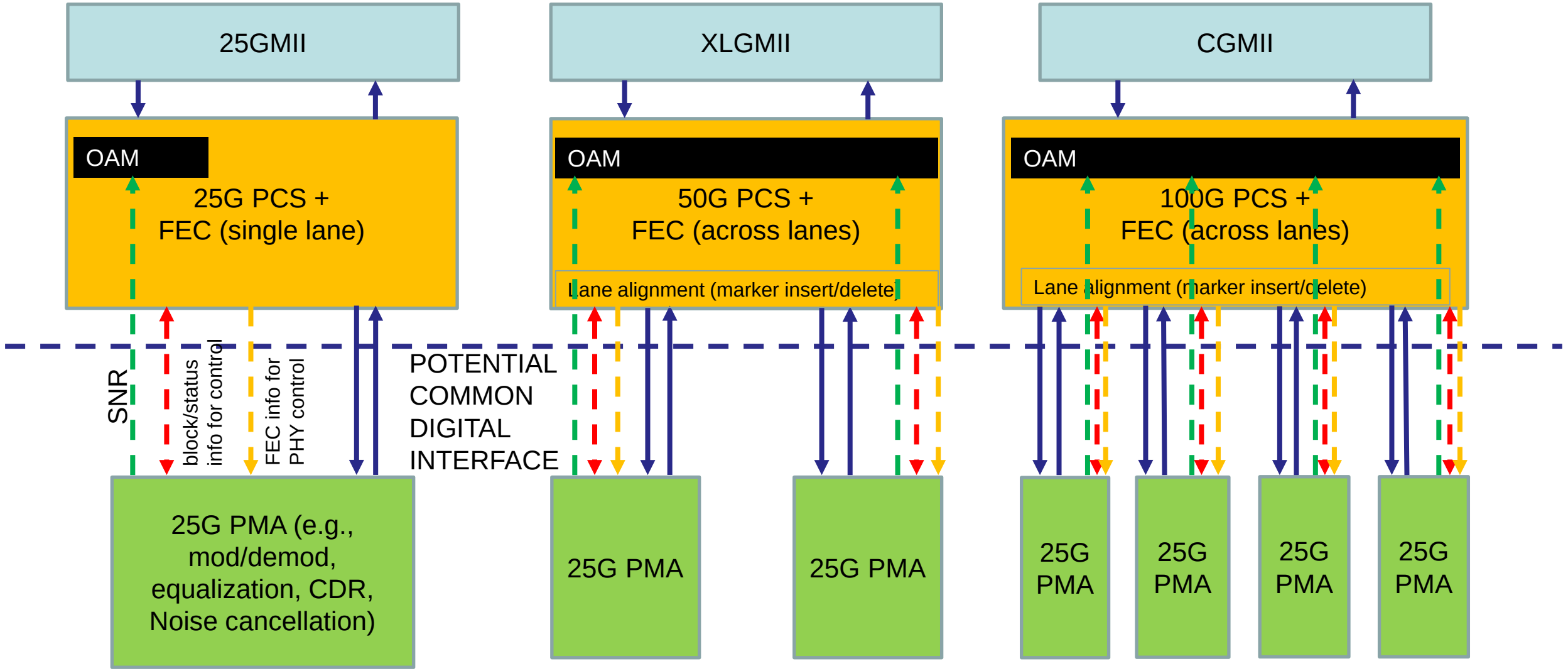
- PCS
  - Encode xMII commands and data into blocks for transmission (e.g., 64B/65B)
  - Lane separation, alignment, and combination
  - OAM encoding/packing into data blocks/PHY frames
- FEC
  - Encoding/Decoding for Error correction and detection
- Bit grouping for PMA symbols traditionally in PCS, actually in PMA
- PMA
  - Modulation/precoding – translation of code groups to pulse levels, generating waveform to transmit
  - Demodulation/equalization – conversion of received analog waveforms to bit groups
  - Noise cancellation & filtering – echo cancellation, crosstalk or EMI cancellation
  - A/D, D/A conversion, Clock generation/recovery, Pulse shape, filtering

Clause 149 PCS & PMA Exchange Information

- Cl. 149 PCS and PMA exchange:
  - pcs_data_mode
  - tx_mode
  - config
  - link_status
  - (tx & rx) lpi_active, alert_detect
  - (loc & rem) rcvr_status
- Info not shown here:
  - PHY Health (for OAM SNR info)
  - PCS block lock (for PHY control)
- From FEC:
  - hi_rfer (to PMA for PHY control)
  - RS-FEC frame errors (to PCS for OAM)



Lane PMA Only



Pros/Cons – Lane PMA

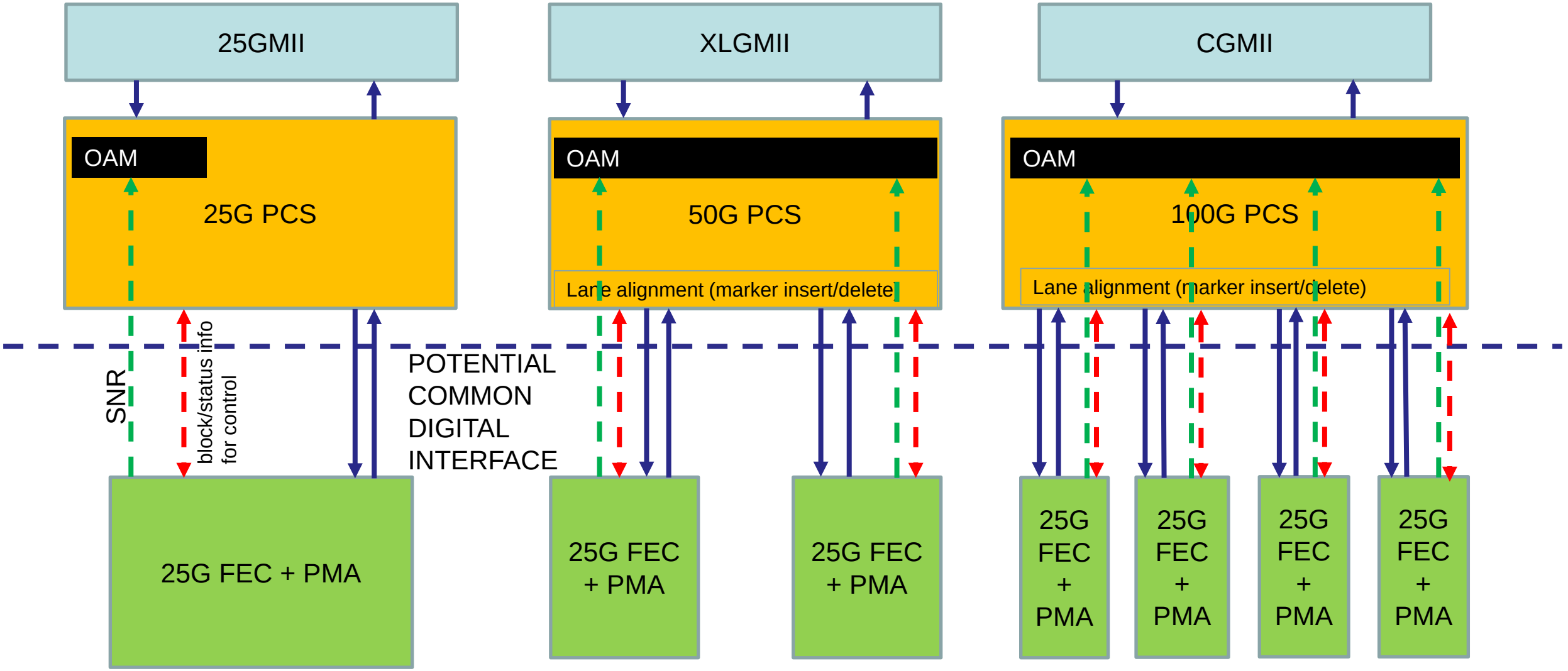
PRO

- Allows coding across pairs
  - Better uncorrelated noise protection
- Separates design at traditional PCS/PMA boundary
  - Natural specification of common digital interface
- Potentially smallest “PHY” silicon
- FEC and PCS may be combined
- Potential for clean, standard digital interface for all 25G PHY units

CON

- May require lane alignment prior to FEC decoding
- Requires code block length (with any interleaving) to scale as rate
- Speed-dependent FEC & PCS
- PMA operation cannot rely on PCS & FEC specifications (robust against noise)
- Potential misalignment between FEC and PMA bit groups
- Even 25G PHY exists in 2 parts
- Need to resolve multi-phy SNR in OAM
- SNR information for OAM crosses laning interface
- Numerous control signals cross laning interface in both directions

Lane PMA + FEC


25GMII
XLGMII
CGMII
OAM
OAM
OAM
25G PCS
50G PCS
100G PCS
Lane alignment (marker insert/delete)
Lane alignment (marker insert/delete)
SNR
block/status info for control
POTENTIAL COMMON DIGITAL INTERFACE
25G FEC + PMA
25G FEC + PMA
25G FEC + PMA
25G FEC + PMA
25G FEC + PMA
25G FEC + PMA
25G FEC + PMA

Pros/Cons – Lane PMA + FEC

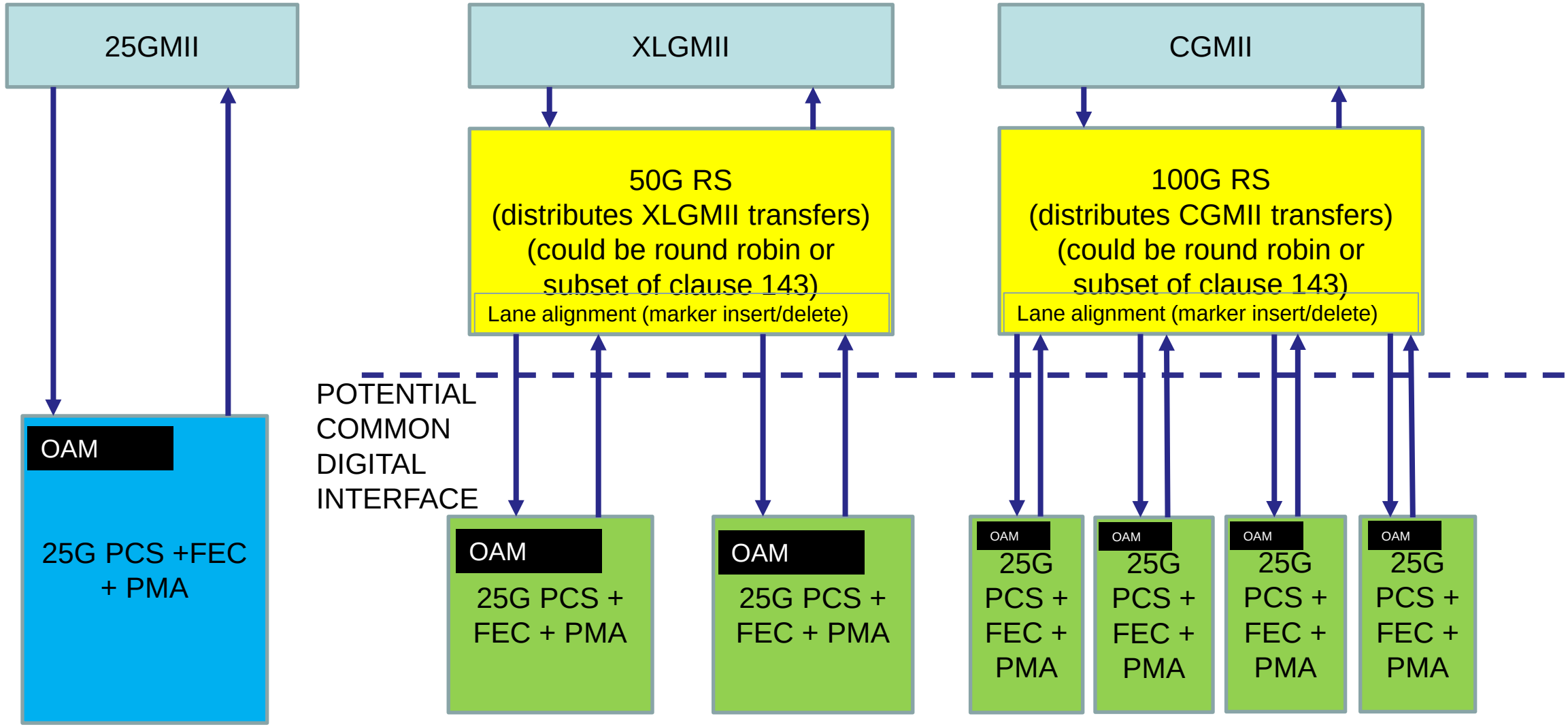
PRO

- PMA subunit gets benefit of FEC
- FEC block length independent of laning without interleaving
- PMA can benefit from FEC operation/decoding statistics
  - FEC information available to PMA directly for PHY control/status
- Lower rate, Speed-independent FEC
- Cleaner tie between FEC bit grouping and PMA bit grouping
- Potential for clean, standard digital interface for all 25G PHY units

CON

- No benefit from decorrelation of noise on other pairs
- Hard to do crosstalk cancellation
- Speed-dependent PCS
- FEC must be below PCS in layering, cannot be above or combined
- Even 25G PHY exists in 2 parts
- SNR information for OAM crosses laning interface
- block_lock, lpi_active, and rcvr_status signals cross laning interface (both directions)

Lane PMA + FEC + PCS



Pros/Cons – Lane PMA + FEC + PCS

PRO

- Full 25G PHY as atomic unit
- Shared digital interface only needed on higher speeds
- Full PHY bit error protection on subunit
- Single-speed FEC & PCS
- All processing at 25G rate
- Easier subunit test, most modular
- Maximum 25G reuse
- All PCS OAM and PCS/FEC/PMA control information in one place

CON

- Largest “PHY” unit
- Need to define RS to do laning
  - Can borrow from existing clauses
- 25G PHY likely has a different interface to other chips/blocks than blocks used for other lanes

Discussion

- Recommendation:
  - Proceed with architecting laning on full PMA/FEC/PCS PHY basis
  - Extra interface makes difference
    - Vendors may still split their chipsets, but together they'd make an interoperable PHY (parts not interchangeable)
  - Reasonable minds may differ…

THANK YOU!