802.3cy
Update PCB and Test Fixture Considerations

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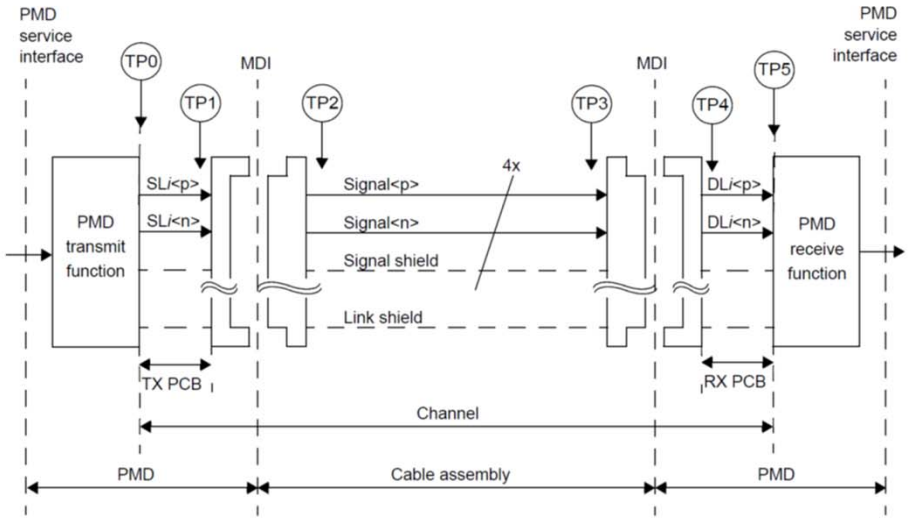
Purpose

- **Update 802.3cy PCB and Test Fixture Considerations**

Background – 802.3bj/by/cd/ck

- The channel is defined between the transmitter and receiver blocks to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly (link segment).
- Test points provide specification references for channel and cable assembly and RX and TX
- Test fixtures enable testing at test points – module compliance board (MCB); host compliance board (HCB)



Test points	Description
TP0 to TP5	The 100GBASE-CR4 channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 92–2. The cable assembly test fixture of Figure 92–17 or its equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 92.8.3 and 92.8.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 92.8.3.6.
TP2	Unless specified otherwise, all transmitter measurements defined in Table 92–6 are made at TP2 utilizing the test fixture specified in 92.11.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 92.8.4 are made at TP3 utilizing the test fixture specified in 92.11.1.

Background – 802.3bj/by/cd/ck

IEEE Standards - 25/50/100 Gb/s Operation – Shielded Cable

- 802.3bj - 100GBASE-CR4 - 2-level PAM - 25.78125 GBd per lane – Channel loss budget (35 dB@12.8906 GHz). Link segment up to at least 5 m (22.8 dB@12.8906 GHz)

- 802.3by - 25GBASE-CR and 25GBASE-CR-S - 2-level PAM - 25.78125 GBd per lane – Channel loss budgets (35 dB, 29 dB, 28.02 dB)@12.8906 GHz . Link Segments 3-5 m (22.48 dB, 16.48 dB, 15.50 dB)@12.8906 GHz reach depending on FEC

- 802.3cd - 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4– PAM4 - 26.5625 GBd per lane – Channel loss budgets 30 dB@13.28 GHz. Link Segment up to at least 3 m reach 17.6 dB@13.28 GHz.

- 802.3ck - 100GBASE-CR1, 200GBASE-CR2, and 400GBASE-CR4 – PAM4 - 53.125 GBd per lane – Channel loss budgets 28.5 dB@26.56 GHz. Link Segment up to at least 3 m reach 19.75 dB@26.56 GHz

Background –TP0-TP5 Channel

Test points	Description
TP0 to TP5	The 100GBASE-CR4 channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
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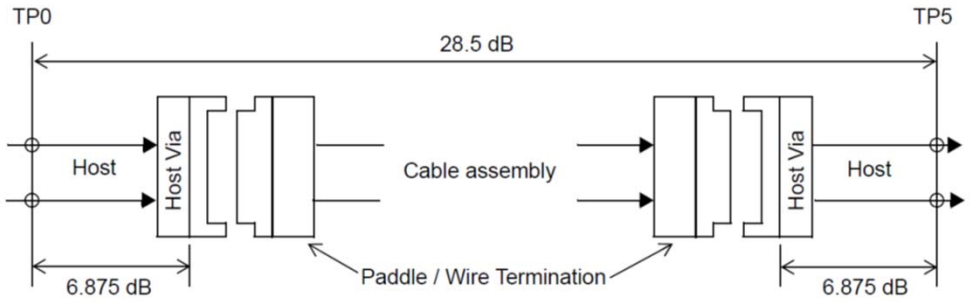

Channel IL = 28.5 dB @ 26.56 GHz = 2*(6.875+1.6)+11.55

NOTE—Channel IL derived from cable assembly host, and mated test fixture

Channel insertion loss at 26.56 GHz

Source: IEEE P802.3ck™/D2.0, 10th March 2021

Background –TP1-TP4 Cable Assemblies

Test points	Description
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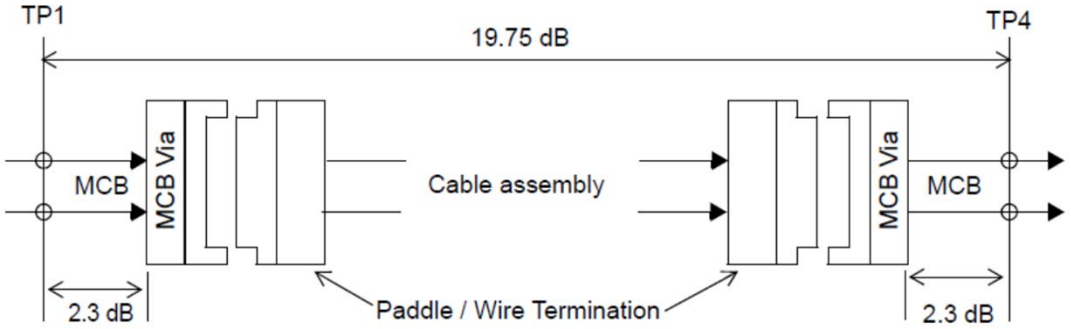

Cable assembly insertion loss at 26.56 GHz

Source: IEEE P802.3ck™/D2.0, 10th March 2021

Background –TP0-TP2 or TP3-TP5 Host

Test points	Description
TP0 to TP5	The 100GBASE-CR4 channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 92–2. The cable assembly test fixture of Figure 92–17 or its equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4.
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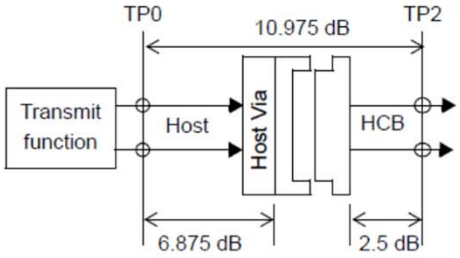
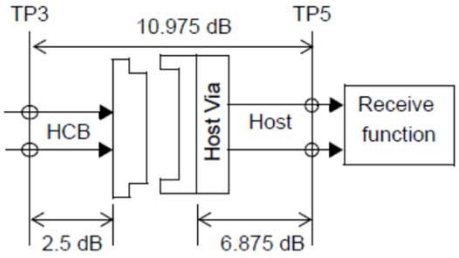
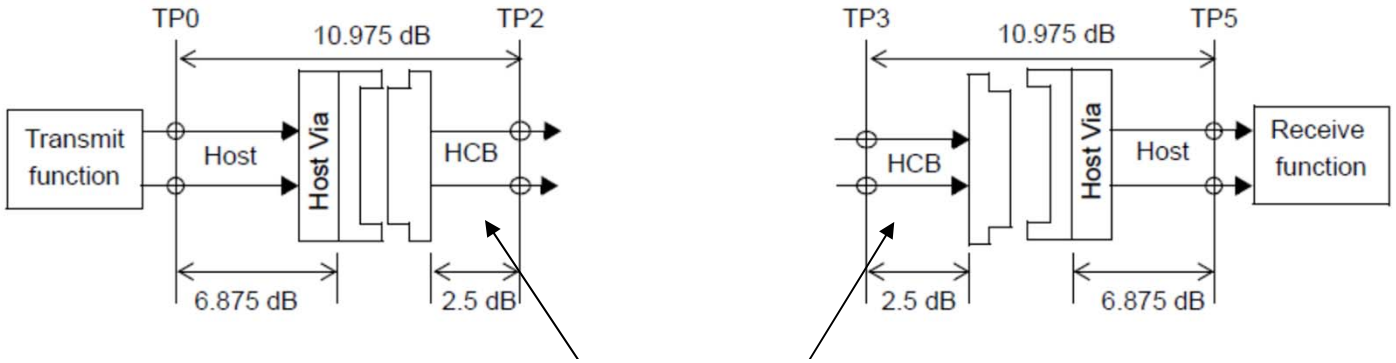




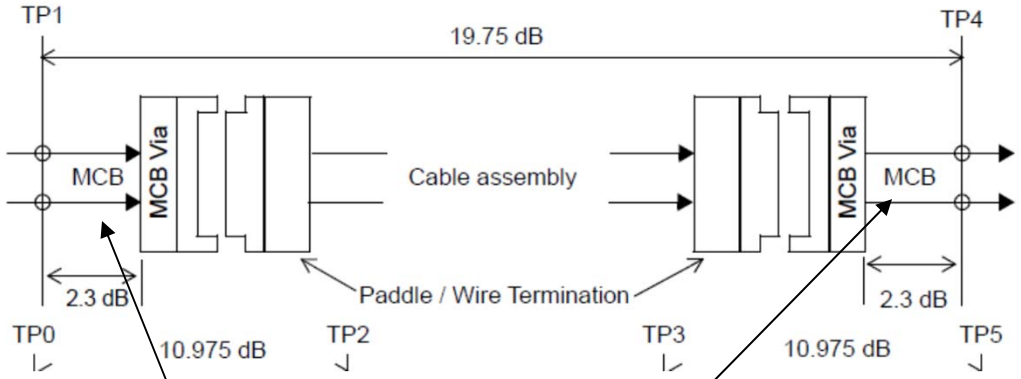
Host insertion loss at 26.56 GHz

Source: IEEE P802.3ck™/D2.0, 10th March 2021

Background –Test Fixtures



Host Compliance Board (TP2 or TP3) - Plug in at TP2 or TP3 for TX and RX measurements – PCB IL minimizes



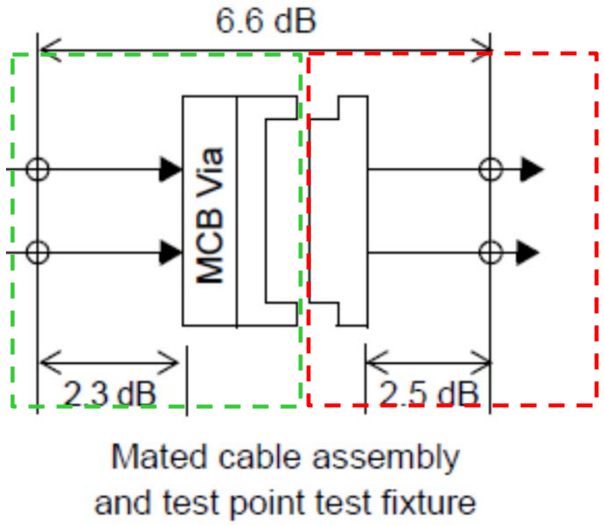
Module Compliance Board or Cable Assembly Test – PCB IL to emulate minimum host IL

Source: IEEE P802.3ck™/D2.0, 10th March 2021

Background –Test Fixtures

- **Specified in a mated state**

Module Compliance or Cable Assembly Test Fixture



Host Compliance Board (TP2 or TP3

NOTE—2.3 dB MCB PCB IL includes the RF connector (up to the RF connector reference plane).

Mated Test Fixture Parameter description
Maximum insertion loss
Minimum insertion loss
Effective Return Loss (ERL)
Common-mode conversion insertion loss
Common-mode return loss
Common-mode to differential – mode return loss
Integrated Crosstalk Noise (ICN)

Test Fixture insertion loss at 26.56 GHz

Source: IEEE P802.3ck™/D2.0, 10th March 2021

TX and RX PCB Loss

IEEE 802.3bj/by/cd

Host Tx and Rx PCB losses

- Transmitter and receiver differential printed circuit board trace loss

GHz	dB/in
1	0.1856
6.5	0.8971
7	0.9557
12.89	1.5924
14	1.702

Attenuation* (dB/in) at:	1 GHz	6.5 GHz	7 GHz	12.89 GHz	14 GHz
Meg6_LowSR – Wide	0.0951	0.4159	0.4433	0.7562	0.8127
Meg6_LowSR – Narrow	0.1466	0.5849	0.6205	1.0152	1.0847
Meg6_HighSR – Wide	0.1175	0.5960	0.6367	1.0891	1.1688
Meg6_HighSR – Narrow	0.1856	0.8971	0.9557	1.5924	1.7020
ImpFR4_LowSR – Wide	0.1202	0.6096	0.6541	1.1772	1.2734
ImpFR4_LowSR – Narrow	0.1717	0.7794	0.8323	1.4410	1.5512
ImpFR4_HighSR – Wide	0.1427	0.7904	0.8484	1.5158	1.6367
ImpFR4_HighSR – Narrow	0.2106	1.0930	1.1692	2.0283	2.1813

PROPOSED PARAMETERS; GRAPHS ON PREVIOUS SLIDE

*using Algebraic Model v2.02a – see backup slides for values entered in Model

Proposal for Defining Material Loss
26-Jan 12

Elizabeth Kochuparambil
Joel Goergen

Cisco

http://www.ieee802.org/3/bj/public/jan12/kochuparambil_01a_0112.pdf

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802.3bj Cu specifications

http://www.ieee802.org/3/bj/public/may12/diminico_01a_0512.pdf

PHY	MBd	Bandwidth (MHz)	PCBILdb/76.2mm	PCBILdb/in
25GBASE-T1	14062.25	7031.25	1.8717	0.624

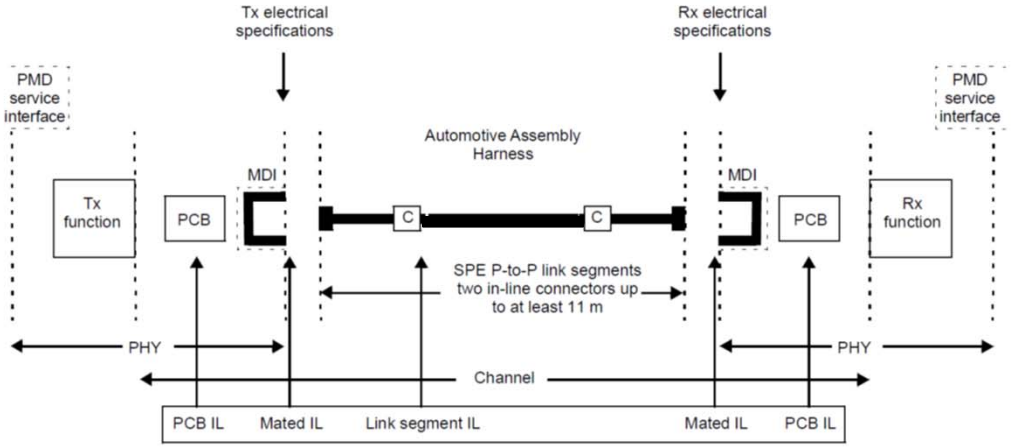
Dk Df Algebraic Model

Background

- Model first shown in Kochuparambil_01_1111
  - Filling a gap – allows us to talk the same "language"
  - Great for initial channel loss discussions!
- Model is made public: http://www.ieee802.org/3/bj/public/tools.html
- No secret sauce
  - All equations used in the model are given in reference document
  - Also in public Tools folder; link above

Tx Function to Rx function channel IL

- **Tx Function to Rx function channel IL proposal**



$$IL_{Channel} \leq 2 \cdot IL_{PCB(76.2mm)} + 2 \cdot IL_{MDI} + IL_{Linksegment} \quad (dB)$$

$$IL_{PCB(76.2mm)} \leq \left(0.0071 \cdot \sqrt{f/2.5 \cdot 10\text{^}3} + 0.0045 \cdot f/2.5 \cdot 10\text{^}3\right) \cdot 76.2 \ (dB)$$

$$IL_{Linksegment} \leq 0.002\left(\frac{f}{2.5}\right) + 0.68\left(\frac{f}{2.5}\right)^{0.45} \quad (dB)$$

$$IL_{MDI} \leq 0.1\sqrt{\frac{f}{2.5 \cdot 10\text{^}3}} \quad (dB)$$

https://www.ieee802.org/3/cy/public/adhoc/diminico_3cy_01a_1_5_21.pdf

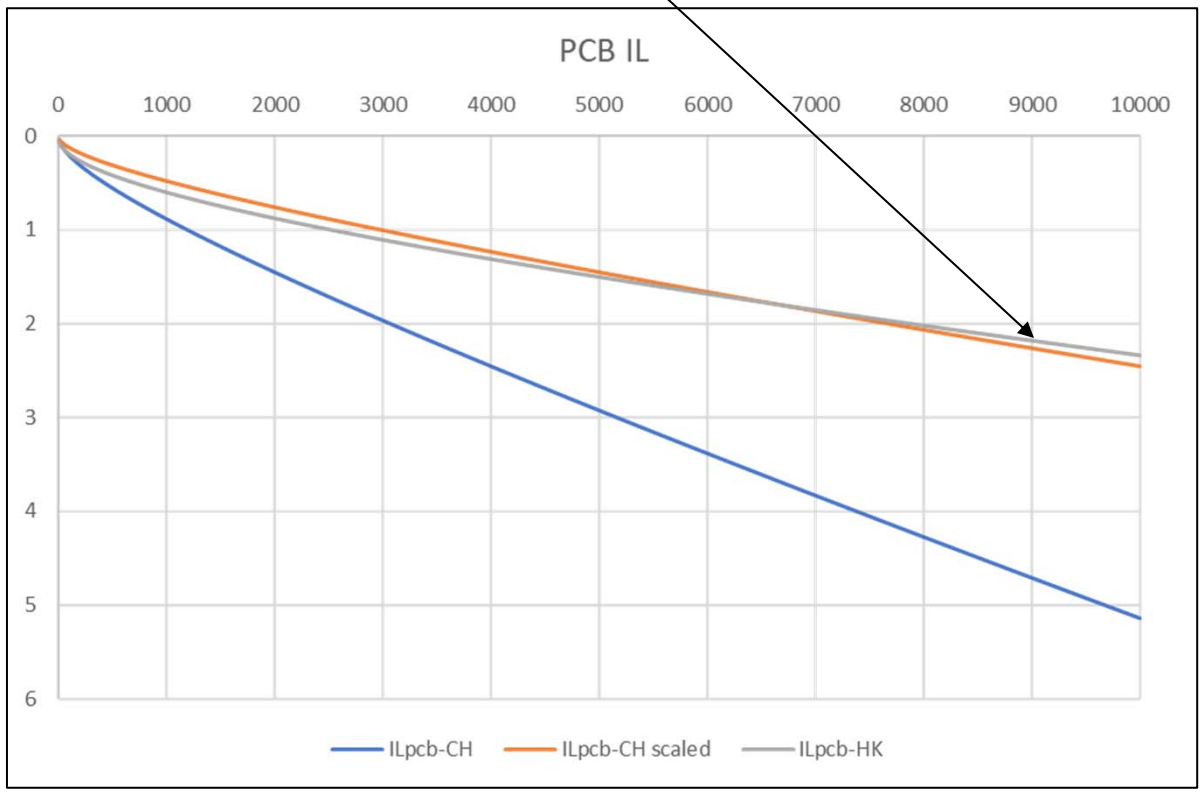
PHY	MBd	Bandwidth (MHz)	PCBILdb/76.2mm	IL Link Segment	IL MDI	IL Channel Max
25GBASE-T1	14062.25	7031.25	1.8717	29.8688	0.168	33.948

PCB – 76.2 mm/3 inch

- *The PCB budget is determined based on the material comparison analysis done in Kadry_3cy_01a_03_01_21.*
- *The PCB loss budget profile was based on the loss of the high-density stack of material with Er=3.4 and Df=0.008*

$$IL_{PCB}\left(dB/_{in}\right) = 0.17(f_{GHz})^{0.45} + 0.03(f_{GHz})$$

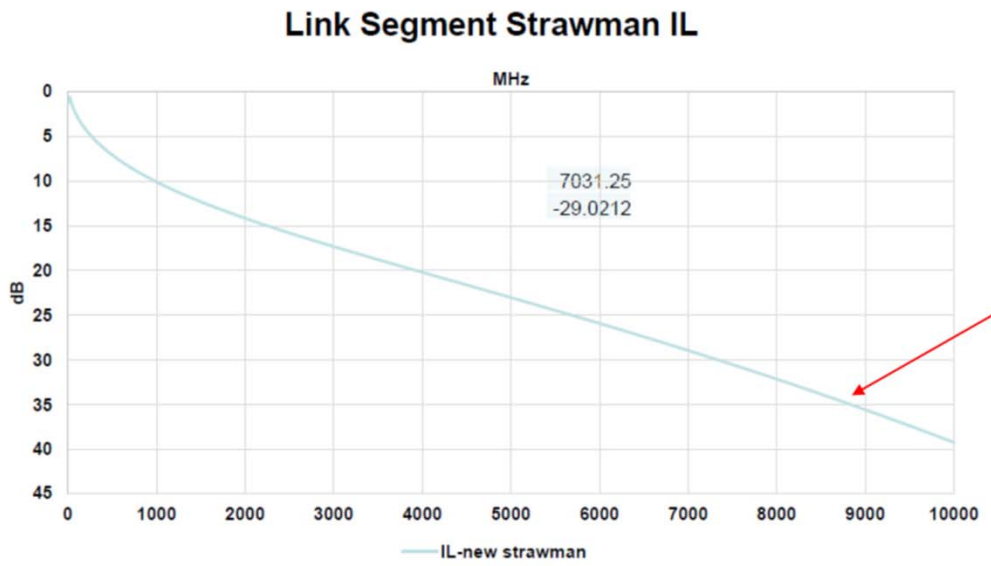
$$IL_{PCB}\left(dB/_{mm}\right) = 0.0067\left(\frac{f_{MHz}}{1000}\right)^{0.45} + 0.0012\left(\frac{f_{MHz}}{1000}\right)$$



Link Segment Strawman IL

The link segment IL strawman was proposed in the following contribution DiBiaso_et_all_3cy_adhoc_01a_04_20_21. This contribution outlines the history and references all previous contribution that led to this proposal.

Link Segment Strawman IL



Additional Relaxation of IL Limit above 7GHz

*Link Segment IL= -1.2+0.41*SQRT(f_{MHz})-0.00185* f_{MHz} +1.79E-07* f_{MHz} ^2*

*Link Segment IL= -1.2+0.41*SQRT(7031.25)-0.00185* 7031.25+1.79E-07* 7031.25 ^2= ~29 dB*

Fmin = 10MHz

Fmax = 9/10GHz

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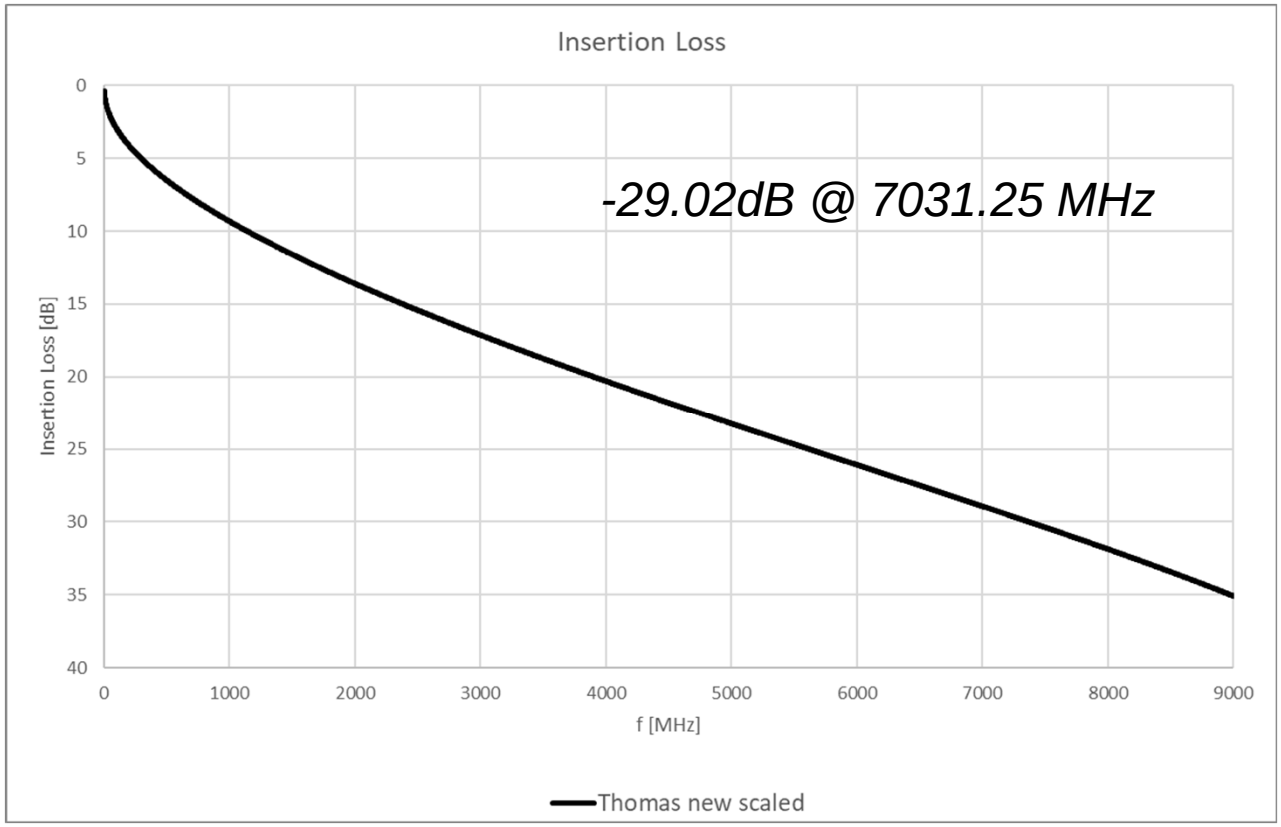
Updated Link Segment Strawman IL

An adjustment to the Link Segment IL proposal was put fourth by Thomas Muller in mueller_3cy_01_05_18_21.pdf

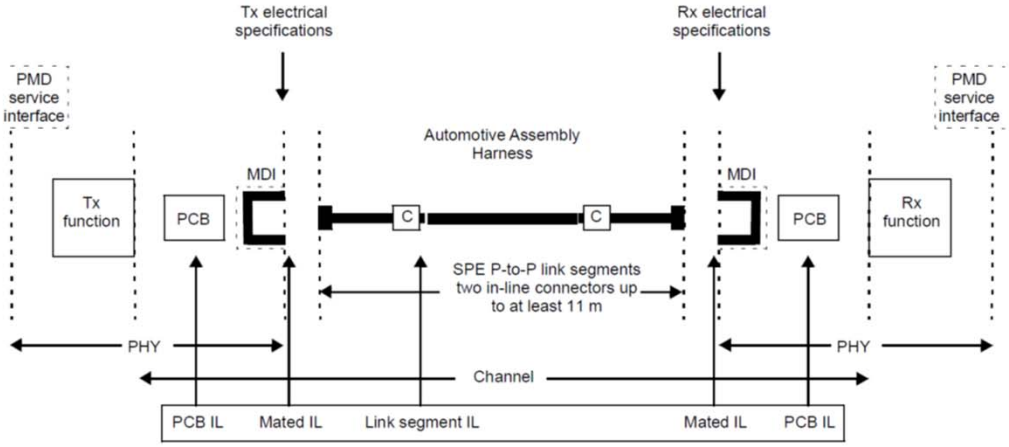
$$IL_{LinkSegment}(dB) \leq 0.00135(f_{MHz}) + 0.3564(f_{MHz})^{0.45} + 0.495\left(\frac{f_{MHz}}{7500}\right)^{6}$$

$$where\ f\ is\ the\ frequency\ in\ MHz;\ 10 \leq f \leq 9000$$



Tx Function to Rx function channel IL

- **Tx Function to Rx function channel IL proposal**



$$IL_{Channel}\,(dB) \le 2 \cdot IL_{PCB} + 2 \cdot IL_{MDI} + IL_{Linksegment}$$

$$IL_{PCB}(dB) \le 0.09144\left(\frac{f_{MHz}}{1000}\right) + 0.51054\left(\frac{f_{MHz}}{1000}\right)^{0.45}$$

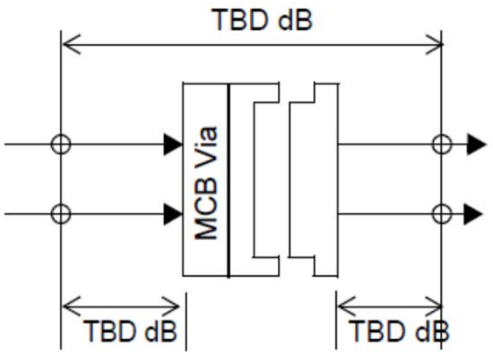
$$IL_{LinkSegment}(dB) \le 0.00135(f_{MHz}) + 0.3564(f_{MHz})^{0.45} + 0.495\left(\frac{f_{MHz}}{7500}\right)^{6}$$

$$IL_{MDI}(dB) \le 0.1\sqrt{\frac{f_{MHz}}{2500}}$$

PHY	MBd	Bandwidth (MHz)	IL PCB	IL Link Segment	IL MDI	IL Channel
25GBASE-T1	14062.25	7031.25	1.871	29.02	0.168	33.098

Test Fixture - 802.3cy- Future Work

- Use 802.3cy Channel IL method to formulate 802.3cy test fixture IL
- Specified in a mated state



Mated cable assembly
and test point test fixture

Mated Test Fixture Parameter description
Maximum insertion loss
Minimum insertion loss
Return Loss
Common-mode conversion insertion loss
Common-mode return loss
Common-mode to differential – mode return loss
Alien Crosstalk