802.3cy
Test Fixture Considerations

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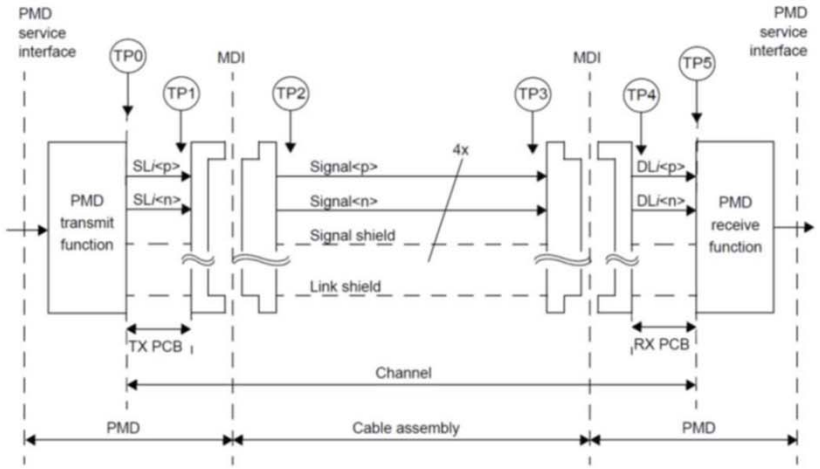
Purpose

- Test Points
- Test Fixture Considerations
  - Use 802.3cy Channel PCB IL and connector IL assumptions to formulate 802.3cy test fixture IL
  - Test fixtures specified in a mated state

Background –Test Points

Background – 802.3bj/by/cd/ck

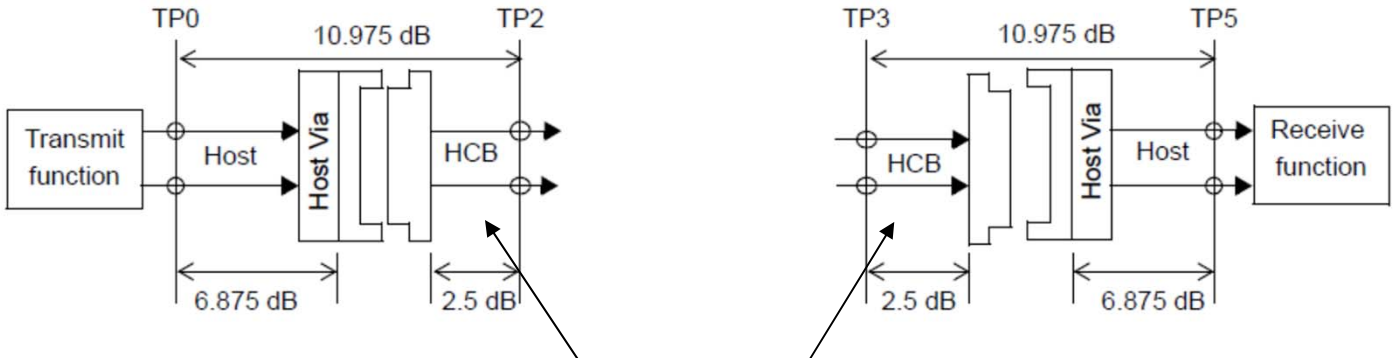
- The channel is defined between the transmitter and receiver blocks to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly (link segment).
- Test points provide specification references for channel and cable assembly and RX and TX
- Test fixtures enable testing at test points – module compliance board (MCB); host compliance board (HCB)



Test points	Description
TP0 to TP5	The 100GBASE-CR4 channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 92–2. The cable assembly test fixture of Figure 92–17 or its equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 92.8.3 and 92.8.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 92.8.3.6.
TP2	Unless specified otherwise, all transmitter measurements defined in Table 92–6 are made at TP2 utilizing the test fixture specified in 92.11.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 92.8.4 are made at TP3 utilizing the test fixture specified in 92.11.1.

https://www.ieee802.org/3/cy/public/adhoc/diminico_3cy_01a_04_27_21.pdf

Background –Test Fixtures- Host Compliance Board



Host Compliance Board (TP2 or TP3) - Plug in at TP2 or TP3 for TX and RX measurements – PCB IL minimized

Table 162–10—Summary of transmitter specifications at TP2

Parameter	Subclause reference	Value	Units
Signaling rate, each (nominal)		53.125 ± 50 ppm[a]	GBd
Differential pk-pk voltage with Tx disabled (max)[b]	93.8.1.3	30	mV
DC common-mode voltage (max)[b]	93.8.1.3	1.9	V
AC common-mode RMS voltage, v_{cmd} (max)[b]	93.8.1.3	30	mV
Differential pk-pk voltage, v_{df} (max)[b]	93.8.1.3	1200	mV
Effective return loss, ERL (min)	162.9.3.5	7.3	dB
Common-mode to common-mode return loss (min)	162.9.3.6	2	dB
Common-mode to differential return loss (min)	162.9.3.7	See Equation (162–5)	dB
Transmitter steady-state voltage, v_f (min) Transmitter steady-state voltage, v_f (max)	162.9.3.1.2	0.387 0.6	V
Linear fit pulse peak ratio (min)	162.9.3.1.2	0.397	—
Level separation mismatch ratio R_{LM} (min)	120D.3.1.2	0.95	—
Transmitter output waveform[c] absolute value of step size for all taps (min) absolute value of step size for all taps (max) value at minimum state for $c(-3)$ (max) value at maximum state for $c(-2)$ (min) value at minimum state for $c(-1)$ (max) value at minimum state for $c(0)$ (max) value at minimum state for $c(1)$ (max)	 162.9.3.1.4 162.9.3.1.4 162.9.3.1.5 162.9.3.1.5 162.9.3.1.5 162.9.3.1.5 162.9.3.1.5	 0.005 0.025 −0.06 0.12 −0.34 0.5 −0.2	 — — — — — — —
Signal-to-noise-and-distortion ratio, SNDR (min)[d]	162.9.3.3	31.5	dB
Output jitter (max) J_{RMS} J3u Even-odd jitter, pk-pk	 162.9.3.4 162.9.3.4 162.9.3.4	 0.023 0.115 0.025	 UI UI UI

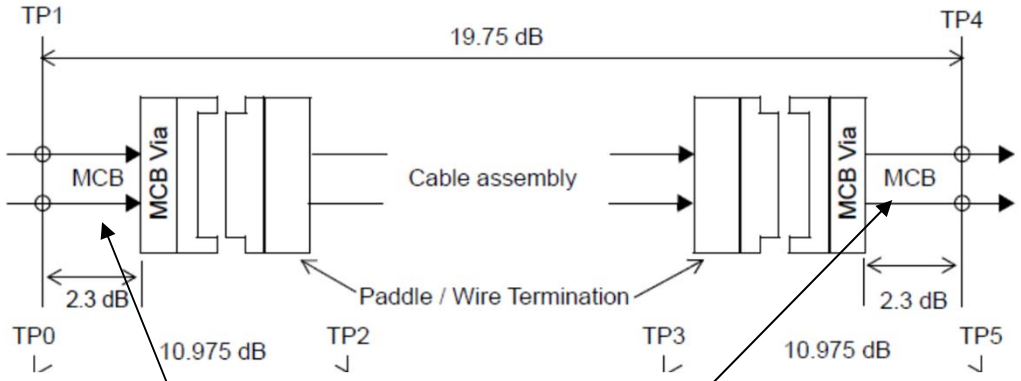
Table 162–14—Summary of receiver specifications at TP3

Parameter	Subclause reference	Value	Units
Signaling rate	162.9.4.1	53.125 ± 100 ppm	GBd
Amplitude tolerance	162.9.4.2	1200[a]	mV
Interference tolerance	162.9.4.3	Table 162–15	—
Jitter tolerance	162.9.4.4	Table 162–16	—
Effective return loss, ERL (min)	162.9.4.5	7.3	dB
Differential to common-mode return loss (min)	162.9.4.6	Equation (162–16)	dB

[a]Amplitude is measured at TP2.

Source: IEEE P802.3ck™/D2.0, 10th March 2021

Background –Test Fixtures - Module Compliance Board



Module Compliance Board or Cable Assembly Test – PCB IL to emulate minimum host IL

Table 162–17—Cable assembly characteristics summary

Description	Reference	Value	Unit
Maximum insertion loss at 26.56 GHz	162.11.2	19.75	dB
Minimum insertion loss at 26.56 GHz	162.11.2	11	dB
Minimum cable assembly ERL[a]	162.11.3	8.25	dB
Differential to common-mode return loss	162.11.4	Equation (162–18)	dB
Differential to common-mode conversion loss	162.11.5	Equation (162–19)	dB
Common-mode to common-mode return loss	162.11.6	Equation (162–20)	dB
Minimum COM	162.11.7	3	dB

[a]Cable assemblies with a COM greater than 4 dB are not required to meet minimum ERL.

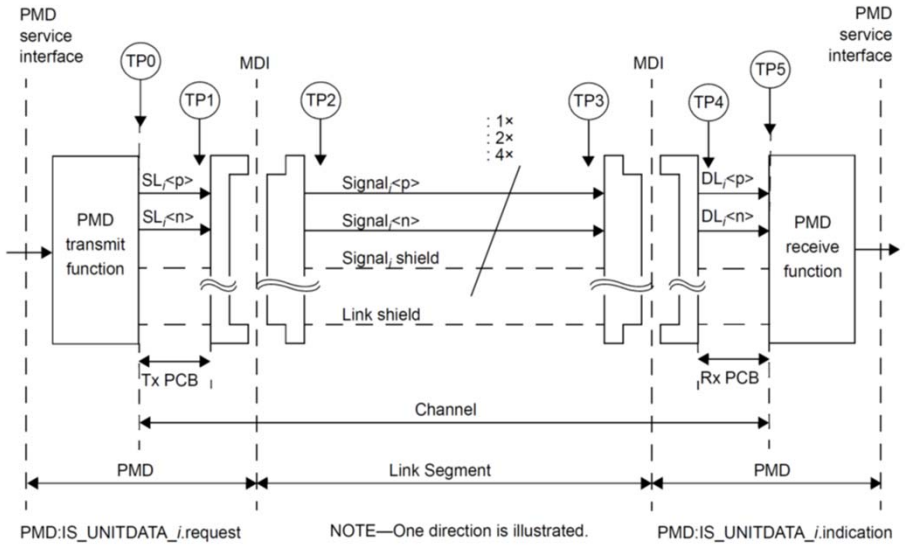
Source: IEEE P802.3ck™/D2.0, 10th March 2021

802.3cy Test Point Definitions

Test Points

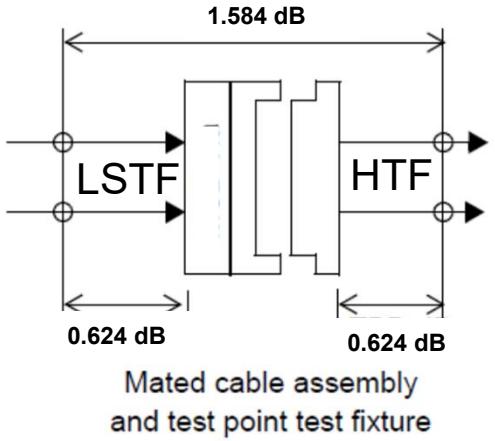
Test points	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance PCB differential-mode to differential-mode insertion loss and the cable assembly differential-mode to differential-mode insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in xxx. The cable assembly test fixture of xxx, or its equivalent, is required for measuring the cable assembly specifications in xxx at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in xxx and xxx. The recommended maximum differential-mode to differential-mode insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in xxx.
TP2	Unless specified otherwise, all transmitter measurements defined in xxx are made at TP2 utilizing the test fixture specified in xxx.
TP3	Unless specified otherwise, all receiver measurements and tests defined in xxx are made at TP3 utilizing the test fixture specified in xxx.

Test Point Figure



802.3cy Mated Test Fixture – IL

- Test fixture specified in a mated state
- Use 802.3cy Channel PCB IL and connector IL to formulate 802.3cy test fixture IL
- Use mated test fixture measurements/models to develop test fixture parameter limits



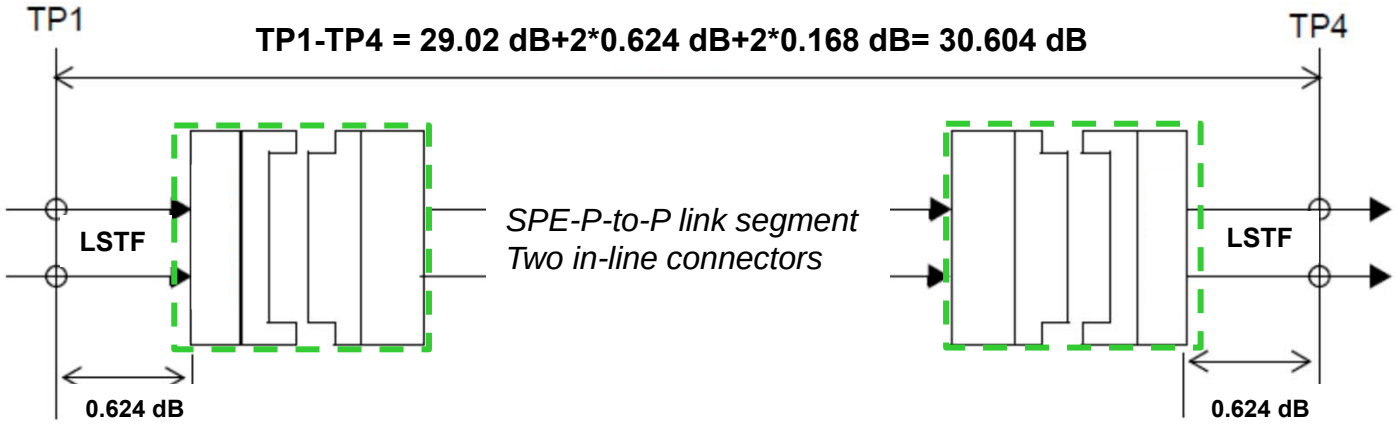
Link Segment Test Fixture (LSTF)
Host Test Fixture (HTF)

PCB IL @ 7031.25 MHz for 25.4 mm (1 in) = 0.624 dB
PCB IL @ 7031.25 MHz for 76.2 mm (3 in) = 1.871 dB
MDI IL @ 7031.25 MHz = 0.168 dB
Plug IL @ 7031.25 MHz = 0.168 dB
*Mated Test Fixture @ 7031.25 MHz = 2*0.624 dB+2*0.168 dB = 1.584 dB*

Mated Test Fixture Parameter description
Maximum insertion loss – 1.584 dB @ 7031.25 MHz
Minimum insertion loss
Return Loss
Common-mode conversion insertion loss
Common-mode return loss
Common-mode to differential – mode return loss
Crosstalk

802.3cy–TP1-TP4 Link Segment IL- Normative

TP1 toTP4	Test points for all link segment measurements. The link segment test fixture, or its equivalent, is required for measuring the link segment specifications in xxx.xx at TP1 and TP4.



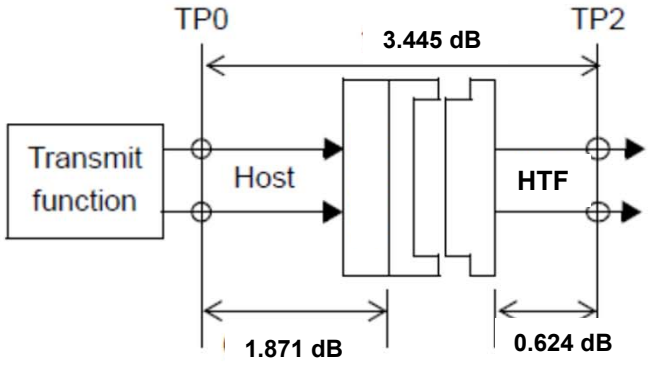
Link segment insertion loss at 7031.25 MHz

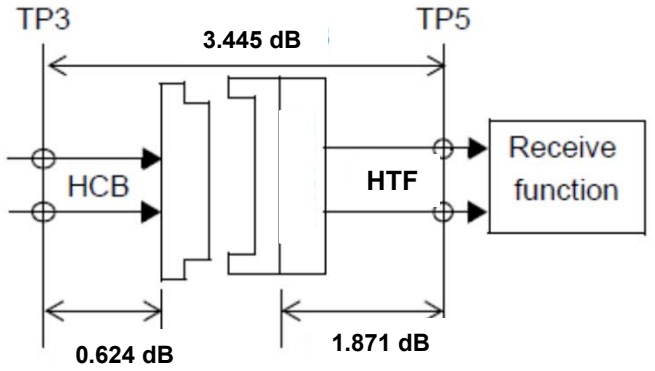
$$IL_{TP1-TP4}\,(dB) \leq 2 \cdot IL_{HSTFPCB\_25.4\,mm} + 2 \cdot IL_{connector} + IL_{Linksegment}$$

Normative = requirements

802.3cy –TP0-TP2 or TP3-TP5 Host IL- Informative

TP0 to TP2 TP3 to TP5	A mated connector pair is included in both the transmitter and receiver specifications. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is specified.
TP2	Unless specified otherwise, all transmitter measurements are made at TP2 utilizing the specified test fixture.
TP3	Unless specified otherwise, all receiver measurements and tests are made at TP3 utilizing the specified test fixture.





TP0-TP2=1.871 dB+0.624 dB +0.624 dB +0.168 dB +0.168 dB = 3.445 dB

TP0-TP2=1.871 dB+0.624 dB +0.624 dB +0.168 dB = 3.445 dB

$$IL_{TP0-TP2\ or\ TP3-TP5}(dB) \leq IL_{HOSTPCB\_76.2mm} + IL_{PCBHTF} + IL_{MDI} + IL_{Plug}$$

Informative = information not requirements

Straw Poll

I support adoption of test point definitions and test fixture specifications slide 6-9 above.

Y:
N:
A:

Summary

- **Test Point and Test Fixture Considerations**

- **Motion Preview**

Move to adopt test point definitions and test fixture specifications slide 6-9 diminico_et_al_3cy_01a_9_7_21.pdf with editorial license.

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Y:
N:
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