802.3cy
Test Fixture Considerations

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Purpose

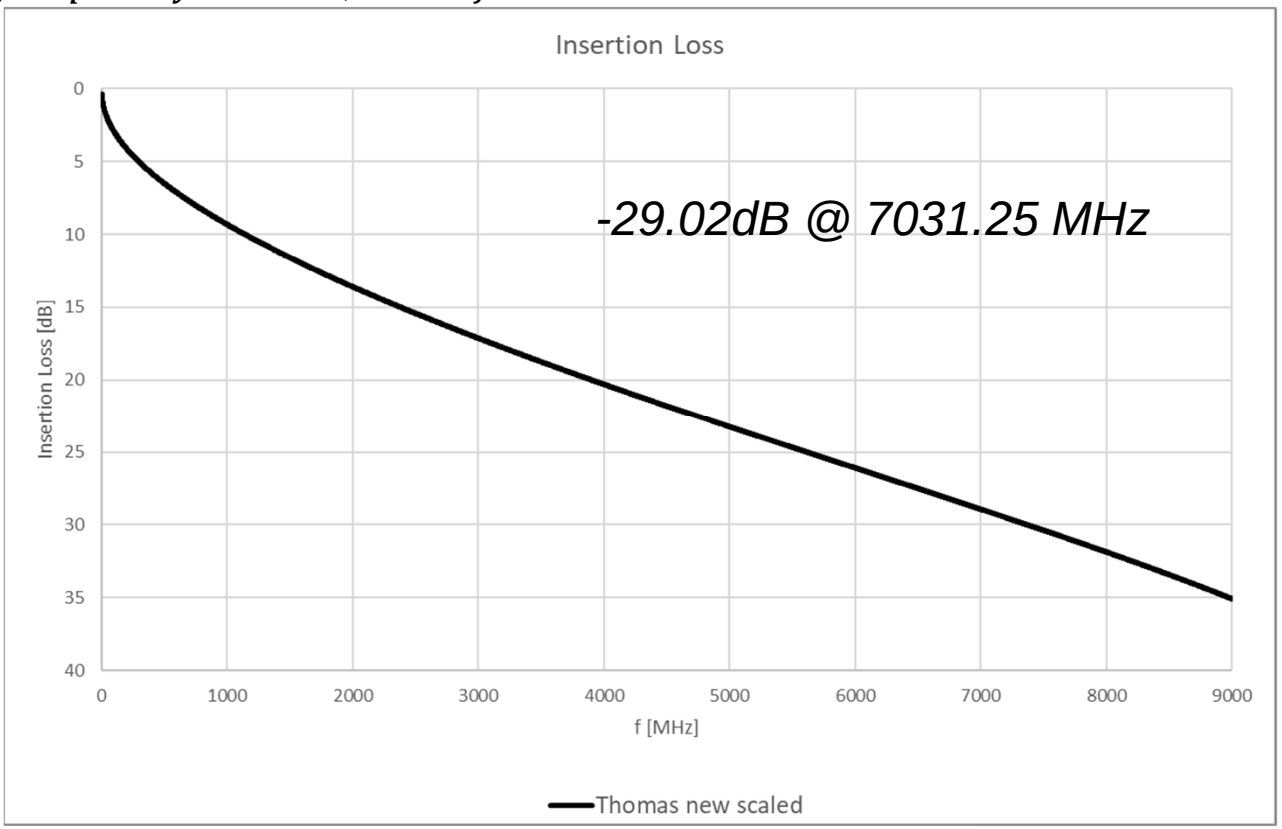
- **Test Fixture Considerations**
  - **Use 802.3cy Channel PCB IL and connector IL assumptions to formulate 802.3cy test fixture IL**
  - **Test fixtures specified in a mated state**

Link Segment Strawman IL

An adjustment to the Link Segment IL proposal was put fourth by Thomas Muller in mueller_3cy_01_05_18_21.pdf

$$IL_{LinkSegment}(dB) \leq 0.00135(f_{MHz}) + 0.3564(f_{MHz})^{0.45} + 0.495\left(\frac{f_{MHz}}{7500}\right)^{6}$$

$$where\ f\ is\ the\ frequency\ in\ MHz;\ 10 \leq f \leq 9000$$



Source: diminico_et_all_3cy_01a_05_18_21.pdf

Link Segment Strawman IL Margin Discussion

Source: DiBiasoCuesta_3cy_01_06_01_21.pdf – slide 6

Conclusion

- Less than 1.6dB margin to the limit line when entire cable is at 105°C across entire frequency range.
- This margin can increase when only 5 meters of cable is exposed to 105°C.
- This margin can decrease when cable is exposed to heat aging .
- This analysis demonstrates the proposed link segment insertion loss limit seems appropriate and will have minimal margin when an 11 meter 24AWG solid conductor cable is exposed to the automotive environment.

Source: koeppendoerfer_3cy_01_06_01_21.pdf – slide 6

Conclusion

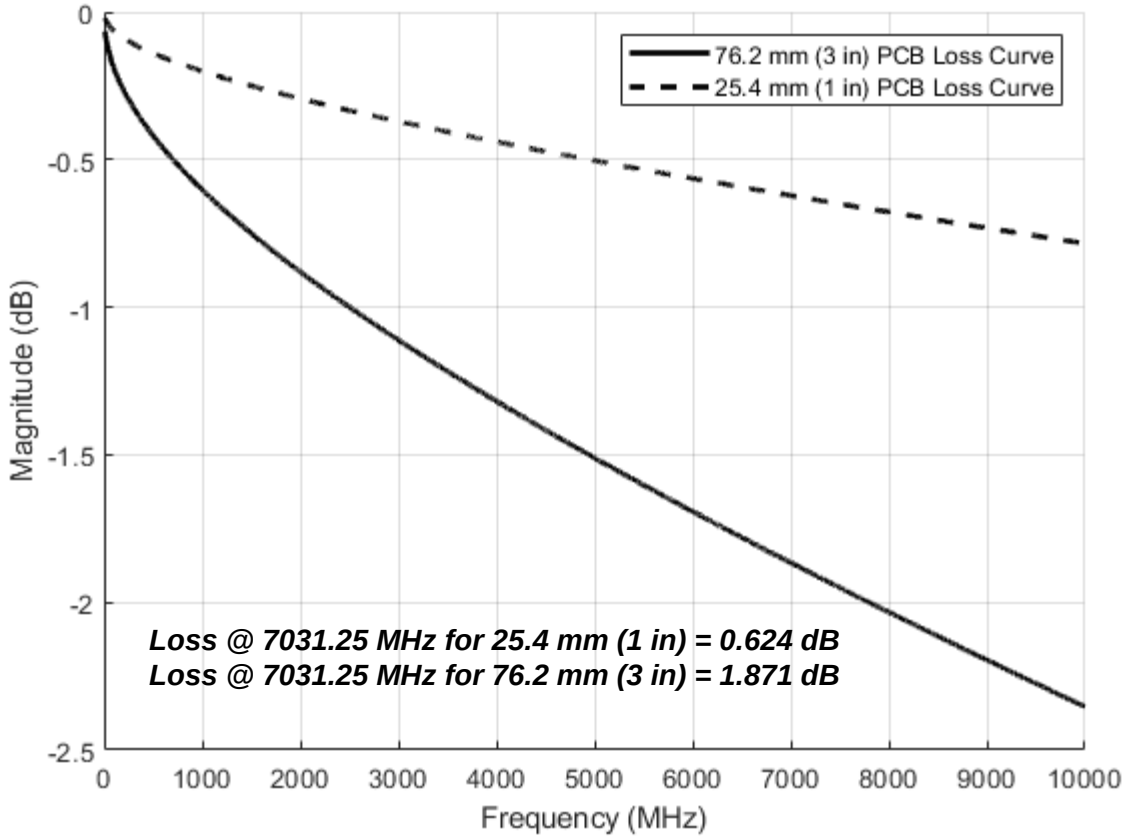
› Based on measurement data (against limit proposal mueller_3cy_01_05_18_21) 9m with an AWG 26 cable is possible

› Based on estimated simulation data (against limit proposal mueller_3cy_01_05_18_21) 11m with AWG 24 is possible

PCB Loss

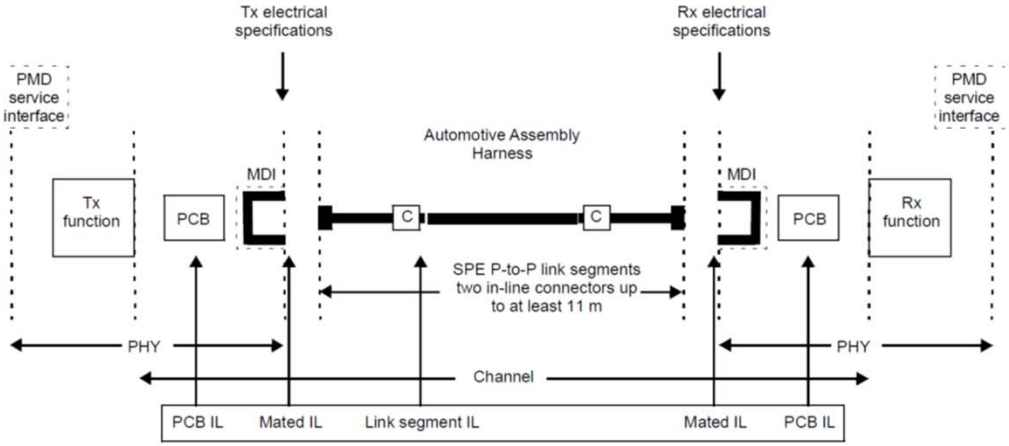
- *The PCB budget is determined based on the material comparison analysis done in Kadry_3cy_01a_03_01_21.*
- *The PCB loss budget profile was based on the loss of the high-density stack of material with Er=3.4 and Df=0.008*

$$IL_{PCB}\left(dB/_{mm}\right) = 0.0067\left(\frac{f_{MHz}}{1000}\right)^{0.45} + 0.0012\left(\frac{f_{MHz}}{1000}\right) \qquad IL_{PCB}\left(dB/_{in}\right) = 0.17(f_{GHz})^{0.45} + 0.03(f_{GHz})$$



Tx Function to Rx function channel IL

- **Tx Function to Rx function channel IL proposal**



$$IL_{Channel}\,(dB) \le 2 \cdot IL_{PCB} + 2 \cdot IL_{MDI} + IL_{Linksegment}$$

$$IL_{PCB}(dB) \le 0.09144\left(\frac{f_{MHz}}{1000}\right) + 0.51054\left(\frac{f_{MHz}}{1000}\right)^{0.45}$$

$$IL_{LinkSegment}(dB) \le 0.00135(f_{MHz}) + 0.3564(f_{MHz})^{0.45} + 0.495\left(\frac{f_{MHz}}{7500}\right)^{6}$$

$$IL_{MDI}(dB) \le 0.1\sqrt{\frac{f_{MHz}}{2500}}$$

PHY	MBd	Bandwidth (MHz)	IL PCB	IL Link Segment	IL MDI	IL Channel
25GBASE-T1	14062.25	7031.25	1.871	29.02	0.168	33.098

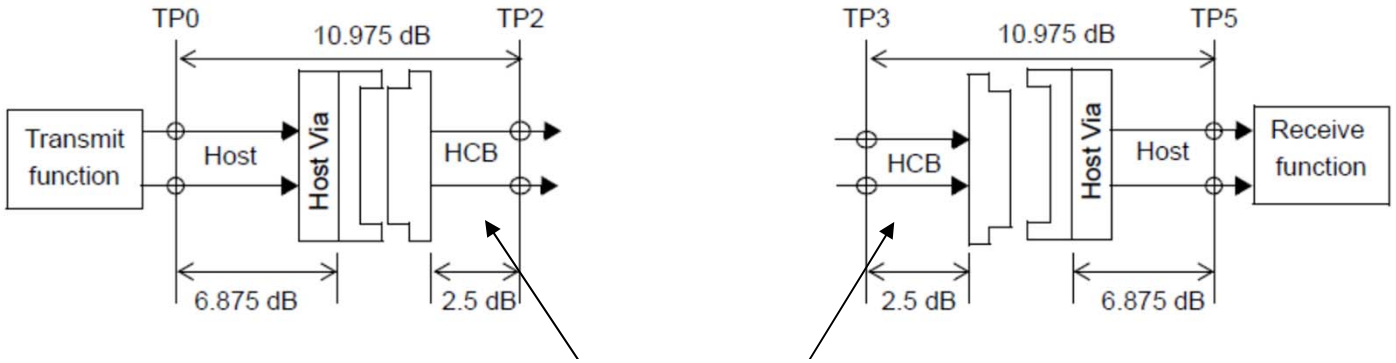
Source: diminico_et_all_3cy_01a_05_18_21.pdf

Background –Test Points

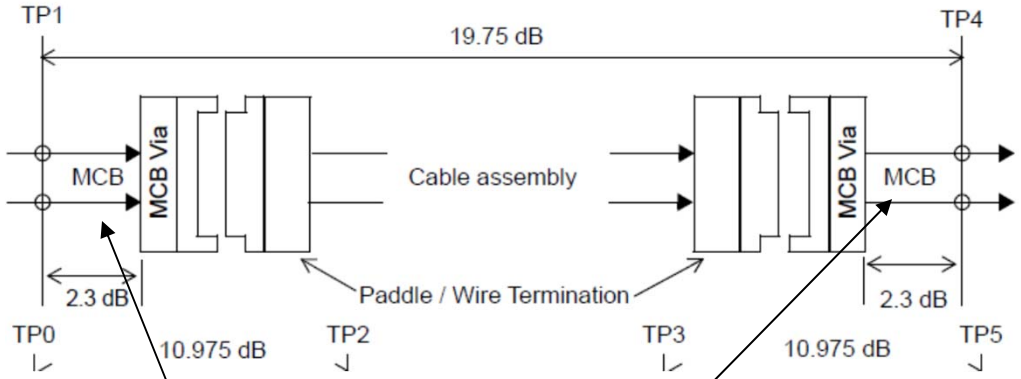
Test points	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance PCB insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure 162–2. The cable assembly test fixture of Annex 162B, or its equivalent, is required for measuring the cable assembly specifications in 162.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 162.9.3 and 162.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 162.9.3.2.
TP2	Unless specified otherwise, all transmitter measurements defined in 162.9.3 are made at TP2 utilizing the test fixture specified in Annex 162B.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 162.9.4 are made at TP3 utilizing the test fixture specified in Annex 162B.

Source: IEEE P802.3ck™/D2.0, 10th March 2021

Background – 802.3ck IL Test Fixtures



Host Compliance Board (TP2 or TP3) - Plug in at TP2 or TP3 for TX and RX measurements – PCB IL minimizes

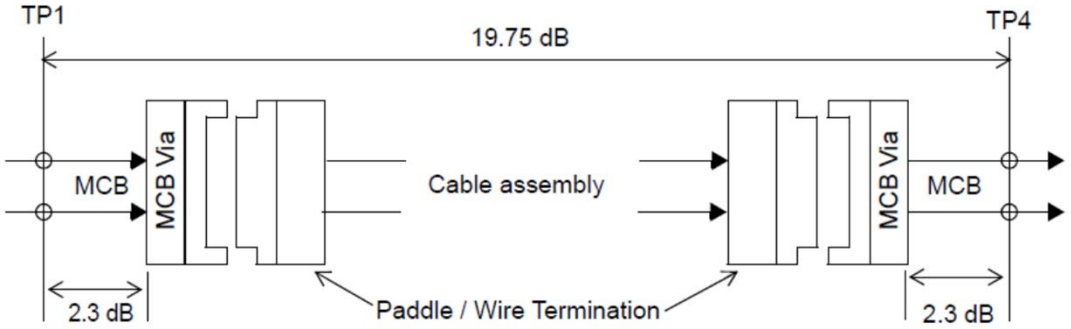


Module Compliance Board or Cable Assembly Test – PCB IL to emulate minimum host IL

Source: IEEE P802.3ck™/D2.0, 10th March 2021

Background –TP1-TP4 Cable Assemblies

Test points	Description
TP0 to TP5	The 100GBASE-CR4 channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 92–2. The cable assembly test fixture of Figure 92–17 or its equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 92.8.3 and 92.8.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 92.8.3.6.
TP2	Unless specified otherwise, all transmitter measurements defined in Table 92–6 are made at TP2 utilizing the test fixture specified in 92.11.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 92.8.4 are made at TP3 utilizing the test fixture specified in 92.11.1.

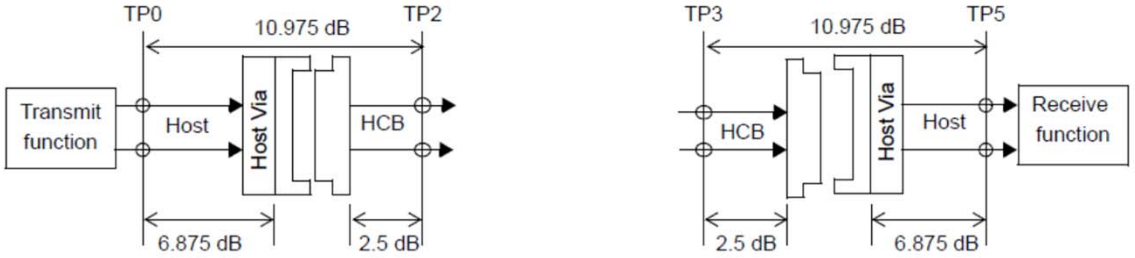


Cable assembly insertion loss at 26.56 GHz

Source: IEEE P802.3ck™/D2.0, 10th March 2021

Background –TP0-TP2 or TP3-TP5 Host

Test points	Description
TP0 to TP5	The 100GBASE-CR4 channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 92–2. The cable assembly test fixture of Figure 92–17 or its equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 92.8.3 and 92.8.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 92.8.3.6.
TP2	Unless specified otherwise, all transmitter measurements defined in Table 92–6 are made at TP2 utilizing the test fixture specified in 92.11.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 92.8.4 are made at TP3 utilizing the test fixture specified in 92.11.1.



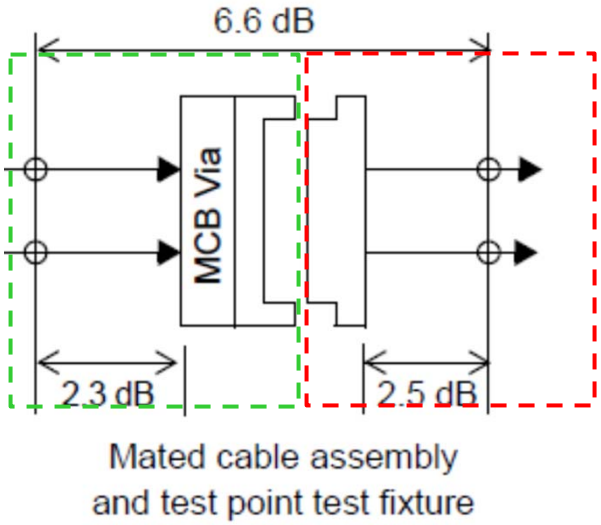
Host insertion loss at 26.56 GHz

Source: IEEE P802.3ck™/D2.0, 10th March 2021

Background –Test Fixtures

- **802.3ck MTF IL specified in a mated state**

Module Compliance or Cable Assembly Test Fixture



Host Compliance Board (TP2 or TP3

NOTE—2.3 dB MCB PCB IL includes the RF connector (up to the RF connector reference plane).

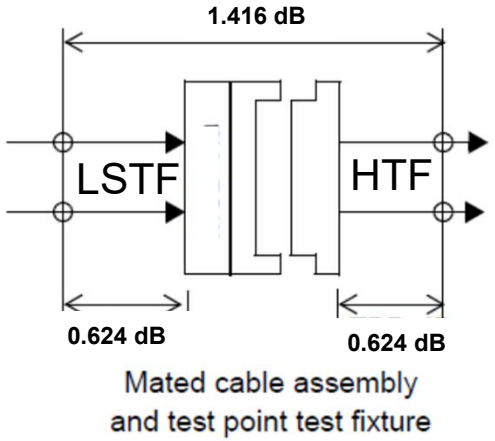
Mated Test Fixture Parameter description
Maximum insertion loss
Minimum insertion loss
Effective Return Loss (ERL)
Common-mode conversion insertion loss
Common-mode return loss
Common-mode to differential – mode return loss
Integrated Crosstalk Noise (ICN)

Test Fixture insertion loss at 26.56 GHz

Source: IEEE P802.3ck™/D2.0, 10th March 2021

802.3cy Mated Test Fixture – IL- Normative

- Test fixture specified in a mated state
- Use 802.3cy Channel PCB IL and connector IL to formulate 802.3cy test fixture IL
- Use mated test fixture measurements/models to develop test fixture parameter limits



Mated cable assembly
and test point test fixture

Link Segment Test Fixture (LSTF)
Host Test Fixture (HTF)

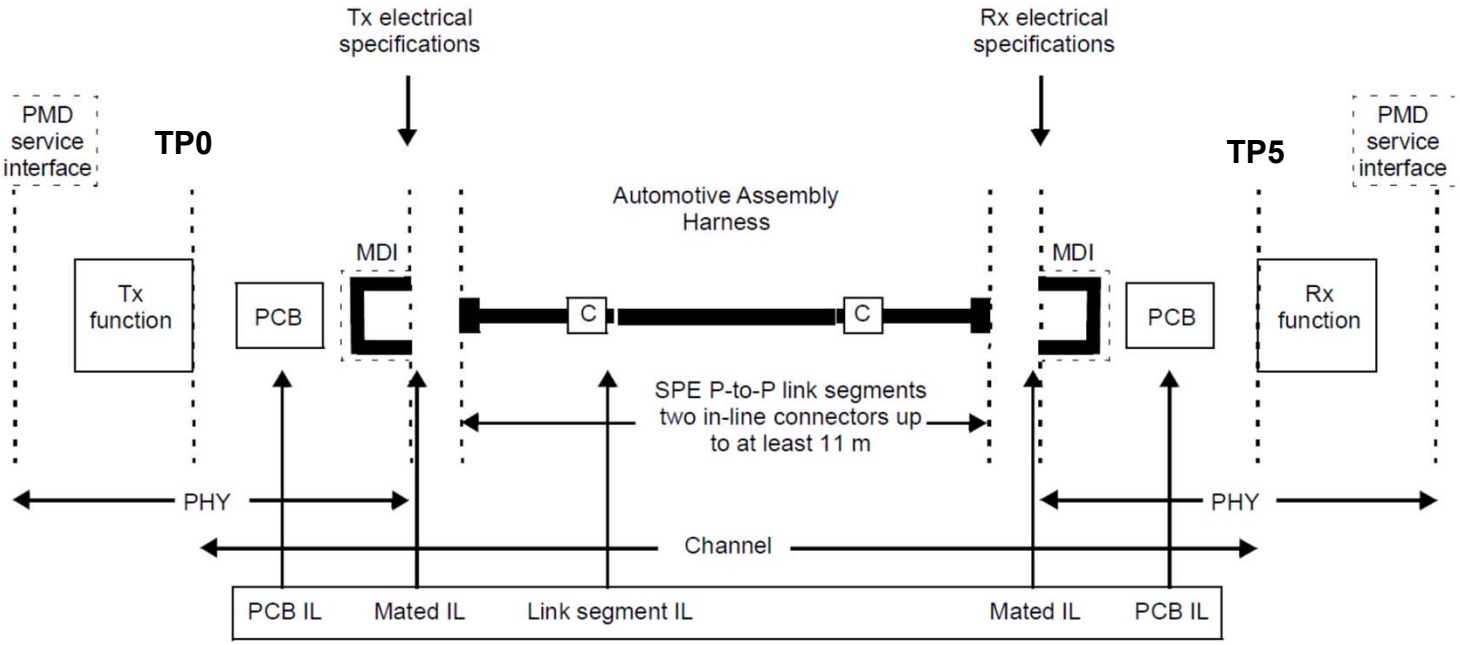
PCB IL @ 7031.25 MHz for 25.4 mm (1 in) = 0.624 dB
PCB IL @ 7031.25 MHz for 76.2 mm (3 in) = 1.871 dB
MDI IL @ 7031.25 MHz = 0.168 dB
Mated Test Fixture @ 7031.25 MHz = 2*0.624 dB+0.168 dB = 1.416 dB

Mated Test Fixture Parameter description
Maximum insertion loss – 1.416 dB @ 7031.25 MHz
Minimum insertion loss
Return Loss
Common-mode conversion insertion loss
Common-mode return loss
Common-mode to differential – mode return loss
Alien Crosstalk

Normative = requirements

802.3cy Test Points – Channel IL- Informative

Test Points	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the link segment insertion loss.



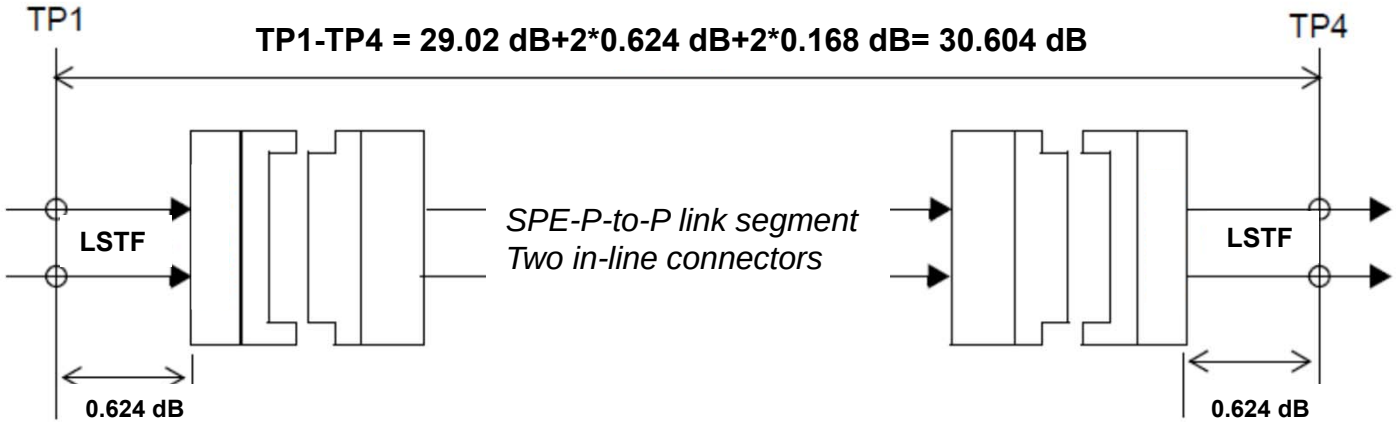
$$IL_{Channel}\,(dB) \leq 2 \cdot IL_{PCB} + 2 \cdot IL_{MDI} + IL_{Linksegment}$$

PHY	MBd	Bandwidth (MHz)	IL PCB	IL Link Segment	IL MDI	IL Channel
25GBASE-T1	14062.25	7031.25	1.871	29.02	0.168	33.098

Informative = information not requirements

802.3cy–TP1-TP4 Link Segment IL- Normative

TP1 toTP4	Test points for all link segment measurements. The link segment test fixture, or its equivalent, is required for measuring the link segment specifications in xxx.xx at TP1 and TP4.



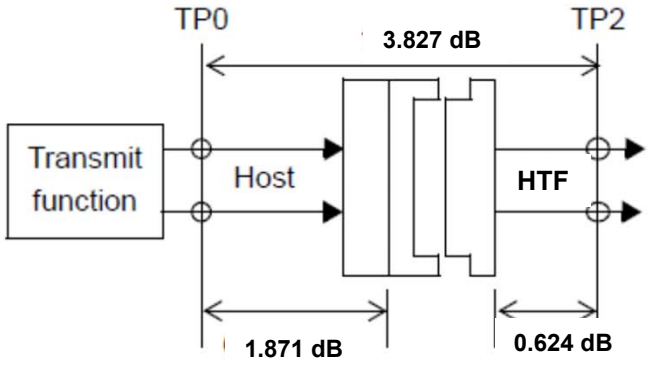
Link segment insertion loss at 7031.25 MHz

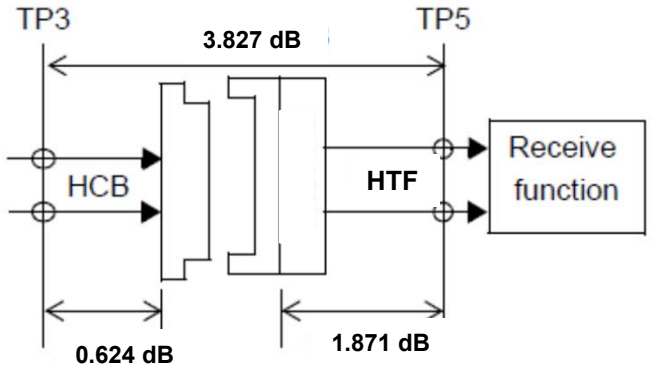
$$IL_{TP1-TP4}\,(dB) \leq 2 \cdot IL_{HSTFPCB\_25.4\,mm} + 2 \cdot IL_{connector} + IL_{Linksegment}$$

Normative = requirements

802.3cy –TP0-TP2 or TP3-TP5 Host IL- Informative

TP0 to TP2 TP3 to TP5	A mated connector pair is included in both the transmitter and receiver specifications. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is specified.
TP2	Unless specified otherwise, all transmitter measurements are made at TP2 utilizing the specified test fixture.
TP3	Unless specified otherwise, all receiver measurements and tests are made at TP3 utilizing the specified test fixture.





TP0-TP2=1.871 dB+0.624 dB +0.624 dB +0.168 dB = 3.287 dB

TP3-TP5=1.871 dB+0.624 dB +0.624 dB +0.168 dB = 3.287 dB

$$IL_{TP0-TP2\ or\ TP3-TP5}(dB) \leq IL_{HSTFPCB\_76.2mm} + IL_{connector} + IL_{HTF}$$

Informative = information not requirements

Summary

- **Test Fixture Considerations**
  - **Use 802.3cy Channel PCB IL and connector IL assumptions to formulate 802.3cy test fixture IL**
  - **Test fixtures specified in a mated state**