On Using PAM4 Modulation

Contribution to IEEE 802.3cy

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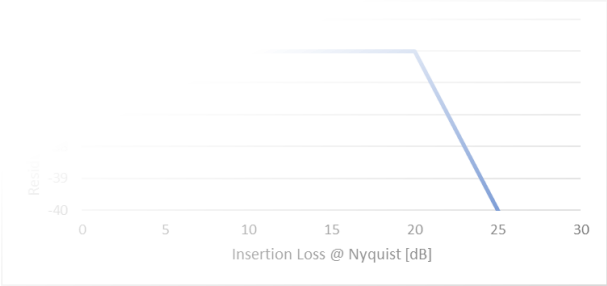
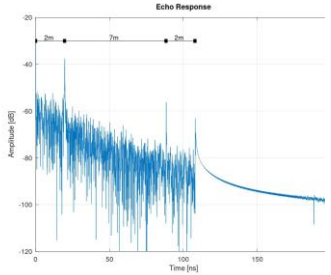
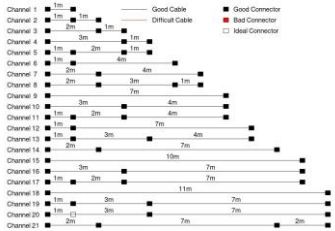
Introduction

- PAM4 modulation is a good candidate for 802.3cy
- PAM4 modulation has good performance across different cables
- PAM4 modulation has more efficient implementation than fractional bits per symbol modulations like PAM5
- We suggests using PAM4 modulation with 802.3ch like precoding for 802.3cy

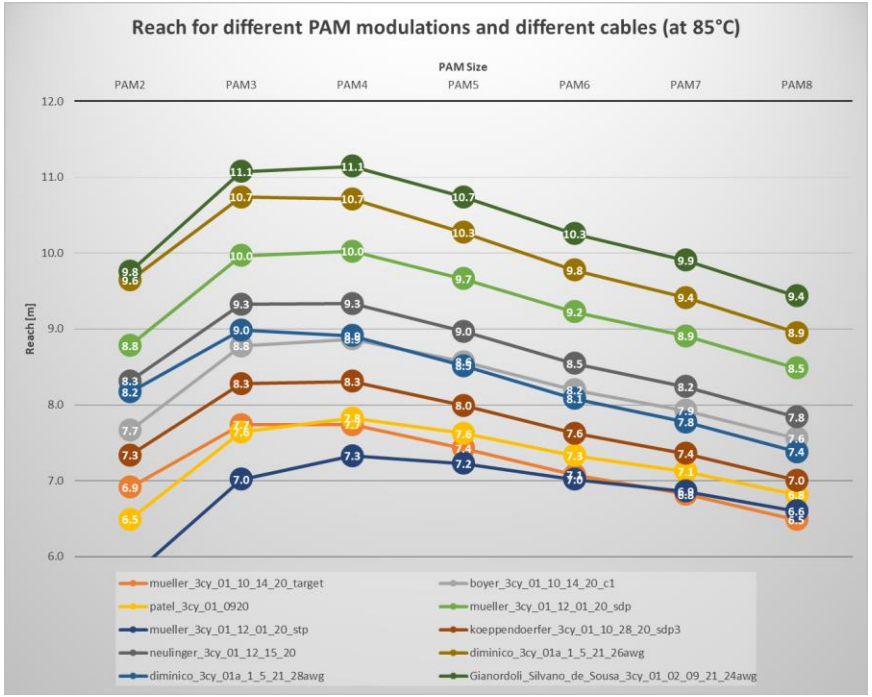






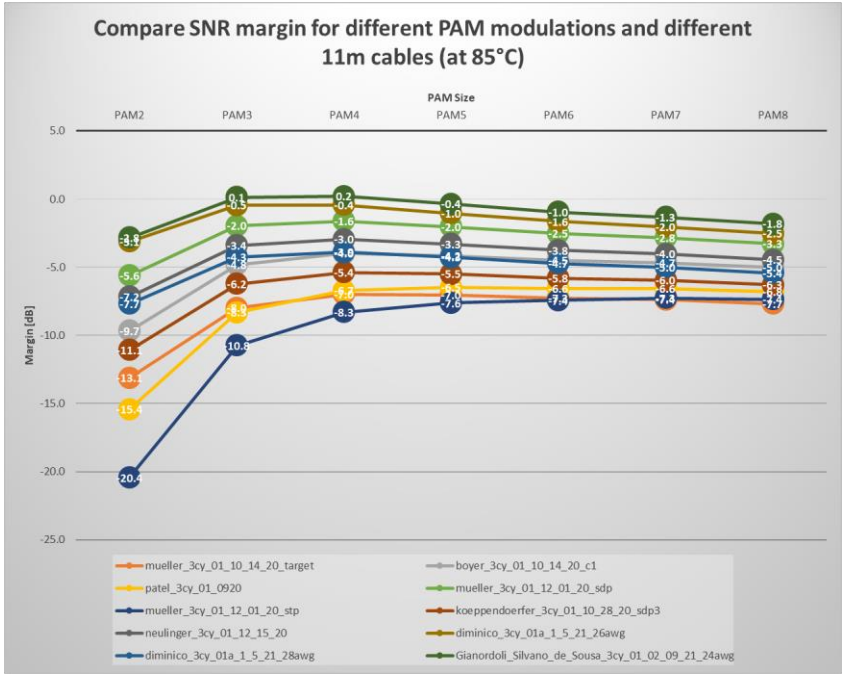
Reach for PAM Modulations

- The plot to the right shows achievable reach for different PAM modulations
- The reach was calculated using the CCC (jonsson_3cy_01_04_20_21), assuming **constant peak voltage**
- PAM4 is clearly a good candidate
- Note that this is simplified CCC calculation and does not account for inefficiency of fractional bit per symbol, error propagation, limitations on FEC, etc.

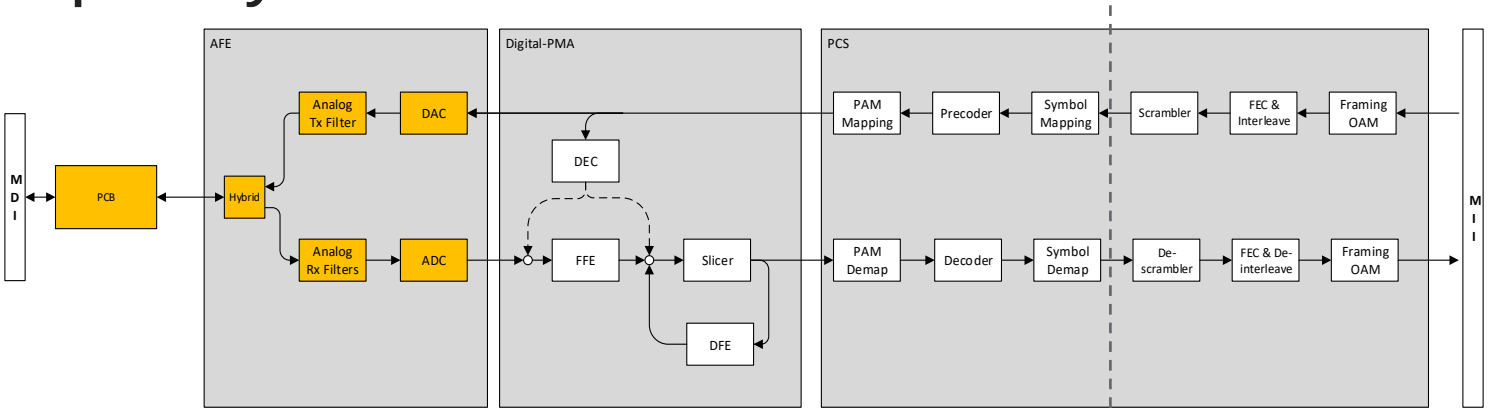


Performance of PAM Modulations

- In jonsson_3cy_01_08_03_21 we calculated the SNR margin for different PAM sizes, assuming **same transmit power**
- The calculations plotted to the right use **constant peak voltage** instead of constant power when comparing performance
- Using constant peak voltage favors lower PAM size, compared to constant power calculations



Complexity of Different PAM Modulations



Simplified PHY block diagram (implementations will vary)

Each PAM modulation impacts each part of the PHY design differently:

- Increasing PAM size will potentially lower the symbol rate
- Increasing PAM size will require higher SNR
- Increasing PAM size will potentially increase error propagation in DFE
- Increasing PAM size will potentially reduce FEC coding gain
- Increasing PAM size may need more bits in digital calculations and memory
- Increasing PAM size is potentially more sensitive to external noise, like RFI
- Different PAM size may result in different PCS design, including different FEC

PAM4 vs PAM5 Complexity

- PAM5 needs about 85% of the symbol rate of PAM4
- PAM5 will need about 3dB higher SNR
- PAM5 will have significantly higher probability of long error burst due to DFE error propagation, which will reduce the FEC coding gain
- PAM5 will need more bits in calculations and more memory, because of larger constellation size and higher SNR requirements
- PAM5 will be more sensitive to RFI, because of higher SNR requirements
- PAM5 would probably result in more complex PCS design than what is used in 802.3ch

- The complexity of PAM5 design would depend heavily on the implementation specifics
- Because PAM5 needs about 3dB higher SNR, the signal processing will need about 0.5 more effective bits
- Simple approximation of relative AFE power gives that PAM5 **probably** needs higher power than PAM4:

  $0.85 * (2^{0.5}) \approx 1.2$

- Simple approximation of Digital-PMA shows that PAM5 will **probably** have higher power consumption:

  $0.85 * (3/2)*(20/17) \approx 1.5$

- The PCS implementation for PAM5 is likely to more complex and have higher power consumption than PAM4 PCS

Note that the calculations above are over simplified and that the power consumption of any real PHY depends on the actual implementation

Benefits of PAM4

- PAM4 has been shown to give good performance across all cables and is the optimum modulation for many cables
  - jonsson_3cy_01_08_03_21
  - feyh_3cy_01a_08_03_21
  - sedarat_3cy_01_08_03_21
- PAM4 would make it efficient to develop multi-rate devices that support both 802.3cy and 802.3ch
- PAM4 is the “sweet spot” for 802.3cy

Compared to PAM5:

- PAM4 has better performance
- PAM4 is more power efficient
- PAM4 is less complex to implement
- PAM4 is more robust to RFI

Note that proper comparison of PAM5 and PAM4 would require specific proposals for PAM5 implementation, but it is unlikely that such comparison will be more favorable to PAM5

Conclusion

PAM4 modulation has many benefits for 802.3cy

No other modulation has been shown to perform better over multiple cables

We suggest to adopt 802.3ch like PAM4 modulation with precoding

Backup Slides

Simplified Comparison of PAM4 vs PAM5 Complexity

AFE Complexity Approximation

- The power consumption of the ADC and DAC with same ENOB will **roughly** scale linearly with the sampling rate
- The power consumption of the ADC and DAC will **roughly** double with each additional bit
- PAM5 symbol rate is approximately 0.85 times the symbol rate of PAM4
- PAM5 needs about 3dB better SNR than PAM4, which translates into about 0.5 bits more in the AFE
- Using the above, we can estimate that the AFE power for PAM5 relative to PAM4 is **roughly**

$$0.85 * 2^{0.5} = 1.2$$

Digital PMA complexity approximation

- The power consumption of the digital signal processing will **roughly** scale linearly with the sampling rate
- The power consumption of digital filters will **roughly** scale with the multiple of the data bits times the coefficient bits
- PAM5 needs 3 data bits for echo cancelers and DFE, compared to 2 for PAM4
- PAM5 needs about 20dB slicer SNR compared to 17dB for PAM4, which can be used as a crude estimate of the ratio of number of filter coefficient bits needed for PAM5 vs PAM4
- Using the above, we can estimate that the Digital PMA power for PAM5 relative to PAM4 is **roughly**

$$0.85 * (3/2)*(20/17) = 1.5$$

Note that the calculations above are over simplified and that the power consumption of any real PHY depends on the actual implementation

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