Scrambler Performance for Speed Beyond 25GBASE-T1

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Overview

- https://www.ieee802.org/3/cy/public/jul22/pandey_3cy_01_0722.pdf

- Replicating IEEE 802.3cy D2.0, 25GBASE-T1 PHY for future 50GBASE-T2 and 100GBASE-T4 will result in poor data randomness among lanes

- Simple replicating IEEE 802.3cy D2.0 PHY means all scramblers in 50G/100G PHY will have the same seed

- Having same seed for all scramblers means data out of those scramblers are highly correlated

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Assumption

- 50GBASE-T2 transmitter
  - Consists of two 25GBASE-T1 transmitters
- Each transmitter is driven by MAC frame
- RS(936,846) encoder
- 33-bits scrambler with polynomial as defined in IEEE 802.3cy D2.0
- PAM4 symbols from both transmitters are checked for degree of data randomness between two lanes using correlation function

MAC Frame	→	RS Coder	→	33-bits Scrambler	→	PAM4 Gray code
MAC Frame	→	RS Coder	→	33-bits Scrambler	→	PAM4 Gray code

Correlation

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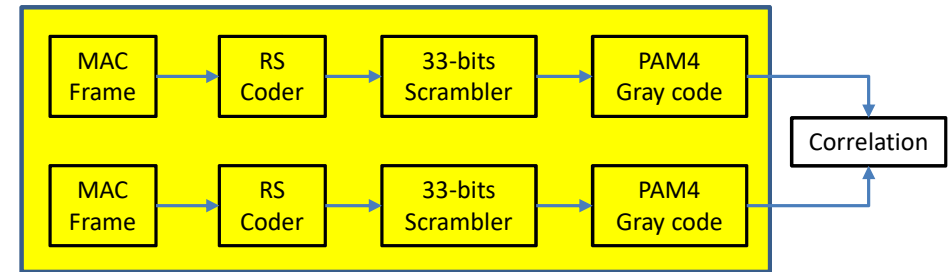
Simulation Results

- 50GBASE-T2 with two replicated 25GBASE-T1 PHYs having the same scrambler seed results in highly correlated between two lanes

- 50GBASE-T2 with two replicated 25GBASE-T2 PHYs having different scrambler seed that are sufficiently distanced apart results in close to statistically independent data between two lanes

- Note: both scramblers are 33-bits with same polynomial as defined in IEEE 802.3cy D2.0

Two scramblers with the exact same seed

Seeds that are sufficiently far apart
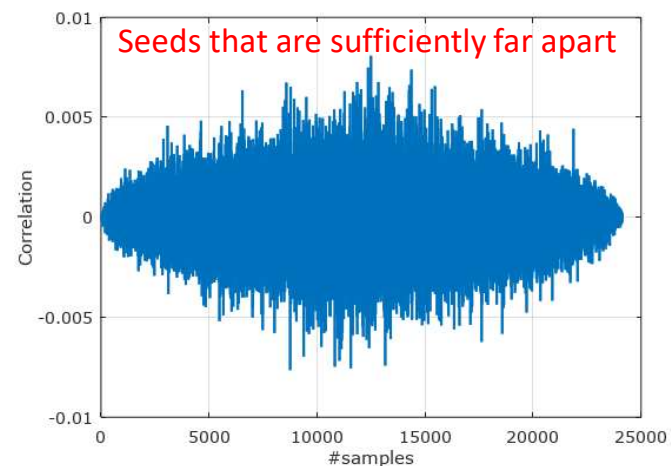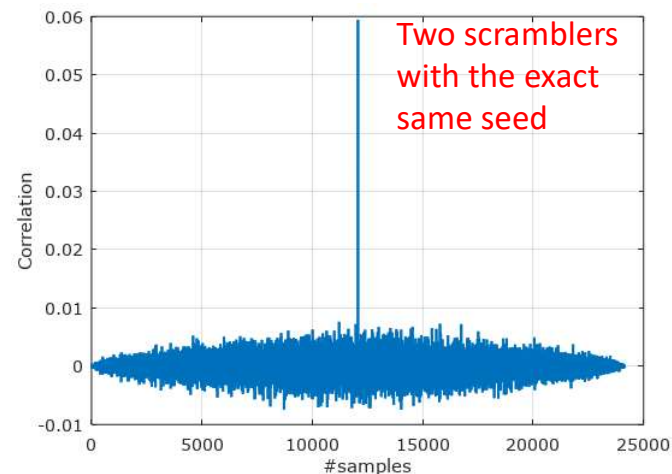
Propose Solution

- Goal: Enable a possibility to configure the scrambler states (seeds) for future PHYs
- 33-bits scrambler is already adopted in IEEE 802.3cy D2.0 draft and we keep it
- Current draft states that "… scrambler seed initialization is left to the implementer"
  - All scramblers use the exact same seed in 50G/100G mode when replicated 25GBASE-T1
- Suggestion
  - The initialization of the scrambler state is left to the implementer only for 25GBASE-T1 mode
  - For multilane (2 or 4) lanes mode, scrambler state is not left to the implementer. It shall be configured to maximize the data randomness between/among lanes
- The scrambler states initialization for 50G/100G will be defined by future task force
  - Seed value
  - How to configure

An implementation of MASTER and SLAVE PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 165–11. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

Conclusion

- 33-bits scrambler is just fine and we can keep it

- There is not a good reason to move to high order polynomial scrambler

- Scramblers with an exact same seed result in poor statistically independent data streams from lanes

- Enable a possibility to configure (not arbitrarily) the scrambler seeds to maintain better data randomness among lanes for future 50G and 100G PHYs

- Details about seeds its content and configuration should be defined by the future task force

THANK YOU