Considerations for a Multi-Speed Standard

IEEE 802.3cy – Beyond 10G Electrical Automotive Ethernet PHY TF

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Managing complexity – A proposal

- 3 PHY speeds, multiple use cases could be a complex project
- Borrow where we can, extend naturally:
  - 802.3ch – our highest automotive speed
    - Not too far off in speed/reach for 25 Gbps
    - Very far off for 100 Gbps
  - Other 802.3 clauses use laning of at least PMAs at high speeds
- Recommend an early decision
  - For discussion now, possibly for decision at a later meeting:
  - PROPOSED: Move that: 802.3cy specify a 25 Gbps PMA and link segment, which is reused as 2x or 4x for the 50Gbps and 100 Gbps objectives, leaving question of how to lane (and other PMA, FEC, and PCS parameters) open

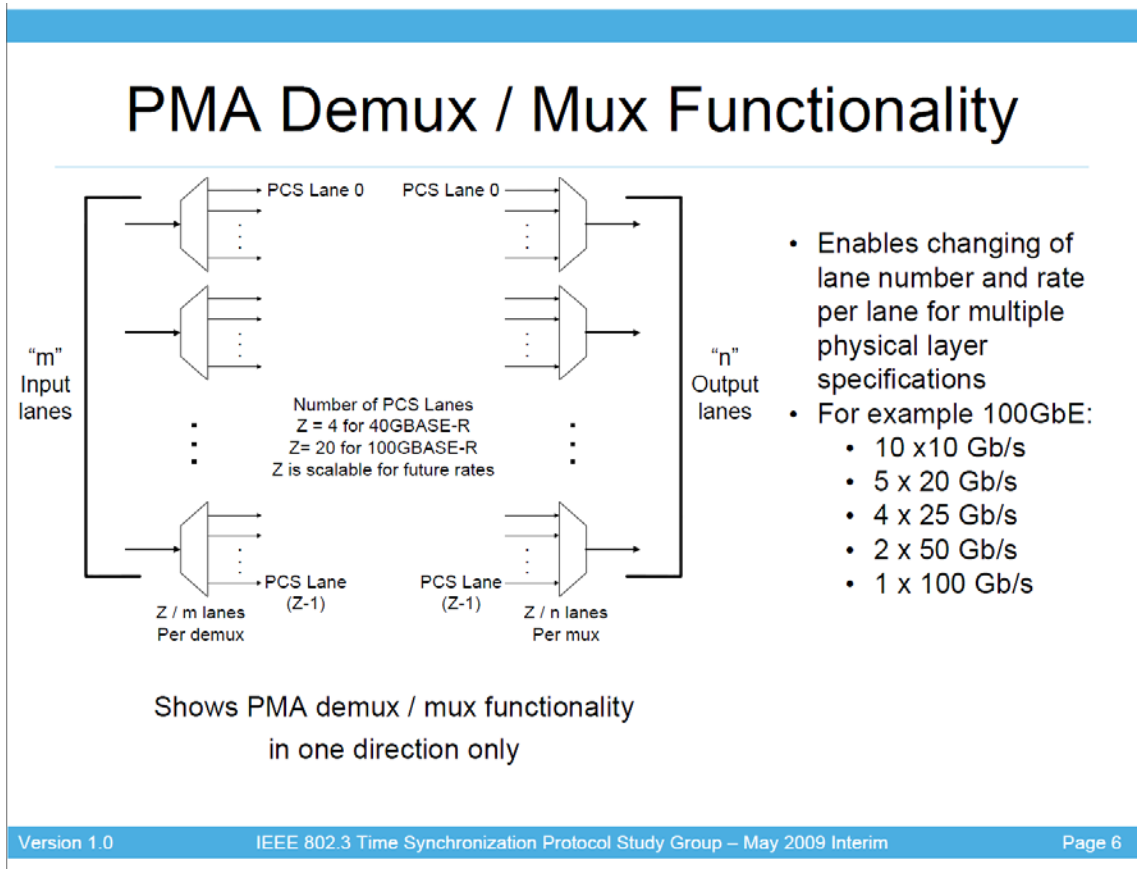
What do I mean “how to lane”?

- Several choices:
  - Lane PMA only as a unit? (combine at FEC)
    - Similar to BASE-T model, although FEC isn’t separate sublayer
  - Lane PMA & FEC as a unit? (combine at PCS)
    - Allows integration and repetition of a PMA/FEC with independent BER
  - Lane PMA/FEC/PCS as a unit? (combine at RS)
    - Allows independent PHY units to be bonded
  - (PCS & FEC can still be internally laned if needed)
    - Independent of PMA - this is done in optical PHYs

Parallelize at the PMA, Combine at the PCS

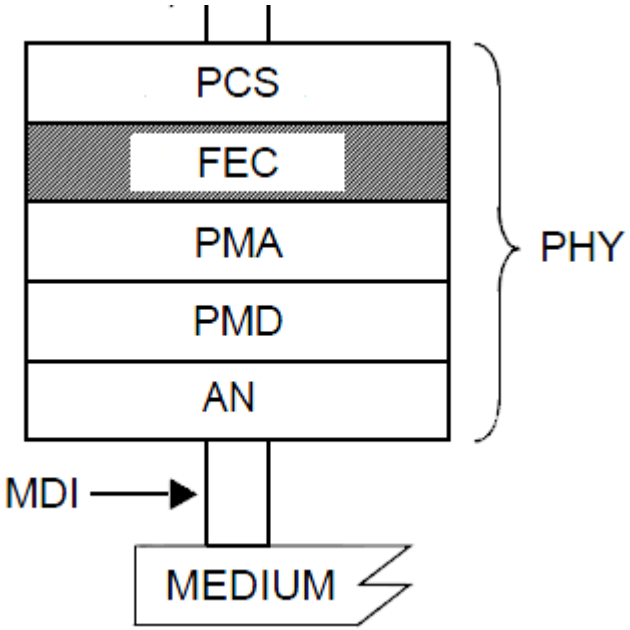
- PMA is the fundamental repeatable unit
- Link segments are identical
- Similar to BASE-T PHYs
  - Lane alignment in PCS
  - Complexity in PCS for bit multiplexing, FEC
  - Decisions on FEC drive complexity

http://www.ieee802.org/3/time_adhoc/public/apr09/dambrosia_03_0509.pdf



FEC as separate sublayer, Combine at the PCS

- PMA/FEC is the fundamental repeatable unit
- FEC is added as a separate sublayer between PMA and PCS
  - Architecture drives PCS laning at output
  - Includes bit mux for PMA lanes
  - May or may not be integrated into PMA
- Link segments are identical
- Adds FEC encode/decode to multi-lane PMA functions



Parallel PCS/FEC/PMA

- Bond above the MII at the MAC interface
- Allows reuse of the entire PHY (PCS/FEC/PMA) stack
- Uses multiple xMIIs
  - Could be multiple 25GMIIs
  - Departure from 50G/100GMII structure
  - As written in 802.3ca uses multiple MACs
- Would likely need specification of an automotive AUI and bond in the RS

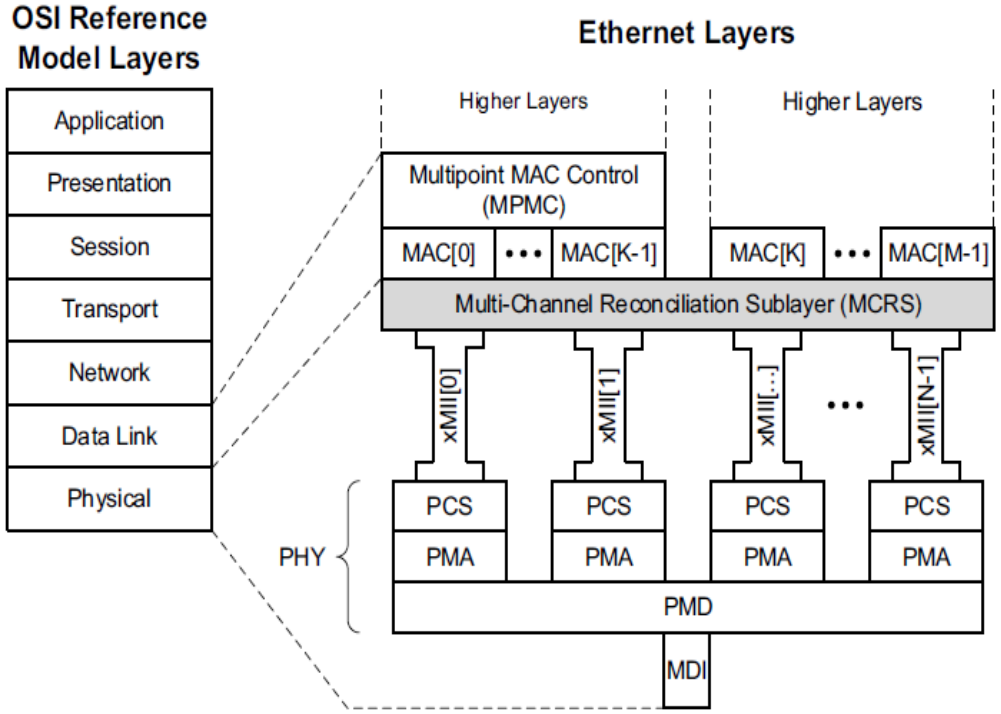


Figure 143–1—Relationship of MCRS to the OSI Reference Model

Source: IEEE Std 802.3ca-2020

Multi-lane PMA functions

Multi-lane processing

- Adapt the PCSL/FECL-formatted signal to the appropriate number of abstract or physical lanes.
- Provide bit-level multiplexing.
- Tolerate Skew Variation.

Per-lane processing

- Provide signal drivers.
- Perform line encoding and decoding, equalization, etc.
- Provide per-input-lane clock and data recovery.
- Provide clock generation.
- Optionally provide local loopback to/from the PMA service interface.
- Optionally provide remote loopback to/from the PMD service interface.
- Optionally provide test-pattern generation and checking.

Advantages

- Focuses link segment analysis on a single target
- Focuses PHY modulation, line coding, receiver performance specifications on a single target
- Minimizes bleeding edge high-frequency work
- Allows design reuse for less-common higher speed links

Decision to consider

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THANK YOU!

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