MARVELL

Slave Startup : Duration Of SILENT State And Defining timing_lock_OK

Seid Alireza Razavi Majomard, Ehab Tahir , and Ragnar Jonsson

June 7, 2022

Slave SILENT state in Current 802.3cy text

- Slave has to detect the infofield
  - "During startup, prior to entering the TRAINING state, the **SLAVE shall** align its transmit 65B RS-FEC frame to within +0/–4 partial PHY frames of the MASTER as seen at the SLAVE MDI. The SLAVE Infofield partial PHY frame count shall match the MASTER Infofield partial PHY frame count for the aligned frame"
  - Slave shall detect en_slave_tx = 1 in master infofield (PHY Control state diagram)
- The main task is making sure slave transmission does not cause problem for Master

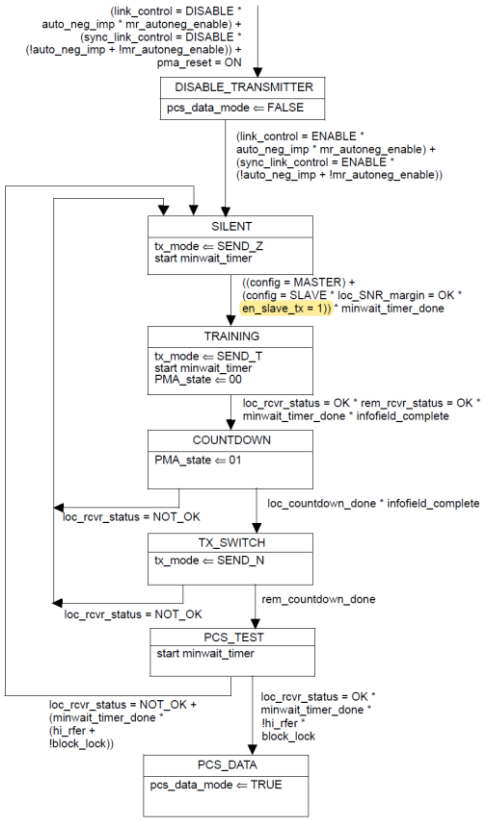

Figure 165–28—PHY Control state diagram

Legacy tasks in slave SILENT state

- Slave may
  - lock timing recovery
  - Initialize analog settings and equalizer
- Slave may lose the timing recovery lock as it starts to transmit
  - As “timing_lock_OK” bit in slave infofield can be either 0 or 1
- Master may train the initial echo canceler when slave is in SILENT state

Proposal I: Reduce the duration slave SILENT state

- Reduce the slave SILENT state to 20ms from 40ms
  - Master : From entry to SILENT state until en_slave_tx = 1 transmitted
  - Slave : Entry to exit of SILENT state
- Either reduce the total training time, or give more time for TRAINING state

Table 165–10—Startup timing maxima for MASTER

Timing interval	Maximum time (ms)
From entry to SILENT state until en_slave_tx = 1 is transmitted	40 – 0.384
From entry of SILENT state until entry to COUNTDOWN state	95.975 – 0.384
Entry to COUNTDOWN until entry of TX_SWITCH	0.384
Entry to exit of PCS TEST	1.025
Total (Entry to SILENT to exit of PCS TEST)	97

Table 165–11—Startup timing maxima for SLAVE

Timing interval	Maximum time (ms)
Entry to exit of SILENT state	40
Entry of SILENT state to exit of TRAINING state	95.975 – 0.384
Entry to COUNTDOWN until entry of TX_SWITCH	0.384
Entry to exit of PCS TEST	1.025
Total (Entry to SILENT to exit of PCS TEST)	97

Proposal II: Define timing_lock_OK

- Based on current standard text, slave can not set “timing_lock_OK” to zero after setting it to one
- However, the criteria for setting “timing_lock_OK” to one is NOT defined
- Possible solution: adding a language similar to requirement on master transmitter clock frequency in 165.5.3.6
  - After setting the “timing_lock_OK”, the slave transmitter clock short-term rate of frequency variation shall be less than TBD ppm/second

MARVELL

Thank You