

# 802.3cy PMA Training Frame

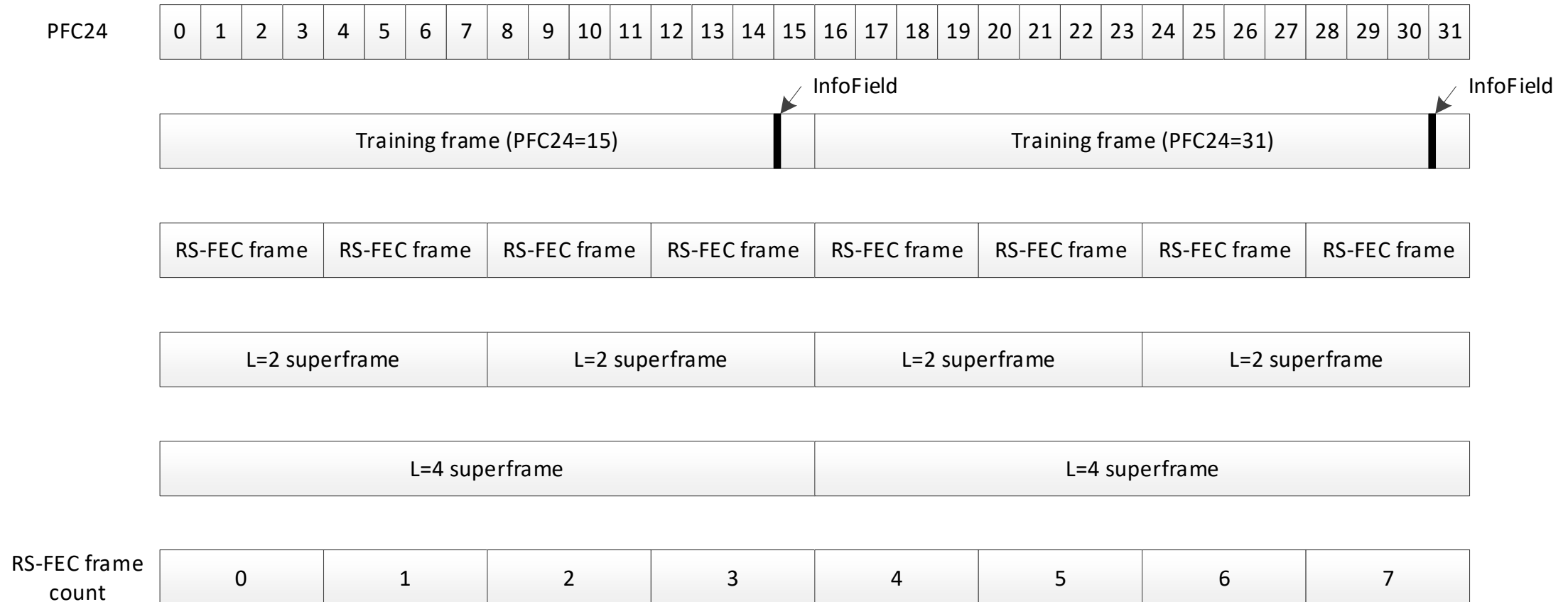
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# Introduction to PMA Training Frame

- Transmitted from both MS and SL during PMA training states
- Pseudo random PAM2 sequences
- Enables the following
  - SL timing recovery
  - Receiver convergence
  - Alignment with data mode interleaved FEC superframe boundaries
  - Exchange InfoField bits
- InfoField
  - PHY capabilities: OAM, EEE, EEE slow wake
  - Receiver preference: interleaving depth, precoder selection
  - Status bits and counter values driving the PHY control state machine
  - 12 octets (96 bits) in 802.3ch
    - 4 RESERVED bits in the MSG octet
    - 1 RESERVED bit in the PHY capability bits

# 802.3ch PMA Training Frame and RS-FEC Superframe Alignment



149.4.2.4.6: DataSwPFC24 shall be set to an integer multiple of 16.

L=4 superframe boundary aligned with PFC24=n, where  $n \bmod 16 = 0$ .

# Reserved Bits within Octet 7 (PMA\_state=00 or 01)

**Table 165–9—Infocfield message field valid MASTER settings**

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

**Table 165–10—Infocfield message field valid SLAVE settings**

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

# Reserved Bit within PHY Capability Bits (PMA\_state=00)

Table 165–11—PHY capability bits

octet 8								octet 9								octet 10									
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7		
VendorSpecificData															Reserved	InterleaverDepth		PrecodeSel		SlowWakeRequest		EEEEen		OAMen	

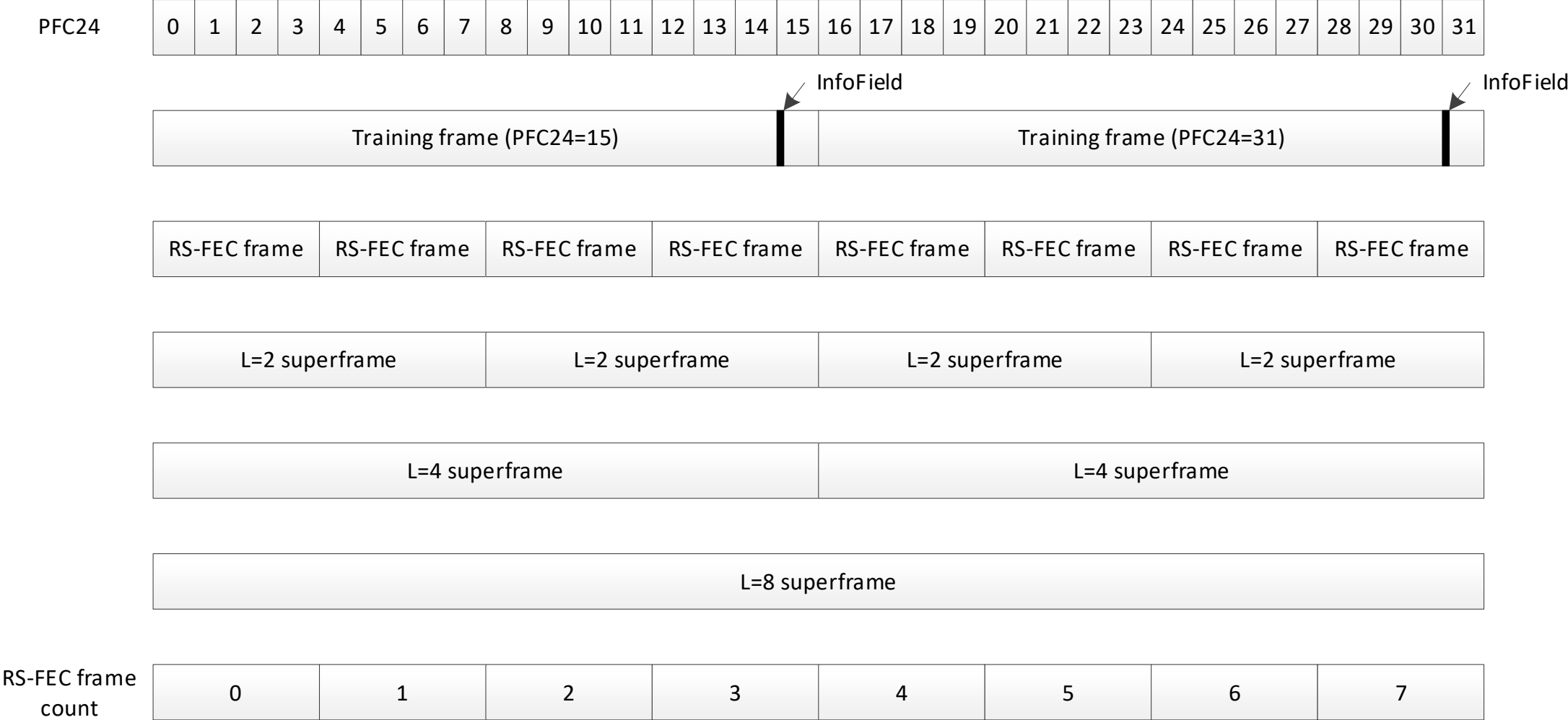
# Proposal for 802.3cy PMA Training Frame

- Based on 802.3ch
- 1 PMA training frame = 4 RS-FEC frames
- 16 partial PHY frames per PMA training frame
- Start with 12 octets (96 bits) of InfoField
  - May use existing 5 RESERVED bits if necessary
  - May add more octets later on if necessary
- InfoField at the first 96 bits of partial frame 15, 31, etc.
- L=8 RS-FEC superframe boundary aligned with PFC24=n, where  $n \bmod 32 = 0$

# PMA Training Frame: 802.3ch vs. 802.3cy Proposal

	802.3ch	802.3cy	Comments
FEC	RS (360,326,m=10)	RS (936,846,m=10)	
PHY frame	320 ns	332.8ns	
PAM2 training frame	1280 ns 7200 PAM2 symbols	1331.2 ns 18720 PAM2 symbols	
Partial PHY frame	16 per PMA training frame 450 PAM2 symbols	16 per PMA training frame 1170 PAM2 symbols	
PFC counter	24 bits	24 bits	
IF octets	12	12	Use 2 reserved bits for lane number?
DataSwPFC24	Multiples of 16	Multiples of 32	Aligned with L=8 RS-FEC superframe

# Proposed Figure 165-12



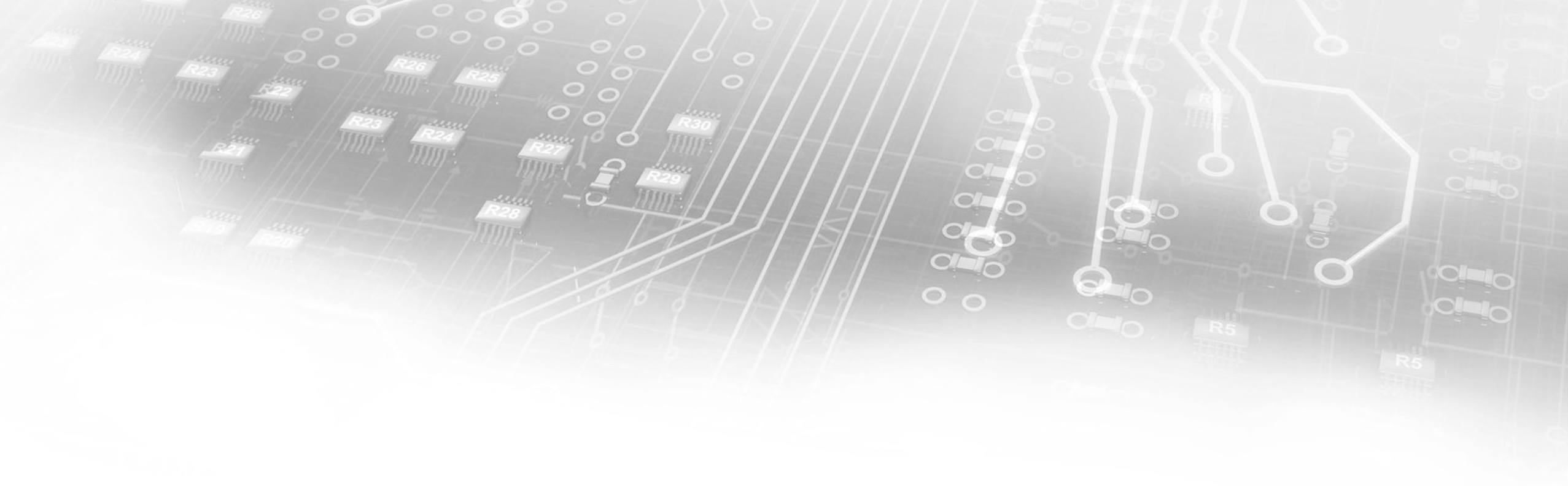


## Proposed Equation 165-7

- $$S_n = \begin{cases} Scr_n[0] \oplus InfoField_{(n \bmod 1170)} & 17550 \leq (n \bmod 18720) \leq 17645 \\ Scr_n[0] \oplus 1 & \text{else if } (n \bmod 1170) = 0 \\ Scr_n[0] & \text{otherwise} \end{cases}$$

## Proposed Changes to 165.4.2.4.6

- Page 140, Line 8-10
- 165.4.2.4.6 Data switch partial PHY frame count
- ...
- The last value of PFC24 prior to the transition is  $\text{DataSwPFC24} - 1$ .  
DataSwPFC24 shall be set to an integer multiple of 32. When the value of DataSwPFC24 is a multiple of 32 the switch from PAM2 to PAM4 occurs on a PHY frame boundary.



# Questions / Comments?

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## Motion

- Move to adopt the 802.3cy PMA training frame related proposals as shown on page 8, 9, and 10 in “tu\_3cy\_02\_03\_08\_2022.pdf”
- M: Mike Tu
- S:
- Technical ( $\geq 75\%$ )
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