802.3cy
Test Fixture Proposals

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802.3cy Test Points

Assuming Clause149 PHY sublayers

165.5 PMA electrical specifications

165.5.1 Test modes

[TBD]

165.5.2 Test Points

For reference, test points for Clause 165 PHYs are defined in one direction as shown in Figure ***165-x1***. Clause 165 PHYs use bidirectional signal lines in full duplex operation. As a result, TP1 and TP4 are physically identical, as are TP0 and TP5. They are shown here separately for reference in discussing parameters at the transmitter vs. the receiver.

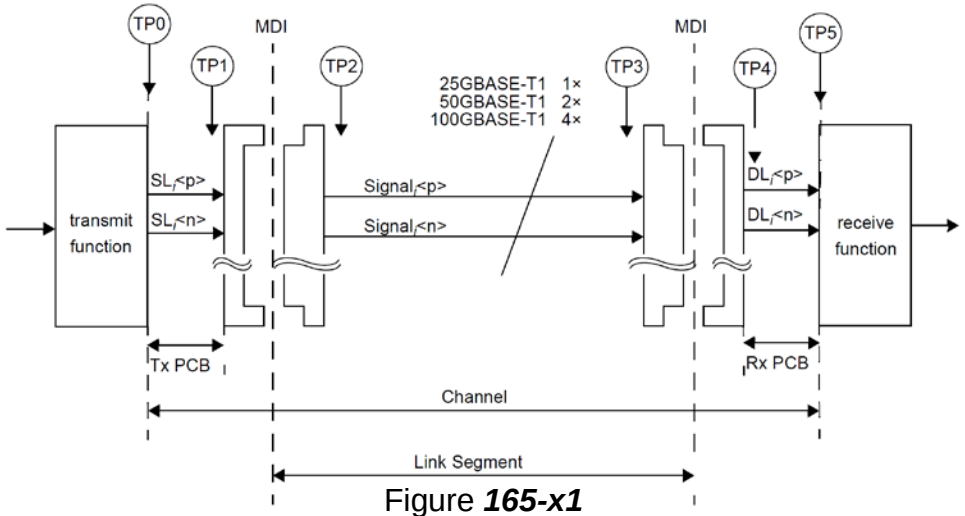


Figure ***165-x1***

Note that the source lane (SL) signals SLi<p> and SLi<n> are the positive and negative sides of the transmitter end's differential signal pair on lane i and the destination lane (DL) signals DLi<p> and DLi<n> are the positive and negative sides of the receiver end's differential signal pair on lane i.

Table ***165-y1*** describes the defined test points illustrated in Figure ***165-x1***.

802.3cy Test Points (continued)

Table 165-y*1*: Test Points

Test points	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance PCB insertion loss and the link segment insertion loss.
TP1 to TP4	All link segment measurements are made between TP1 and TP4 as illustrated in xxx.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 165.5.3 and 165.5.4***(TBD).***
TP2	Unless specified otherwise, all transmitter measurements defined in 165.5.3 are made at TP2.
TP3	TP3 represents the link partner's TP2 test point.

802.3cy Transmitter electrical specifications (use of test points)

165.5.3 Transmitter electrical specifications

The PMA provides the Transmit function specified in ***165.4.2.2?*** in accordance with the electrical specifications of this clause. Unless specified otherwise, all transmitter measurements and tests defined in 165.5.3 are made at TP2 utilizing a test fixture that meets the specifications ***165.5.5***.

Editor's note – reviewers to consider proposing additional text for this subclause from 149.5.2

A mated connector pair has been included in the transmitter specifications defined in this subclause.

Editor's note – the following paragraph tells the reader what to look in the Annex for. It will need to be updated as Annex content develops.

Informative Annex 165A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system. The recommended maximum insertion loss from TP0 to TP2 (or TP3 to TP5) including the test fixture is provided in ***Annex 165A***. ***Annex 165A*** also includes parameters related to recommended differential controlled impedance printed circuit board parameters.

Editor's note – contributors to consider text for transmit droop, linearity, and jitter specifications

(NOTE TO EDITOR – Transmit PSD and power level text, differential output, and clock frequency previously adopted goes here as at the 165.5.3.x level)

Intervening sections – Receiver electrical specifications (TBD)

165.5.4 Receiver electrical specifications

Editor's note – consider tests from 149.5.3, as well as contributions for potential additional tests. These should consider whether there are any requirements relevant to TP3 as an input.

802.3cy Test Fixtures

165.5.5 Test fixtures

Specifications for a Host Test Fixture (HTF) for tests at TP2, and for a Link segment Test Fixture (LSTF) for measurements between TP1 and TP4 are defined. The test fixtures are specified in a mated state in ***165.5.5.3***.

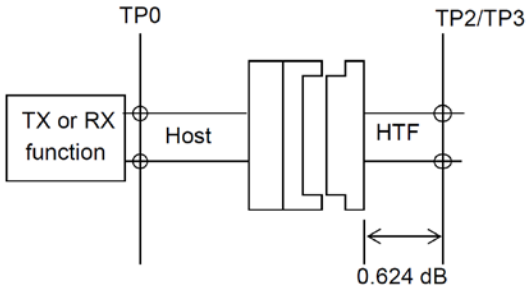
165.5.5.1 Host Test Fixture

The test fixture for measurements at TP2/TP3 is shown in Figure ***165-x2***. Due to the symmetry of the transceiver, this test fixture provides access to TP2 and TP3.

The HTF printed circuit board (PCB) insertion loss values determined using Equation ***165-z1*** is used as the HTF reference insertion loss (IL_{htf_ref}).

$$IL_{htf\_ref}(f) = (0.09144*(f_{MHz}/1000)+0.51054*(f_{MHz}/1000)\text{^}0.45)*0.3334 \text{ dB} \quad \textbf{\textit{(165-z1)}}$$

The reference insertion loss of the TP2 or TP3 test fixtures is 0.624 dB @ 7031.25 MHz using Equation ($IL_{htf\_ref}(f)$). The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the measurements.



NOTE – dB losses shown are reference losses at 7031.25 MHz, actual fixture losses may be different, but are to be accounted for in measurements

HTF: Figure 165-x2

802.3cy Test Fixtures

165.5.5.2 Link Segment Test Fixture

The link segment test fixture (LSTF) is used for measuring the link segment defined in ***165.7*** at TP1 and TP4. The relation of the LSTF and the TP1 and TP4 test points is illustrated in Figure ***165-x3***. One LSTF is used at either end of the link segment under test.

The link segment test fixture PCB and test point insertion loss values determined using Equation ***165-z2*** is used as the test fixture reference insertion loss. The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the measurements. The reference insertion loss of the link segment test fixtures is 0.624 dB @ 7031.25 MHz.

$$IL_{lstf\_ref}(f) = (0.09144*(f_{MHz}/1000)+0.51054*(f_{MHz}/1000)\text{^}0.45)*0.3334 \quad \textbf{(165-z2)}$$

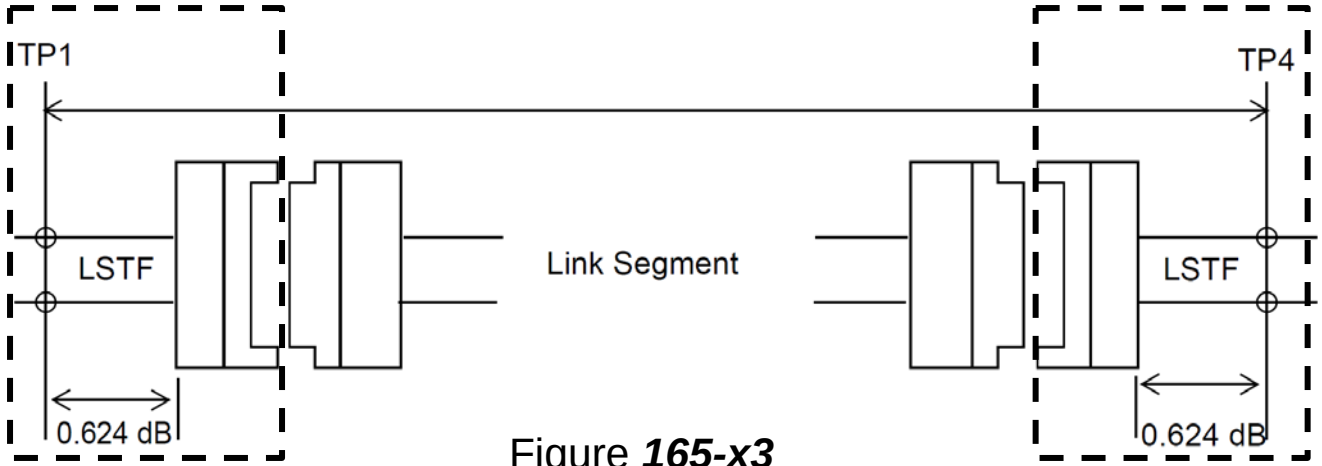


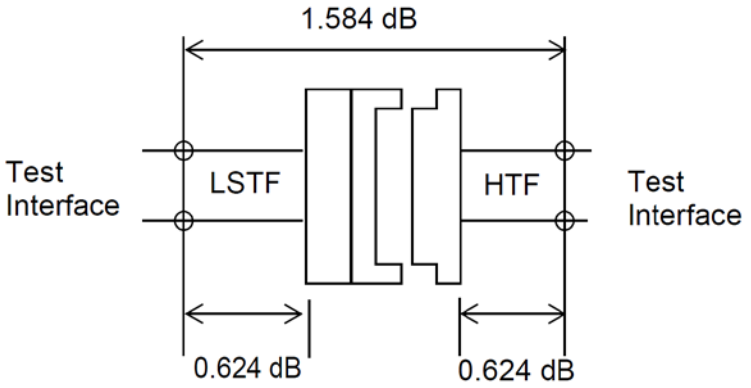
Figure ***165-x3***

802.3cy Test Fixtures

165.5.5.3 Mated Test Fixtures

The HTF and LSTF are specified in a mated state illustrated in Figure ***165-x4***, to enable connections to measurement equipment.

Figure ***165-x4***.



165.5.5.3.1 Insertion loss

The measured insertion loss of the mated test fixtures shall meet the values determined using Equation ***165-z3*** and Equation ***165-z4***.

$$IL(f) \le IL_{mtfmax}(f) = \textbf{TBD}(f) \qquad \textbf{(165-z3)}$$

$$IL(f) \ge IL_{mtfmin}(f) = \textbf{TBD}(f) \qquad \textbf{(165-z4)}$$

Where IL (f) is the measured mated test fixture insertion loss

The reference insertion loss of the mated test fixture is determined using Equation ***165-z5***. The reference insertion loss of the mated test fixture is 1.584 dB @ 7031.25 MHz.

$$IL_{mtf\_ref}(f) = (0.06109*(f_{MHz}/1000)+0.3404*(f_{MHz}/1000)\text{^}0.45)+(0.2*SQRT(f_{MHz}/2500)) \qquad \textbf{(165-z5)}$$

802.3cy Test Fixtures

165.5.5.3.2 Return loss

The Return loss of the mated test fixtures shall meet the values determined using Equation ***165-z6***.

$$RL_{mtf}(f) \geq \textbf{TBD}(f) \qquad \textbf{(165-z6)}$$

165.5.5.3.3 Mode Conversion

The Mode Conversion of the mated test fixtures shall meet the values determined using Equation ***165-z7***.

$$ConversionLoss_{mtf}(f) \geq \textbf{TBD}(f) \qquad \textbf{(165-z7)}$$

165.5.5.3.4 Crosstalk

The crosstalk loss of the mated test fixtures shall meet Equation ***165-z8***.

$$XTF_{mtf}(f) \geq \textbf{TBD}(f) \qquad \textbf{(165-z8)}$$

802.3cy Link Segment (use of test fixtures)

***165.7* Link segment characteristics**

(Editor's note – this introductory paragraph has been adopted from clause 149 – for the Task Force to consider. It is based on previous decisions and is not intended to provide new requirements, but is needed to introduce the use of TP's for the link segment specs)

25GBASE-T1, 50GBASE-T2, and 100GBASE-T4 are designed to operate over a one, two, or four shielded balanced pairs of conductors, respectively, that meet the requirements specified in this subclause. Each shielded balanced pair of conductors supports an effective data rate of 25 Gb/s in each direction simultaneously. The term link segment used in this clause refers to the appropriate number of balanced pairs of conductors (cable or backplane) operating in full duplex.

All link segment measurements are between TP1 and TP4 as illustrated in Figure ***165-x1***. Two link segment test fixtures, specified in ***165.5.5.2***, or equivalent are used for measuring the link segment specifications as illustrated in Figure ***165-x3*** at TP1 and TP4. Two link segment test fixtures have been included in the specifications shown in ***165.7.1***

165.7.1 Link transmission parameters

The transmission characteristics for the link segment are specified to support operation over automotive temperature and electromagnetic conditions.

165.7.1.1 Insertion loss

Note to editor – adopted insertion loss for the link segment alone goes first here, as $IL_{Linksegment}$

The insertion loss from TP1 to TP4 shall meet Equation ***169-z9,*** where the insertion loss of the MDI connector is $0.1 \times \sqrt{\frac{f_{MHz}}{2500}}$.

$$IL_{TP1-TP4}\,(dB) \leq 2 \cdot IL_{LSTF\_ref} + 2 \cdot IL_{MDIconnector} + IL_{Linksegment} \qquad \textbf{165-z9}$$

Annex 165A (informative) Tx Function to Rx function channel characteristics

Note – Needs surrounding text and work. Natalie to write text and build consensus around format similar to Annex 149-C (this is provided here for context)

Tx Function to Rx function channel IL

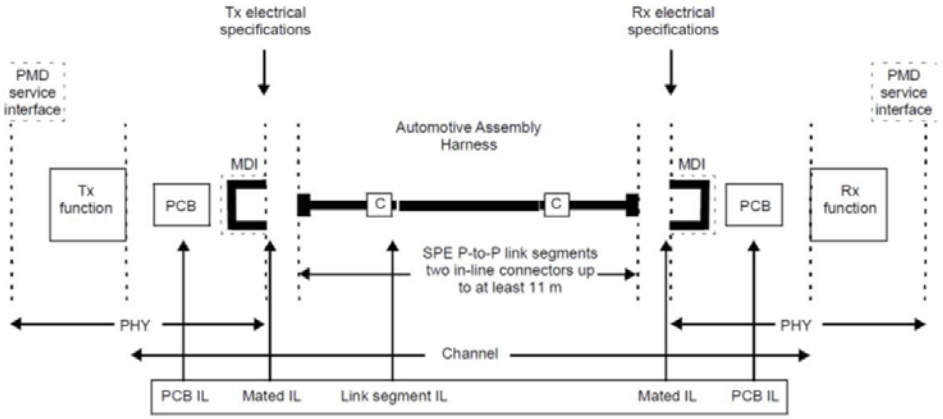


Figure 165A-x1

$$IL_{Channel}\,(dB) \leq 2 \cdot IL_{PCB} + 2 \cdot IL_{MDI} + IL_{Linksegment}$$

$$IL_{PCB}(dB) \leq 0.09144\left(\frac{f_{MHz}}{1000}\right) + 0.51054\left(\frac{f_{MHz}}{1000}\right)^{0.45}$$

$$IL_{LinkSegment}(dB) \leq 0.00135(f_{MHz}) + 0.3564(f_{MHz})^{0.45} + 0.495\left(\frac{f_{MHz}}{7500}\right)^{6}$$

$$IL_{MDI}(dB) \leq 0.1\sqrt{\frac{f_{MHz}}{2500}}$$

PHY	MBd	Bandwidth (MHz)	IL PCB	IL Link Segment	IL MDI	IL Channel
25GBASE-T1	14 062.5	7031.25	1.871	29.02	0.168	33.098

Text for Annex 165A on reference IL

165A.2 TP0 to TP2 Reference Insertion Loss

The recommended maximum insertion loss from TP0 to TP2 (or TP3 to TP5) including the test fixture is shown in Figure ***165A-x2***. Figure ***165A-x2*** includes the host PCB, a mated connector pair, and the HTF recommended insertion losses. All losses shown are at 7031.25 MHz.

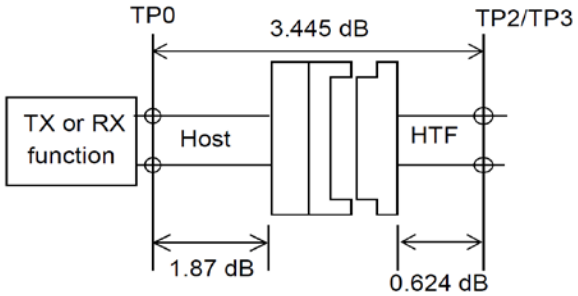


Figure ***165-x4***

Note – This part of the annex is worked, but goes into the framework shown on the preceding page that Natalie is still working around format similar to Annex 149C

Text Ready for Motions (separate)

- Test point definition: slides 2 & 3
- Use of TPs/fixtures with Transmitter electrical specifications: slide 4
- Receiver electrical specifications (TBD): slide 5
- Specification of HTF & LSTF test fixtures: slides 6-9
- Use of TPs/fixtures with Link Segment specs: slide 10
- Annex reference IL material: slide 12

- Still needs work: Annex block diagram material – pending Natalie – slide 11

Motions

Move to adopt test point definitions slide 2-3 diminico_et_al_3cy_01b_10_12_21.pdf with editorial license.

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Move to adopt test fixture specifications Slide 6-9 diminico_et_al_3cy_01b_10_12_21.pdf with editorial license.

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Move to adopt link segment content Slide10 diminico_et_al_3cy_01b_10_12_21.pdf with editorial license.

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Move to adopt text for Annex 165A Slide 12 diminico_et_al_3cy_01b_10_12_21.pdf with editorial license.

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