
802.3cy

Test Fixture Considerations

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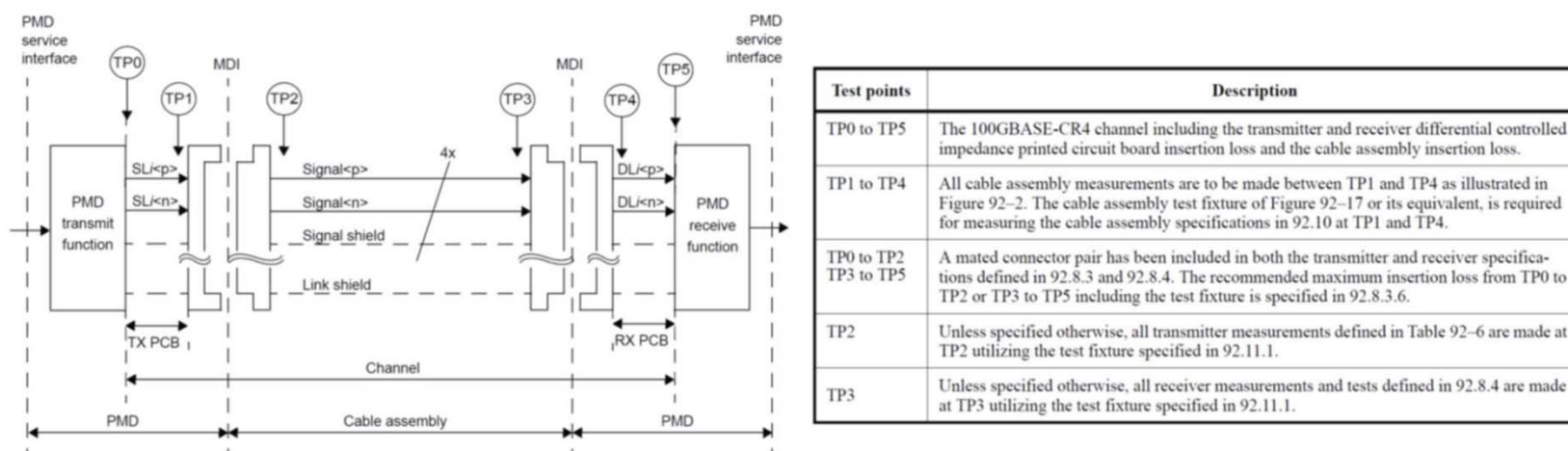
Purpose

- **Test Points**
- **Test Fixture Considerations**
 - **Use 802.3cy Channel PCB IL and connector IL assumptions to formulate 802.3cy test fixture IL**
 - **Test fixtures specified in a mated state**
- **Tx Function to Rx function channel characteristics**

Background –Test Points

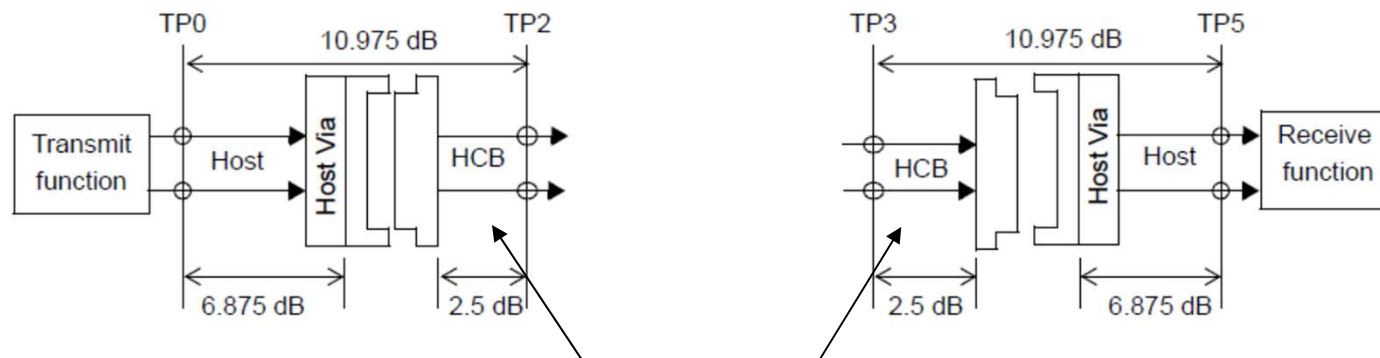
Background – 802.3bj/by/cd/ck

- The channel is defined between the transmitter and receiver blocks to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly (link segment).
- Test points provide specification references for channel and cable assembly and RX and TX
- Test fixtures enable testing at test points – module compliance board (MCB); host compliance board (HCB)



https://www.ieee802.org/3/cy/public/adhoc/diminico_3cy_01a_04_27_21.pdf

Background –Test Fixtures- Host Compliance Board



Host Compliance Board (TP2 or TP3) - Plug in at TP2 or TP3 for TX and RX measurements – PCB IL minimized

Table 162–10—Summary of transmitter specifications at TP2

Parameter	Subclause reference	Value	Units
Signaling rate, each (nominal)		53.125 ± 50 ppm ^a	GBd
Differential pk-pk voltage with Tx disabled (max) ^b	93.8.1.3	30	mV
DC common-mode voltage (max) ^b	93.8.1.3	1.9	V
AC common-mode RMS voltage, v_{cmf} (max) ^b	93.8.1.3	30	mV
Differential pk-pk voltage, v_{df} (max) ^b	93.8.1.3	1200	mV
Effective return loss, ERL (min)	162.9.3.5	7.3	dB
Common-mode to common-mode return loss (min)	162.9.3.6	2	dB
Common-mode to differential return loss (min)	162.9.3.7	See Equation (162–5)	dB
Transmitter steady-state voltage, v_T (min)	162.9.3.1.2	0.387	V
Transmitter steady-state voltage, v_T (max)	162.9.3.1.2	0.6	V
Linear fit pulse peak ratio (min)	162.9.3.1.2	0.397	—
Level separation mismatch ratio R_{LM} (min)	120D.3.1.2	0.95	—
Transmitter output waveform ^c			
absolute value of step size for all taps (min)	162.9.3.1.4	0.005	—
absolute value of step size for all taps (max)	162.9.3.1.4	0.025	—
value at minimum state for $c(-3)$ (max)	162.9.3.1.5	-0.06	—
value at maximum state for $c(-2)$ (min)	162.9.3.1.5	0.12	—
value at minimum state for $c(-1)$ (max)	162.9.3.1.5	-0.34	—
value at minimum state for $c(0)$ (max)	162.9.3.1.5	0.5	—
value at minimum state for $c(1)$ (max)	162.9.3.1.5	-0.2	—
Signal-to-noise-and-distortion ratio, SNDR (min) ^d	162.9.3.3	31.5	dB
Output jitter (max)			
J_{RMS}	162.9.3.4	0.023	UI
$J_{3\sigma}$	162.9.3.4	0.115	UI
Even-odd jitter, pk-pk	162.9.3.4	0.025	UI

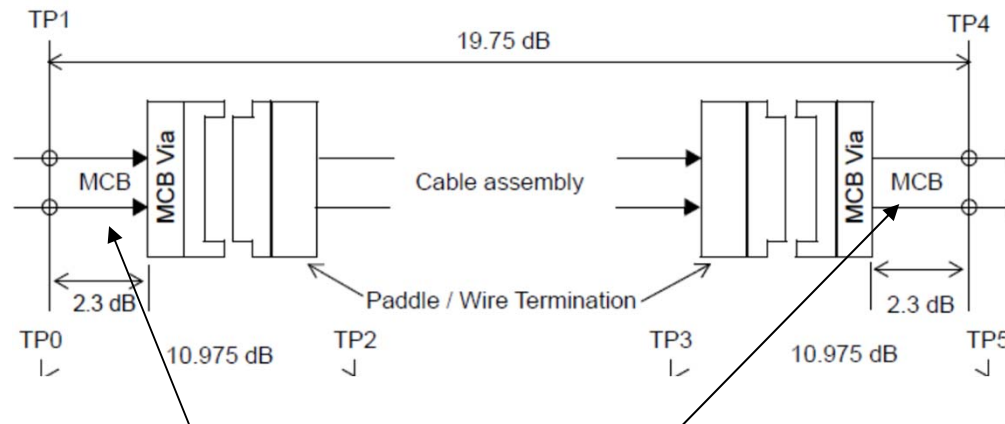
Table 162–14—Summary of receiver specifications at TP3

Parameter	Subclause reference	Value	Units
Signaling rate	162.9.4.1	53.125 ± 100 ppm	GBd
Amplitude tolerance	162.9.4.2	1200 ^a	mV
Interference tolerance	162.9.4.3	Table 162–15	—
Jitter tolerance	162.9.4.4	Table 162–16	—
Effective return loss, ERL (min)	162.9.4.5	7.3	dB
Differential to common-mode return loss (min)	162.9.4.6	Equation (162–16)	dB

^aAmplitude is measured at TP2.

Source: IEEE P802.3ck™/D2.0, 10th March 2021

Background –Test Fixtures - Module Compliance Board



Module Compliance Board or Cable Assembly Test – PCB IL to emulate minimum host IL

Table 162-17—Cable assembly characteristics summary

Description	Reference	Value	Unit
Maximum insertion loss at 26.56 GHz	162.11.2	19.75	dB
Minimum insertion loss at 26.56 GHz	162.11.2	11	dB
Minimum cable assembly ERL ³	162.11.3	8.25	dB
Differential to common-mode return loss	162.11.4	Equation (162-18)	dB
Differential to common-mode conversion loss	162.11.5	Equation (162-19)	dB
Common-mode to common-mode return loss	162.11.6	Equation (162-20)	dB
Minimum COM	162.11.7	3	dB

³Cable assemblies with a COM greater than 4 dB are not required to meet minimum ERL.

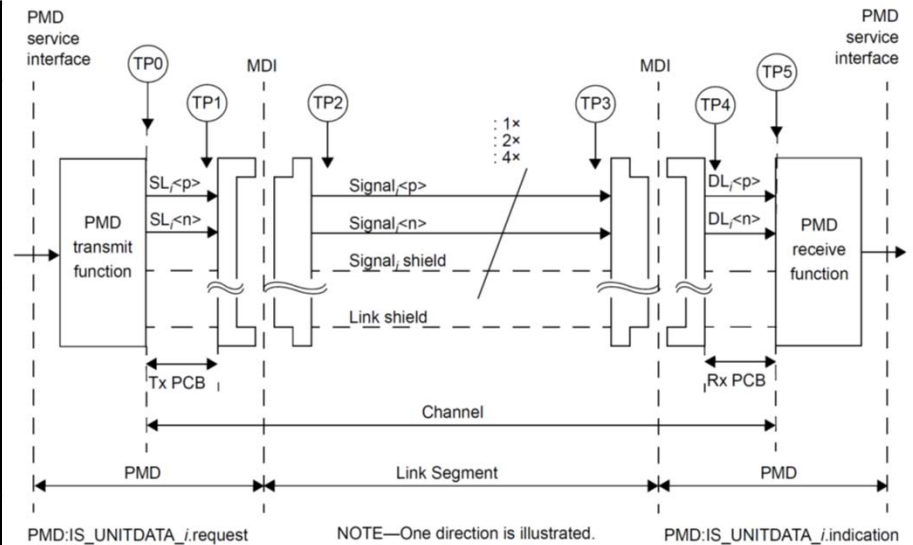
Source: IEEE P802.3ck™/D2.0, 10th March 2021

802.3cy Test Points

Test Points

Test points	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance PCB differential-mode to differential-mode insertion loss and the link segment differential-mode to differential-mode insertion loss.
TP1 to TP4	All link segment measurements are made between TP1 and TP4 as illustrated in xxx. The link segment test fixture of xxx, or its equivalent, is required for measuring the link segment specifications in xxx at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in xxx and xxx. The recommended maximum differential-mode to differential-mode insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in xxx.
TP2	Unless specified otherwise, all transmitter measurements defined in xxx are made at TP2 utilizing the test fixture specified in xxx.
TP3	Unless specified otherwise, all receiver measurements and tests defined in xxx are made at TP3 utilizing the test fixture specified in xxx.

Test Point Figure



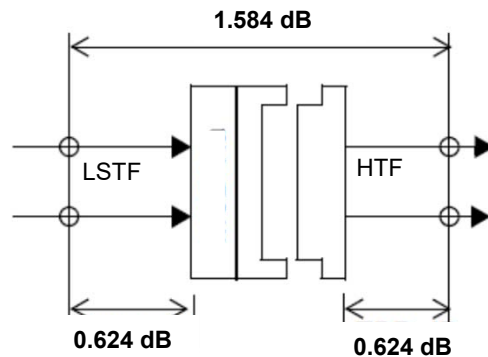
Assuming Clause 149 PHY sublayers

XXX.X PMA electrical specifications

- Test Points
 - Test Point Figure
 - Test point Table

802.3cy Test Fixtures

- Test fixture specified in a mated state
- Use 802.3cy Channel PCB IL and connector IL to formulate 802.3cy test fixture IL
- Use mated test fixture measurements/models to develop test fixture parameter limits



Mated cable assembly
and test point test fixture

Link Segment Test Fixture (LSTF)
Host Test Fixture (HTF)

PCB IL @ 7031.25 MHz for 25.4 mm (1 in) = 0.624 dB

PCB IL @ 7031.25 MHz for 76.2 mm (3 in) = 1.871 dB

MDI IL @ 7031.25 MHz = 0.168 dB

Plug IL @ 7031.25 MHz = 0.168 dB

*Mated Test Fixture @ 7031.25 MHz = 2*0.624 dB+2*0.168 dB = 1.584 dB*

In XXX.XX PMA electrical specifications - Test Fixtures

XXX.XX Link Segment Test Fixture

- Insertion loss

XXX.XX Host Test Fixture

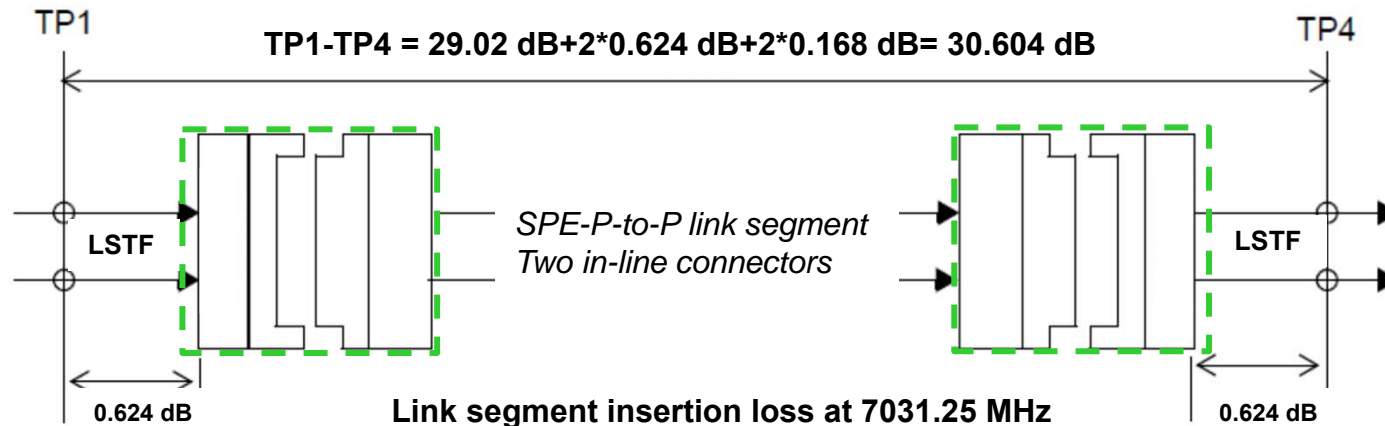
- Insertion loss

XXX.X Mated Test Fixture

Insertion loss(f)
Insertion loss reference – Max 1.584 dB @ 7031.25 MHz, Min @ 7031.25 MHz
Return Loss(f) -
Common-mode conversion insertion loss(f)
Common-mode return loss(f)
Common-mode to differential – mode return loss (f)
Crosstalk(f)

802.3cy-TP1-TP4 Link Segment

TP1 to TP4	Test points for all link segment measurements. The link segment test fixture, or its equivalent, is required for measuring the link segment specifications in xxx.xx at TP1 and TP4.
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$$IL_{TP1-TP4} (dB) \leq 2 \cdot IL_{HSTFPCB_{25.4 \text{ mm}}} + 2 \cdot IL_{connector} + IL_{Linksegment}$$

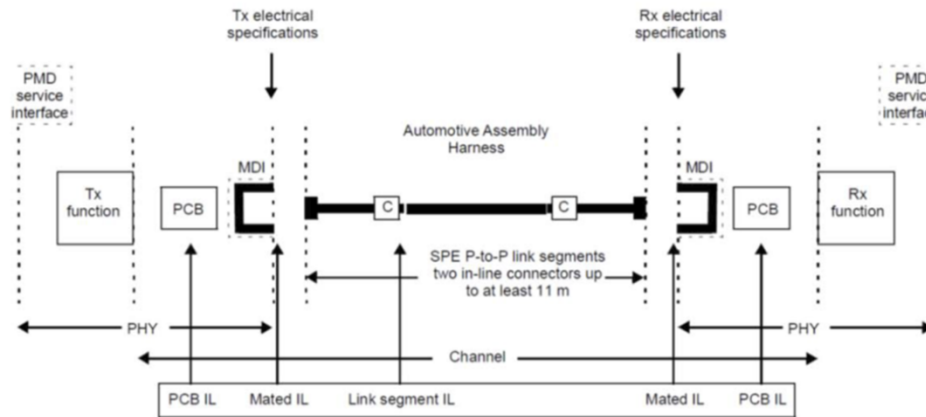
XXX.XX PMA electrical specifications

- Link Segment
 - Insertion Loss(f)
 - Return Loss(f)
- Link Segment Parameters Specified with Test Fixtures

Annex XXX (informative) Tx Function to Rx function channel characteristics

Proposal for Annex XXX (informative) Tx Function to Rx function channel characteristics

Tx Function to Rx function channel IL proposal



$$IL_{Channel} (dB) \leq 2 \cdot IL_{PCB} + 2 \cdot IL_{MDI} + IL_{Linksegment}$$

$$IL_{PCB}(dB) \leq 0.09144 \left(\frac{f_{MHz}}{1000} \right) + 0.51054 \left(\frac{f_{MHz}}{1000} \right)^{0.45}$$

$$IL_{LinkSegment}(dB) \leq 0.00135(f_{MHz}) + 0.3564(f_{MHz})^{0.45} + 0.495 \left(\frac{f_{MHz}}{7500} \right)^6$$

$$IL_{MDI}(dB) \leq 0.1 \sqrt{\frac{f_{MHz}}{2500}}$$

PHY	MBd	Bandwidth (MHz)	IL PCB	IL Link Segment	IL MDI	IL Channel
25GBASE-T1	14062.25	7031.25	1.871	29.02	0.168	33.098

Motions

**Move to adopt test point definitions and test fixture specifications slide 6-7
diminico_kadry_3cy_0a1_9_28_21.pdf with editorial license.**

M: Natalie Wienckowski

S: Haysam Kadry

Y:

N:

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**Move to adopt link segment specifications with adopted test fixtures slide 8
diminico_kadry_3cy_01a_9_28_21.pdf with editorial license.**

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**Move to adopt Annex XXX (informative) Tx Function to Rx function channel characteristics
Slide 9 diminico_kadry_3cy_01a_9_28_21.pdf with editorial license.**

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