



# 50 Gb/s demonstration in extreme temperatures using 850nm VCSELs

---

Rubén Pérez-Aranda, KDPOF

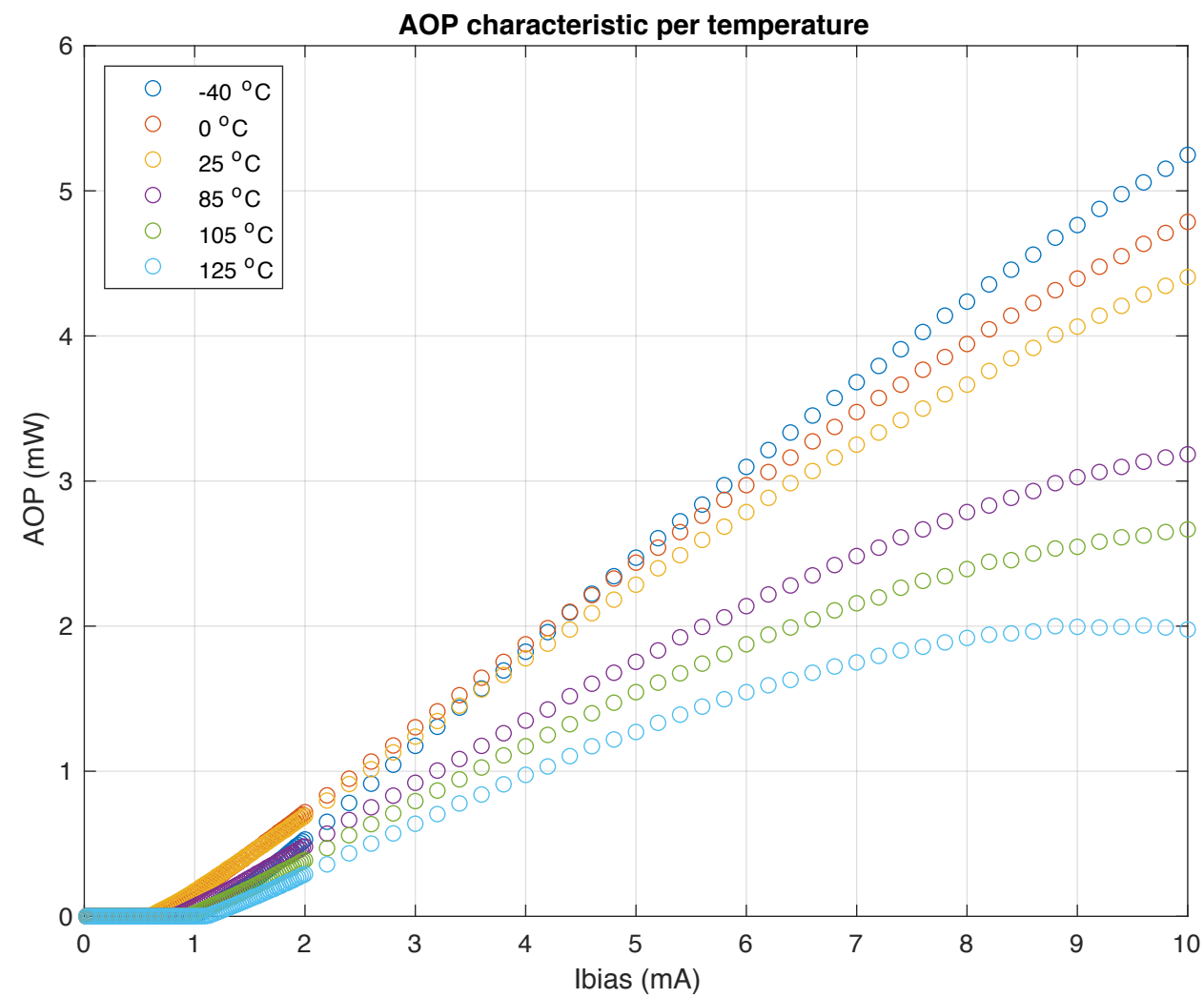
# Introduction and objectives

- A new 850nm VCSEL designed by TRUMPF for 25 Gb/s NRZ transmission was characterized according to the methodology reported in [1] and used for 50 Gb/s PAM4 real-time transmissions
- In order to build a technical feasibility assessment with margin, operation with low current densities of less than 13 kA/cm<sup>2</sup> in high temperature experiments has been demonstrated, with margin with respect to the maximum 15 kA/cm<sup>2</sup> considered in [2]
- It is demonstrated that 50 Gb/s is feasible in extreme temperatures using PAM4 modulation scheme, even using a VCSEL not designed for that aim, when the proper transmitter and receiver are used (i.e. TX FFE, RX timing-recovery & equalization, etc)
- These experiments will be the base for a 50 Gb/s PCS/PMA baseline proposal as well as for a first 50 Gb/s link budget assessment that demonstrate that a PMD based on VCSEL + OM3 is able to fulfill 100% of the project's objectives
- **Nevertheless**, in the short term, characterization, reliability data, real-time transmission experiments, as well as link budget assessments will be provided for **longer wavelength VCSEL** devices able to operate even faster and with better reliability in high temperatures, therefore allowing **lower power consumption and lower complexity** transceiver implementations (i.e. reduced DSP requirements like lower TX FFE gain and smaller RX equalizer computational complexity)

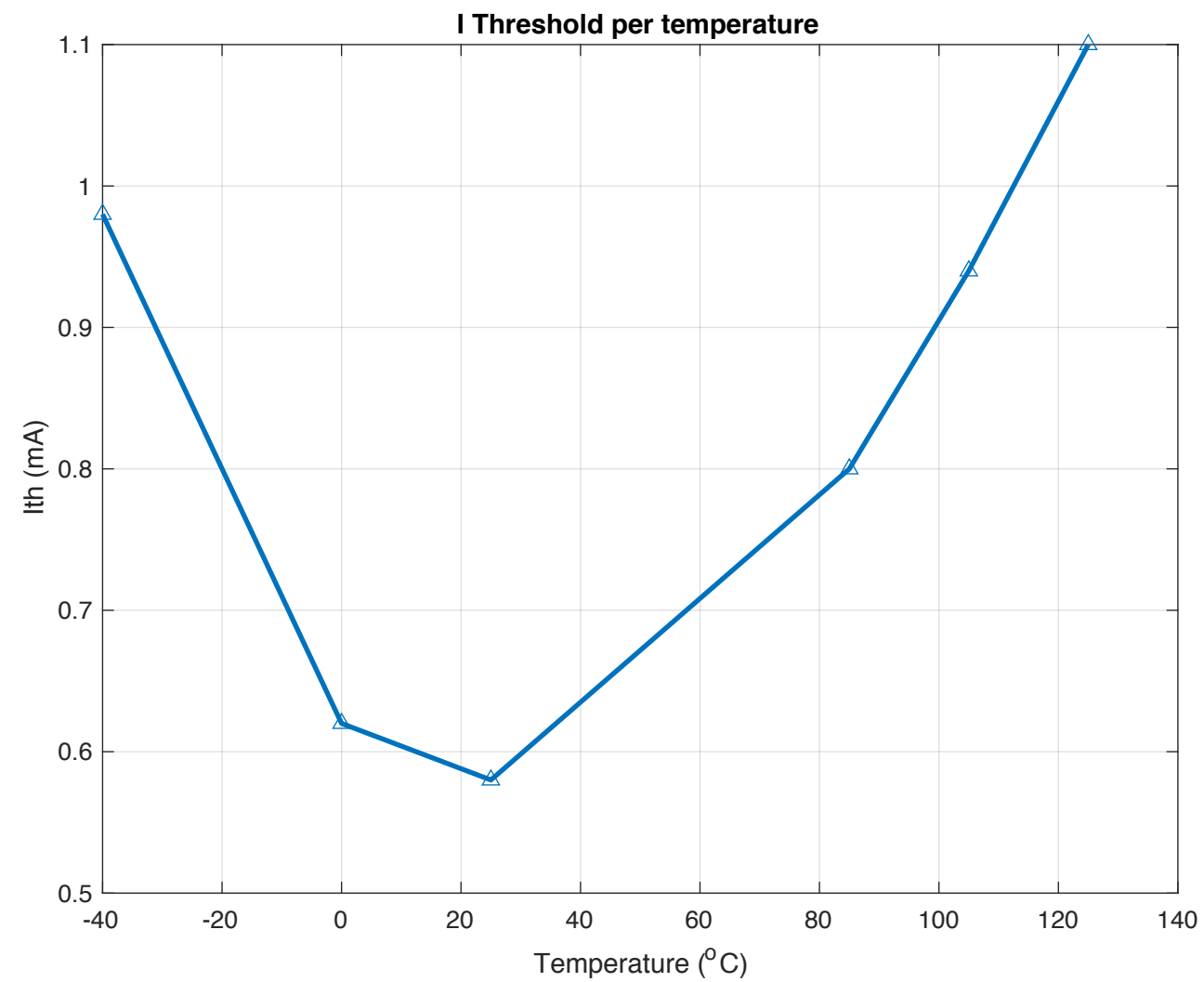


# Characterization of ULM850-25-TT-W0101U 25 Gbps NRZ VCSEL

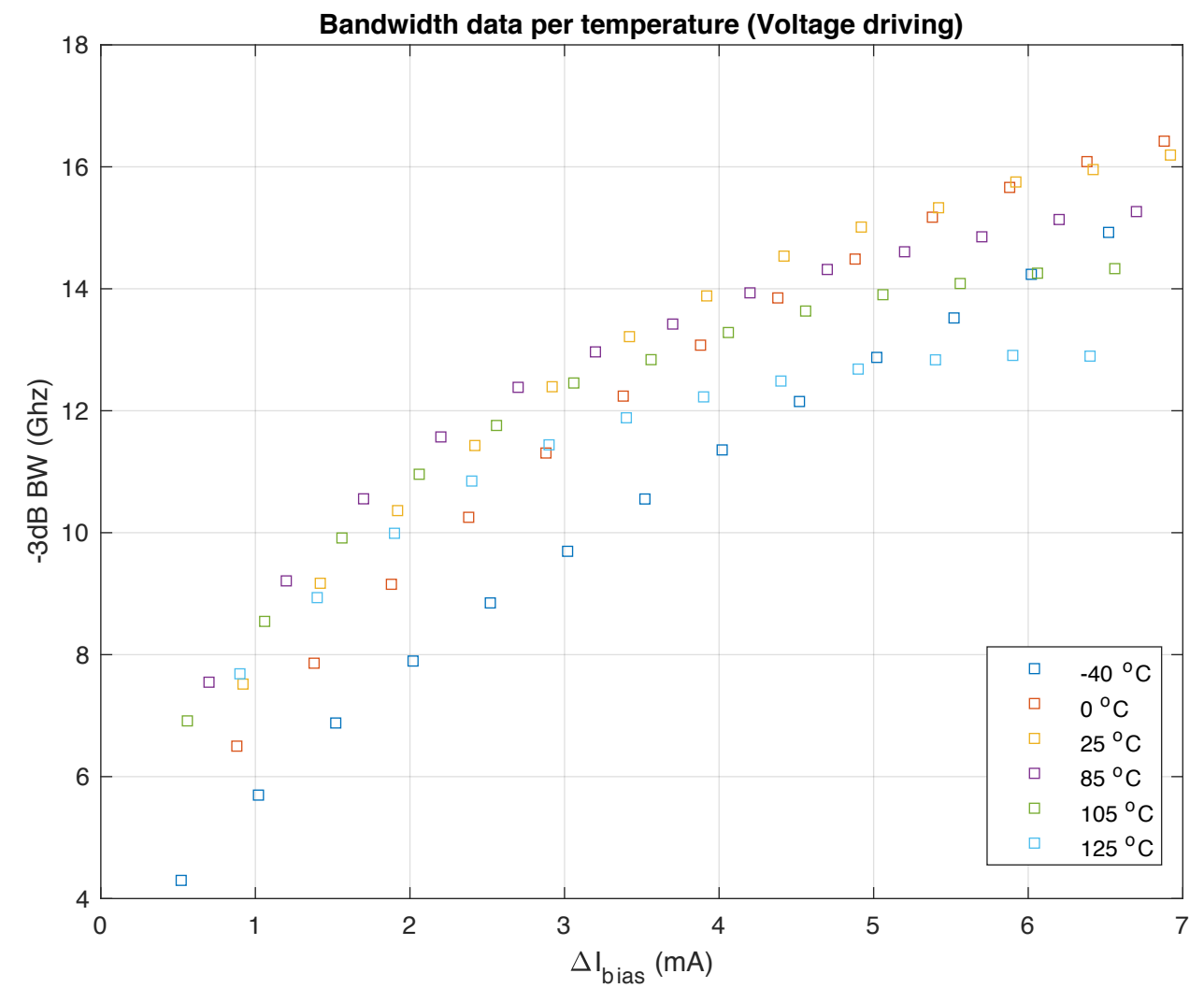
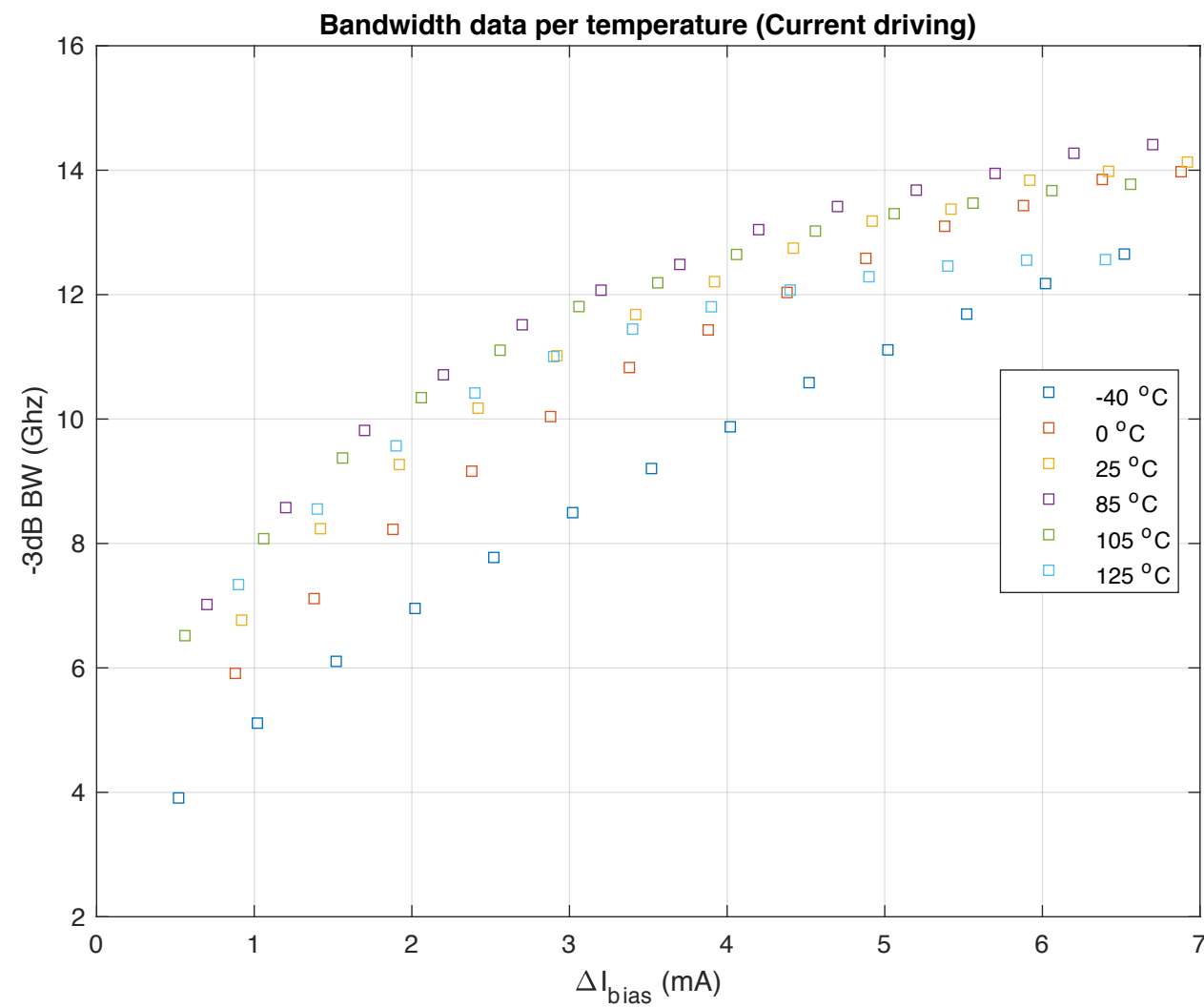
# L-I characteristic



# Threshold current characteristic

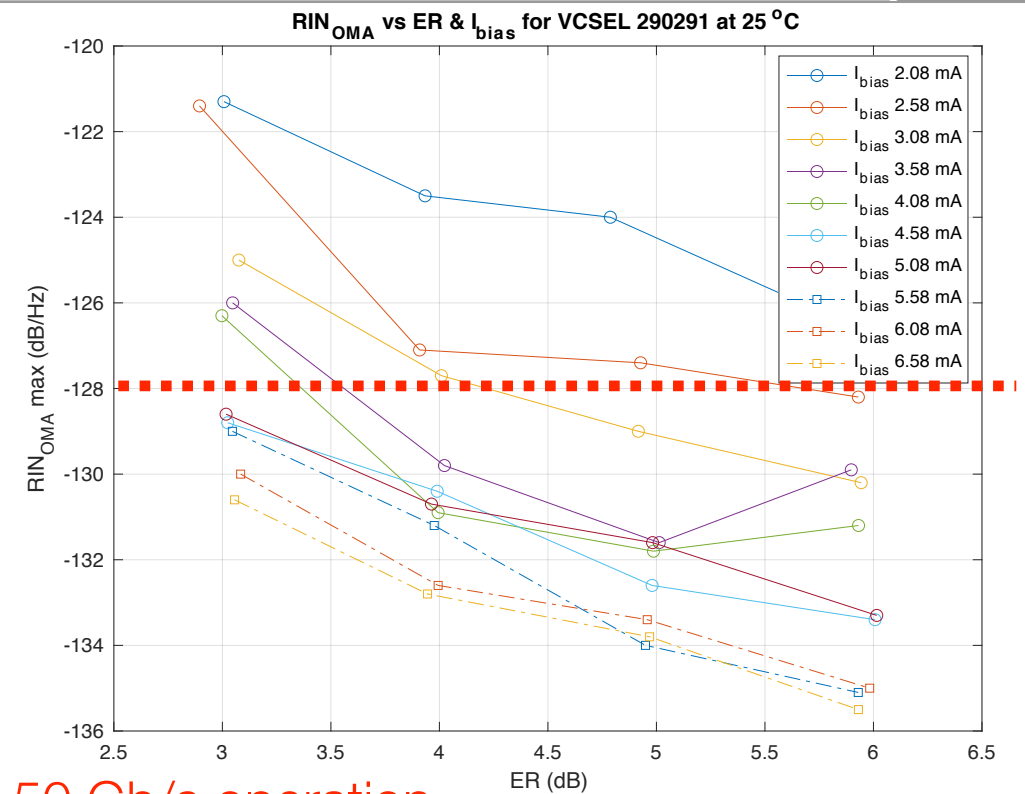
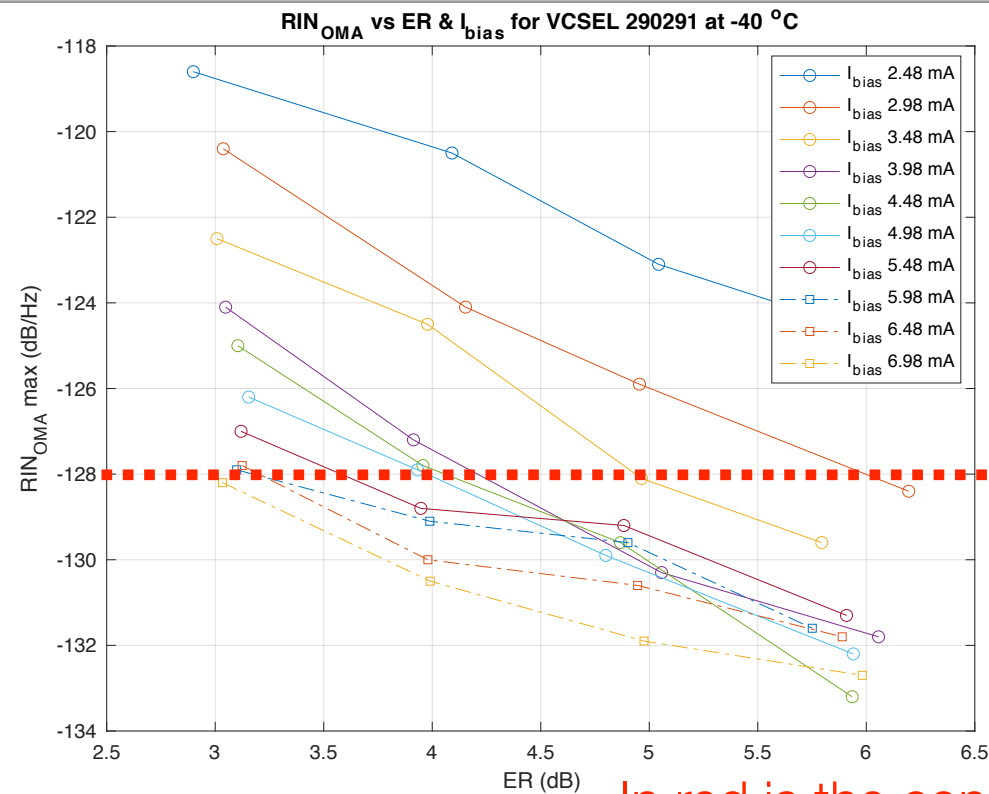


# Small signal frequency response

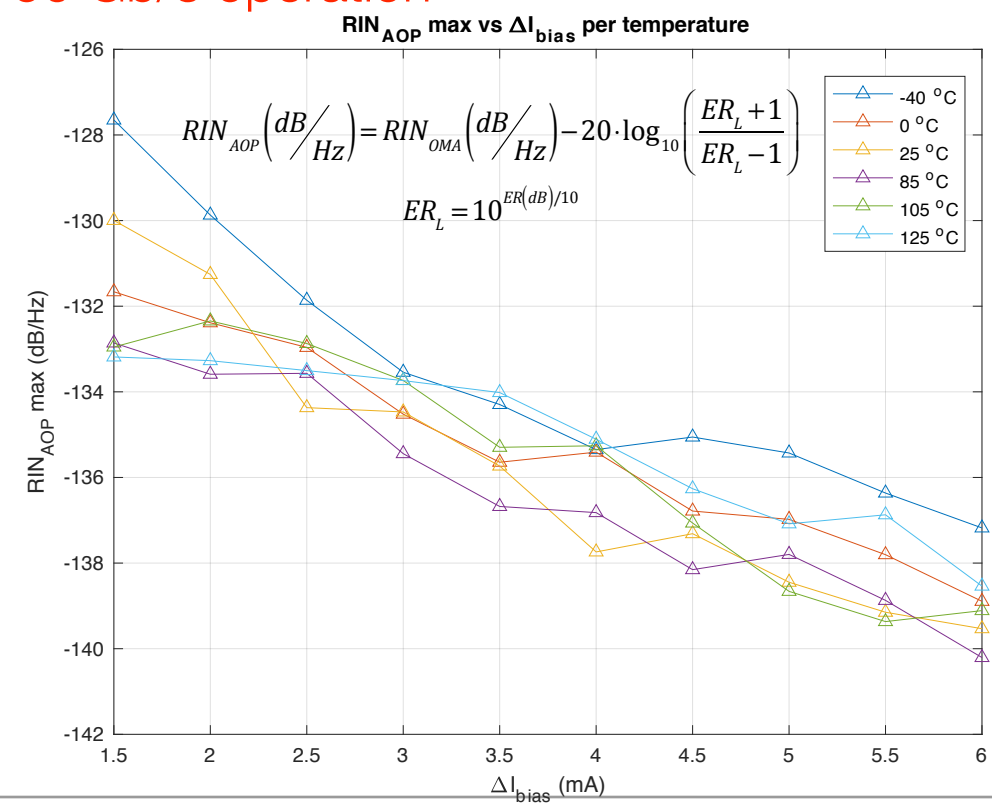
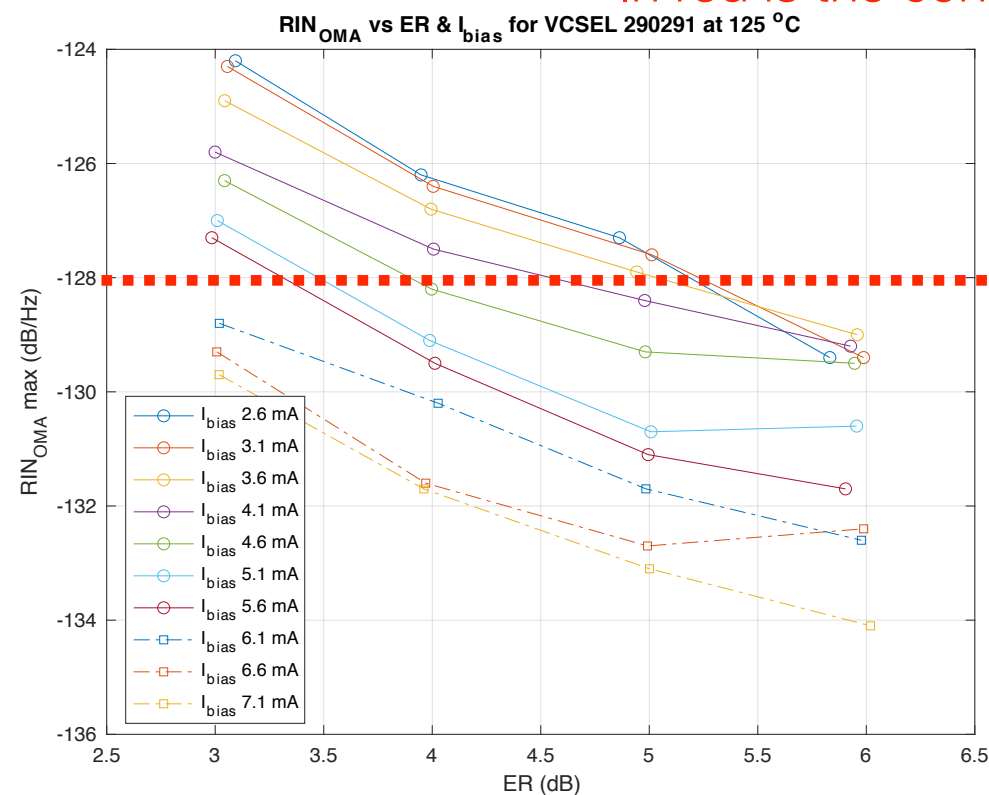


Considered source impedance 100  $\Omega$

# Relative intensity noise (RIN<sub>OMA</sub>)



In red is the considered limit for 50 Gb/s operation





# Real-time transmission setup

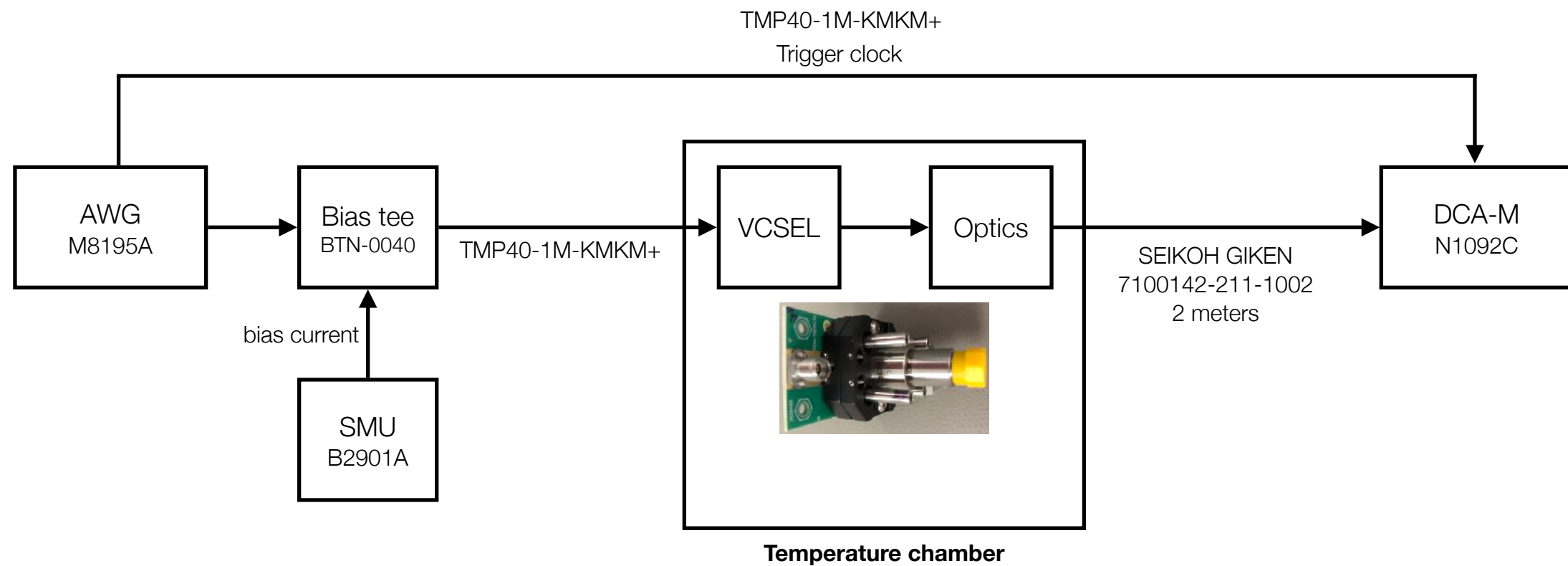


# Equipment & Software



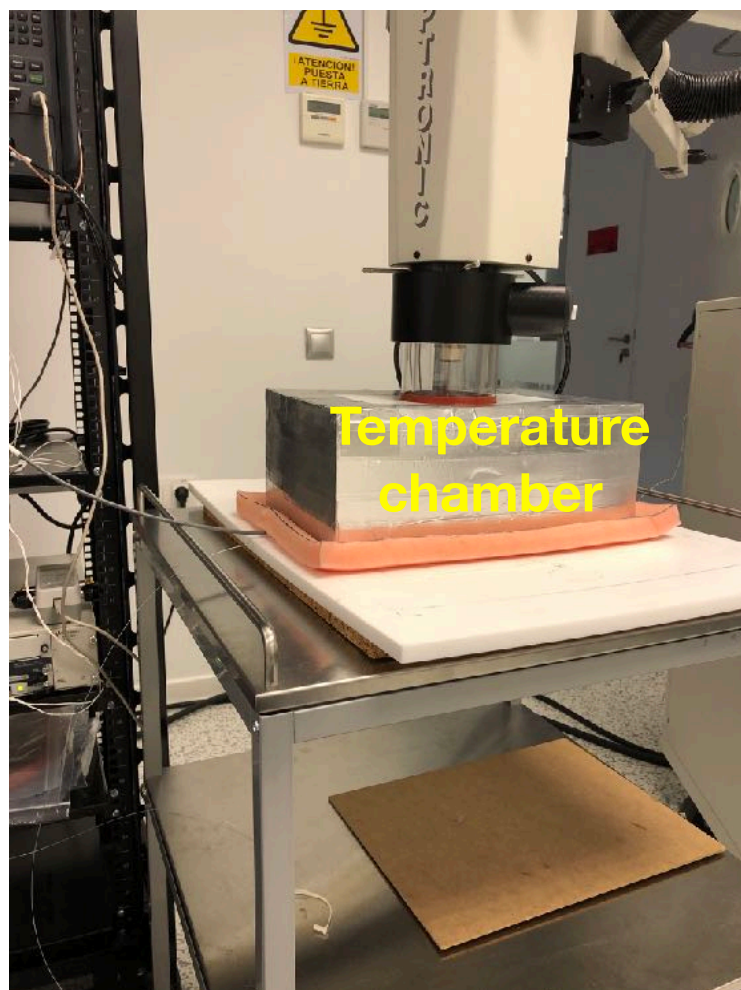
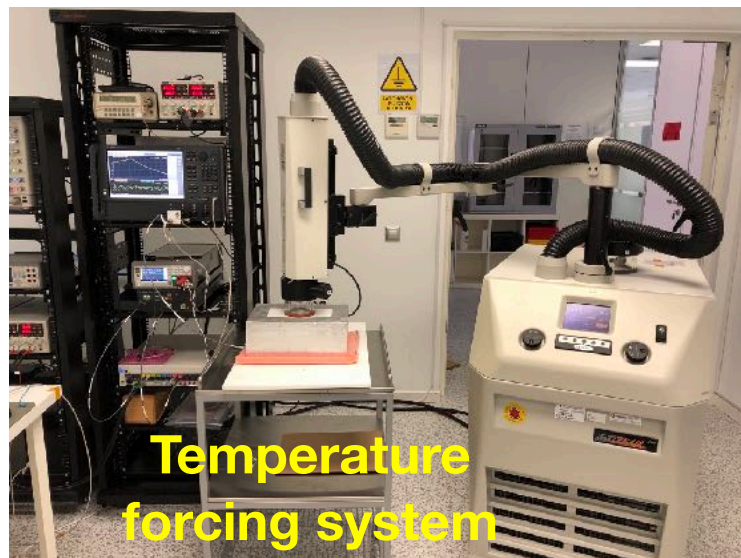
1. Amphenol SVmicrowave SF1521-60115, 2.92mm female solderless LiteTouch PCB Connector, 2 Hole (CPW / Microstrip)
  - Coaxial to CPWG transition used to connect the coax cable to the PCB where the VCSEL is assembled
2. Marki Microwave BTN-0040 bias tee (40 kHz to 40 GHz)
  - Used to combine bias current with RF signal from VNA or AWG
3. Minicircuits TMP40-1M-KMKM+, temperature stable 2.92mm cable, 40.0 GHz
  - Used to connect bias tee output to the DUT
  - Used to provide trigger clock from AWG to DCA
4. Keysight B2901A Precision Source/Measure Unit
  - Bias current to VCSEL
  - Voltage drop measurement (V-I curve)
5. SEIKOH GIKEN 7100142-211-1002 APC to PC,MM, SX, OM3, 3mm, 2 meters
  - Used to connect the DUT to the measurement equipments: O/E converters and DCA
- APC is used in the DUT side to reduce back reflection effect
6. Keysight M8195A 65 GSa/s, 25 GHz, Arbitrary Waveform Generator
  - Used to generate time-domain RF signal that drives the VCSEL
  - Capability of real-time digital signal processing with 8 bits DAC
  - One port used to provide symbol clock to DCA
7. Keysight N1092C DCA-M Sampling Oscilloscope (one optical and two electrical channels)
  - Used to make the time-domain characterization with periodic arbitrary signal generated by VCSEL
  - Background noise calibrated for RIN measurement
8. Keysight N1010A FlexDCA Sampling Oscilloscope Software R&D software package
9. Matlab 2019b:
  - Test automation
  - Signal processing
  - Model extraction

# Test setup





# Tests setup

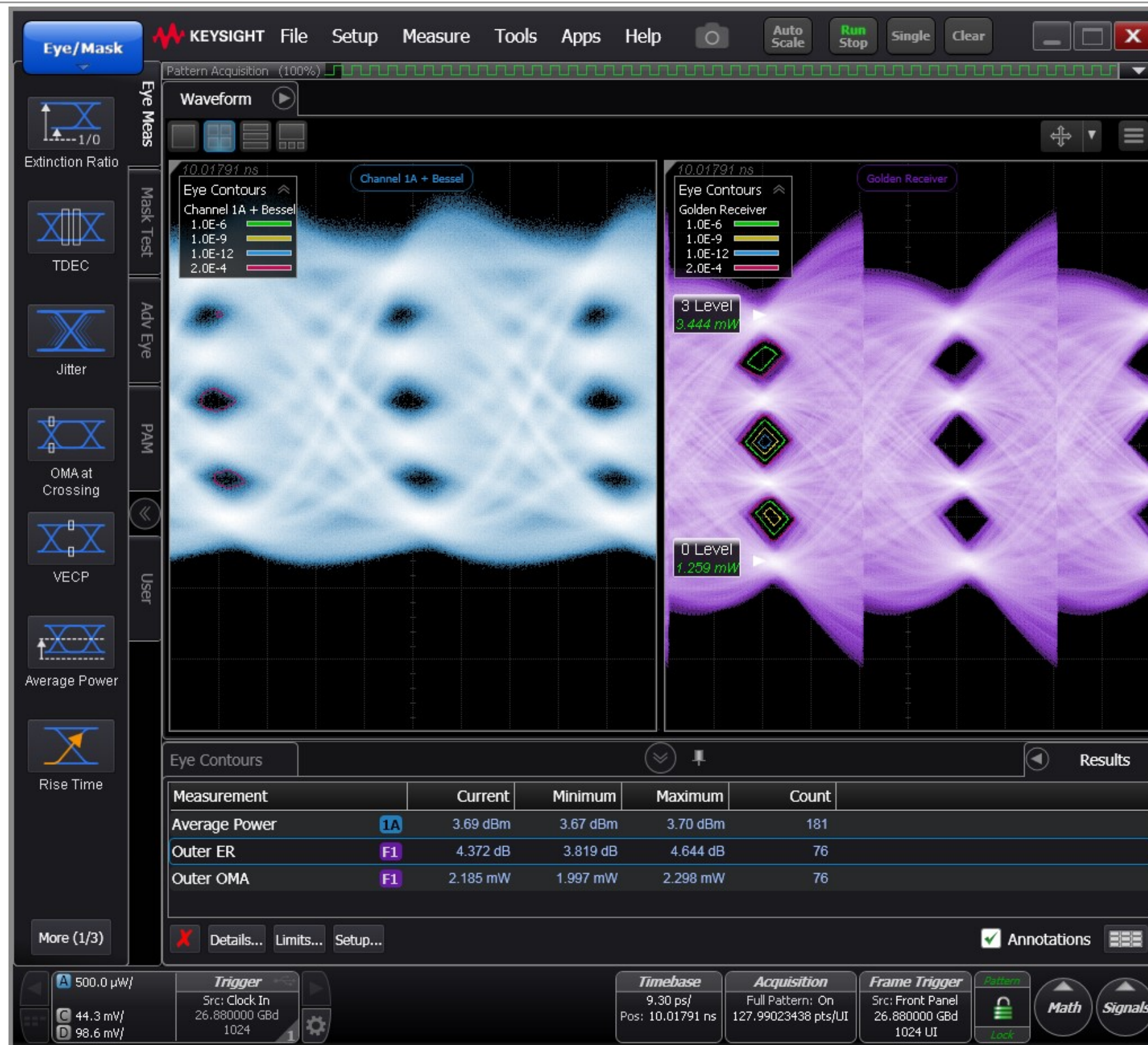




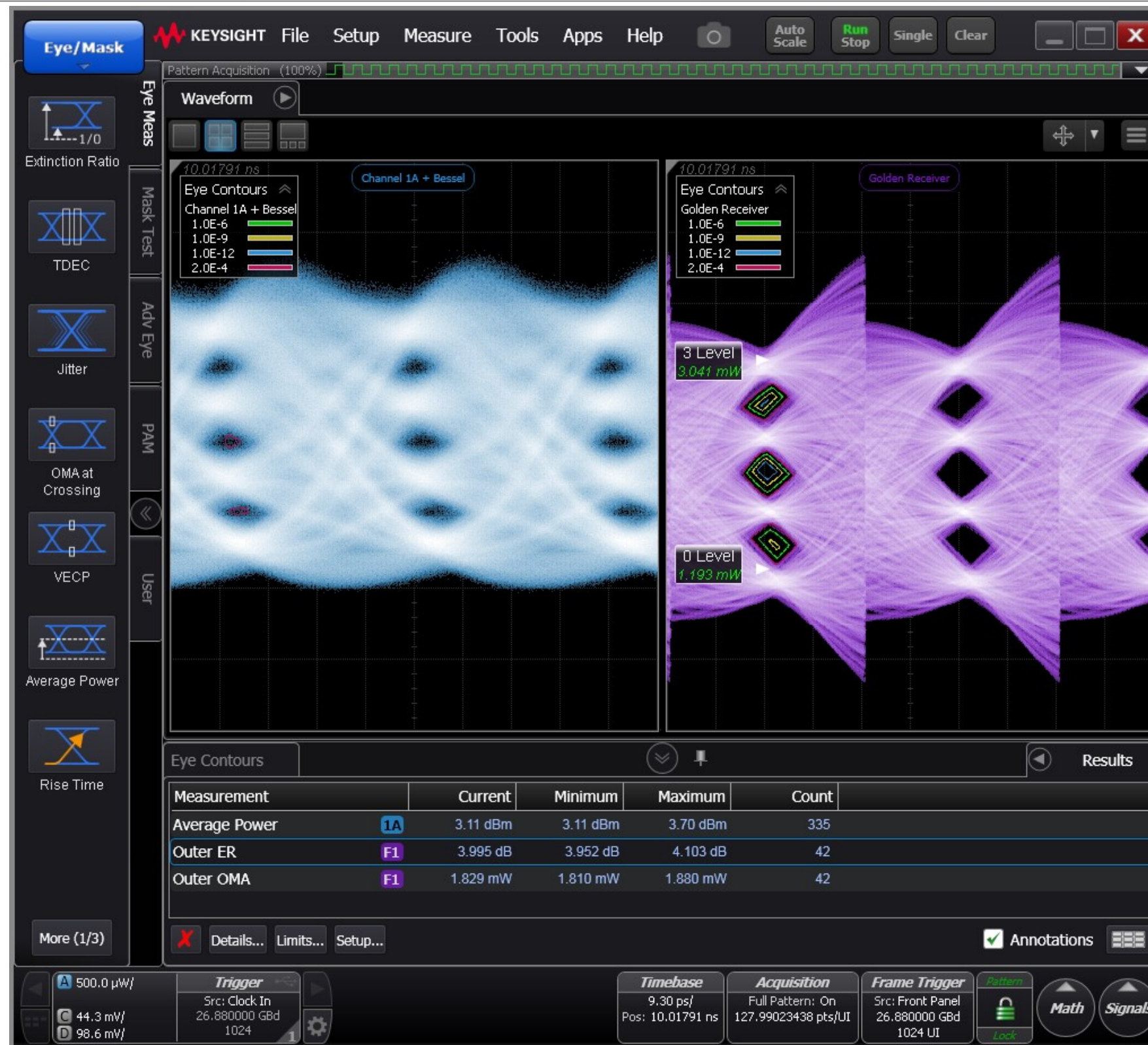
# Real-time performance at 25°C



# 25°C, 53.76 Gb/s PAM4, Ibias 7mA, ER 4 dB



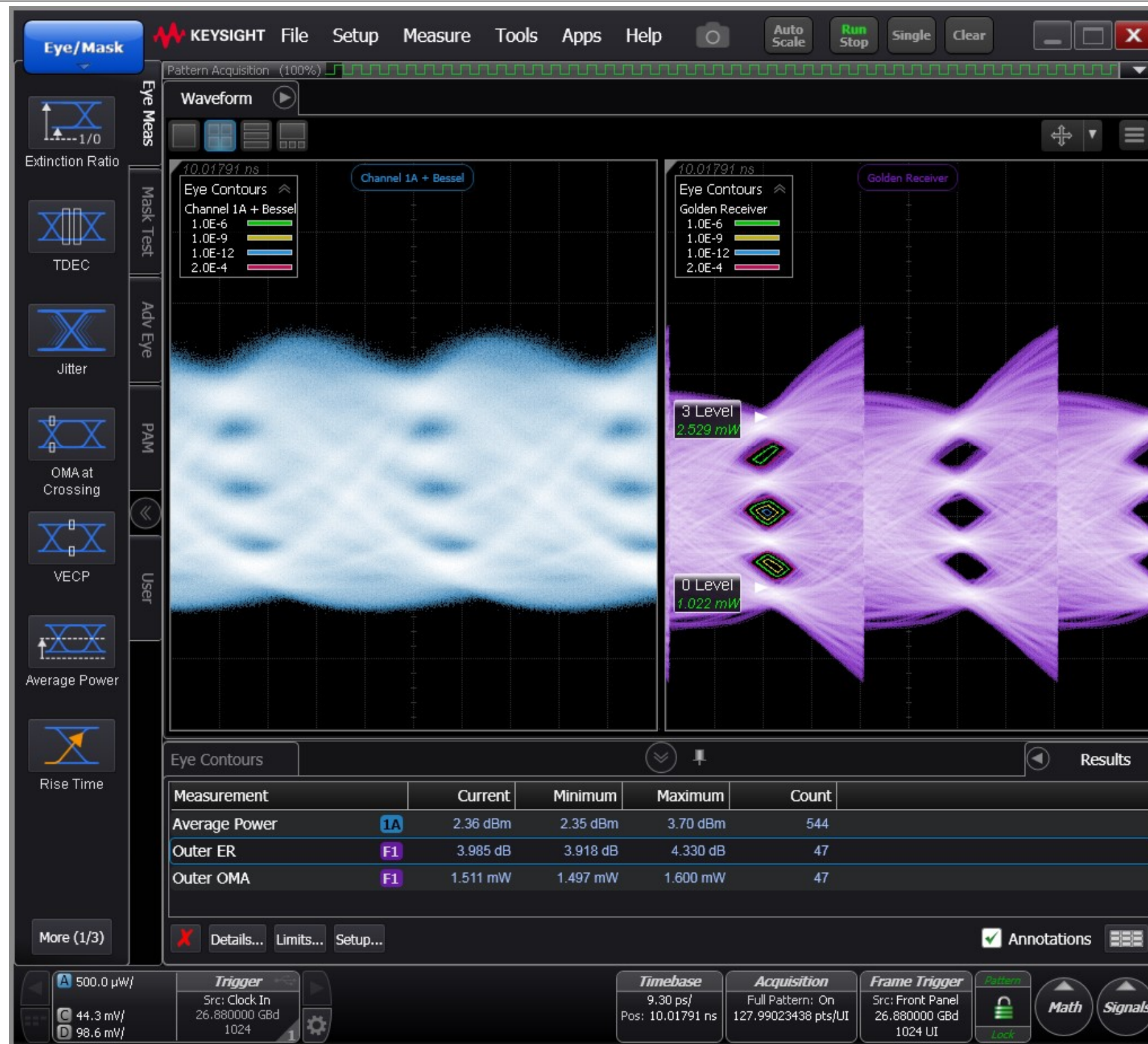
# 25°C, 53.76 Gb/s PAM4, I<sub>bias</sub> 6mA, ER 4 dB





# 25°C, 53.76 Gb/s PAM4, I<sub>bias</sub> 5mA, ER 4 dB

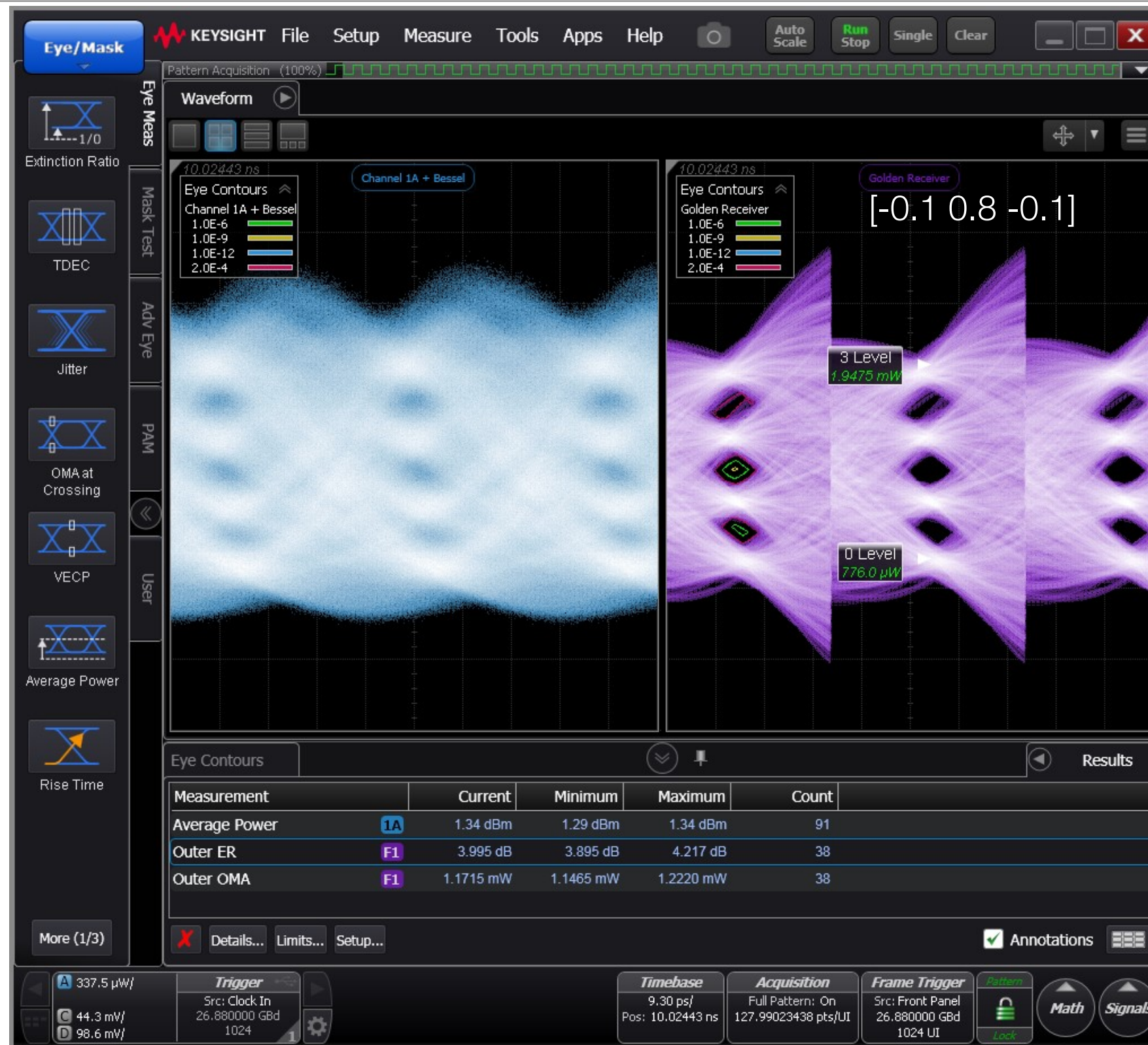
< 13 kA/cm<sup>2</sup>



25°C, 53.76 Gb/s PAM4, 3-tap TX FFE, I<sub>bias</sub> 4mA, ER 4 dB



< 13 kA/cm<sup>2</sup>

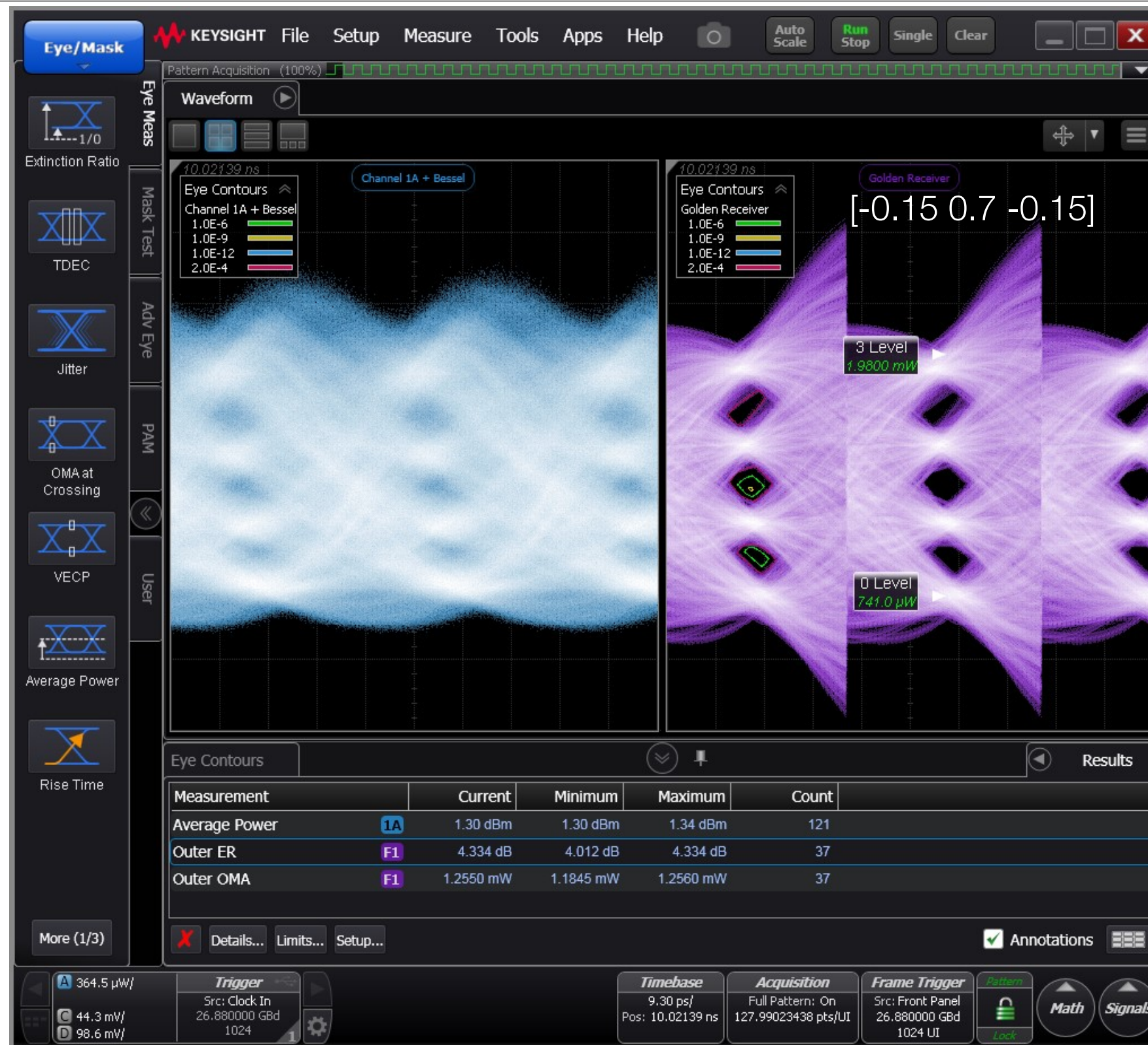




25°C, 53.76 Gb/s PAM4, 3-tap TX FFE, I<sub>bias</sub> 4mA, ER 4 dB



< 13 kA/cm<sup>2</sup>





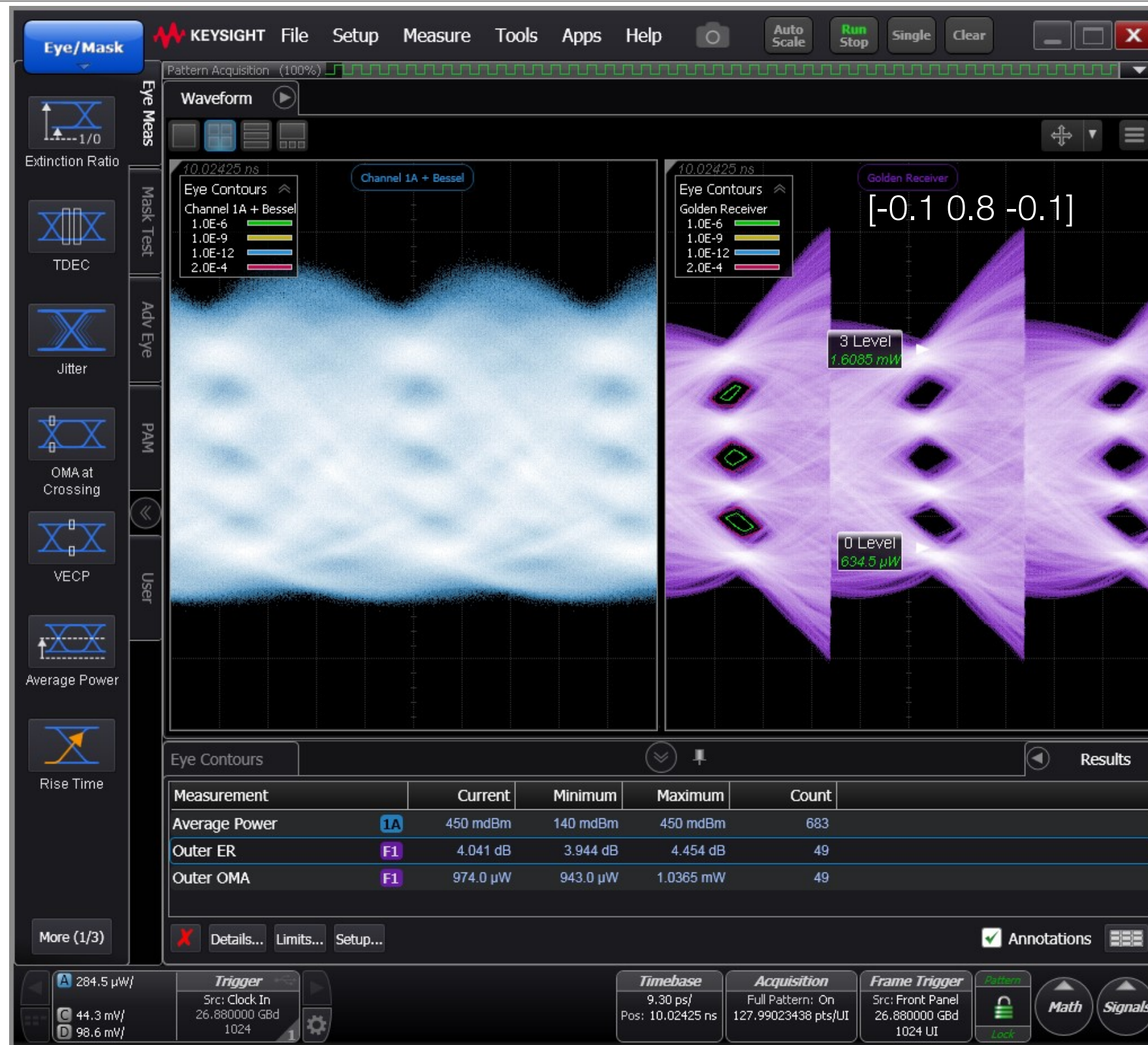
# Real-time performance at 125°C



# 125°C, 53.76 Gb/s PAM4, Ibias 6mA, ER 3 dB

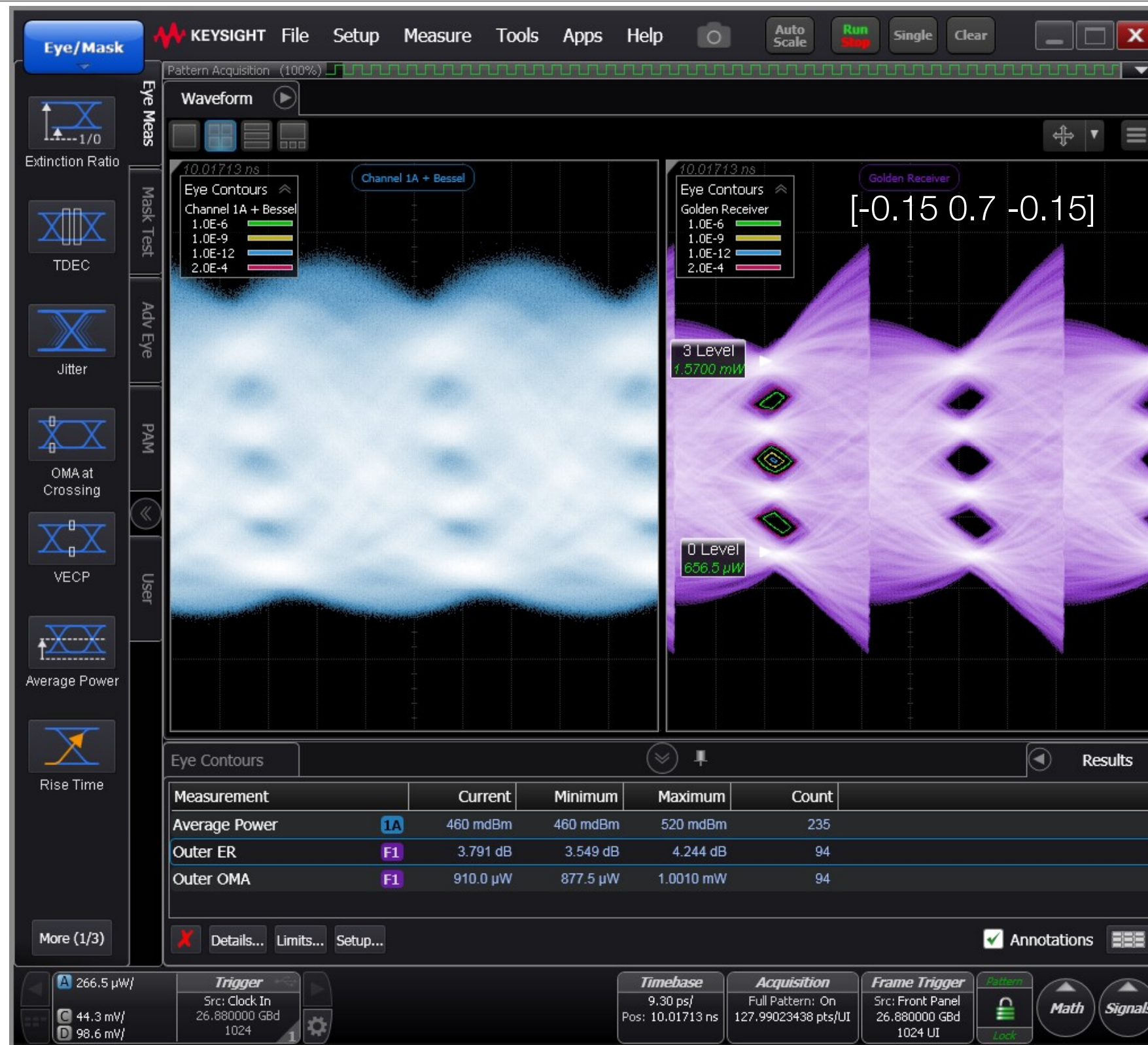


125°C, 53.76 Gb/s PAM4, 3-tap TX FFE, I<sub>bias</sub> 6mA, ER 4 dB





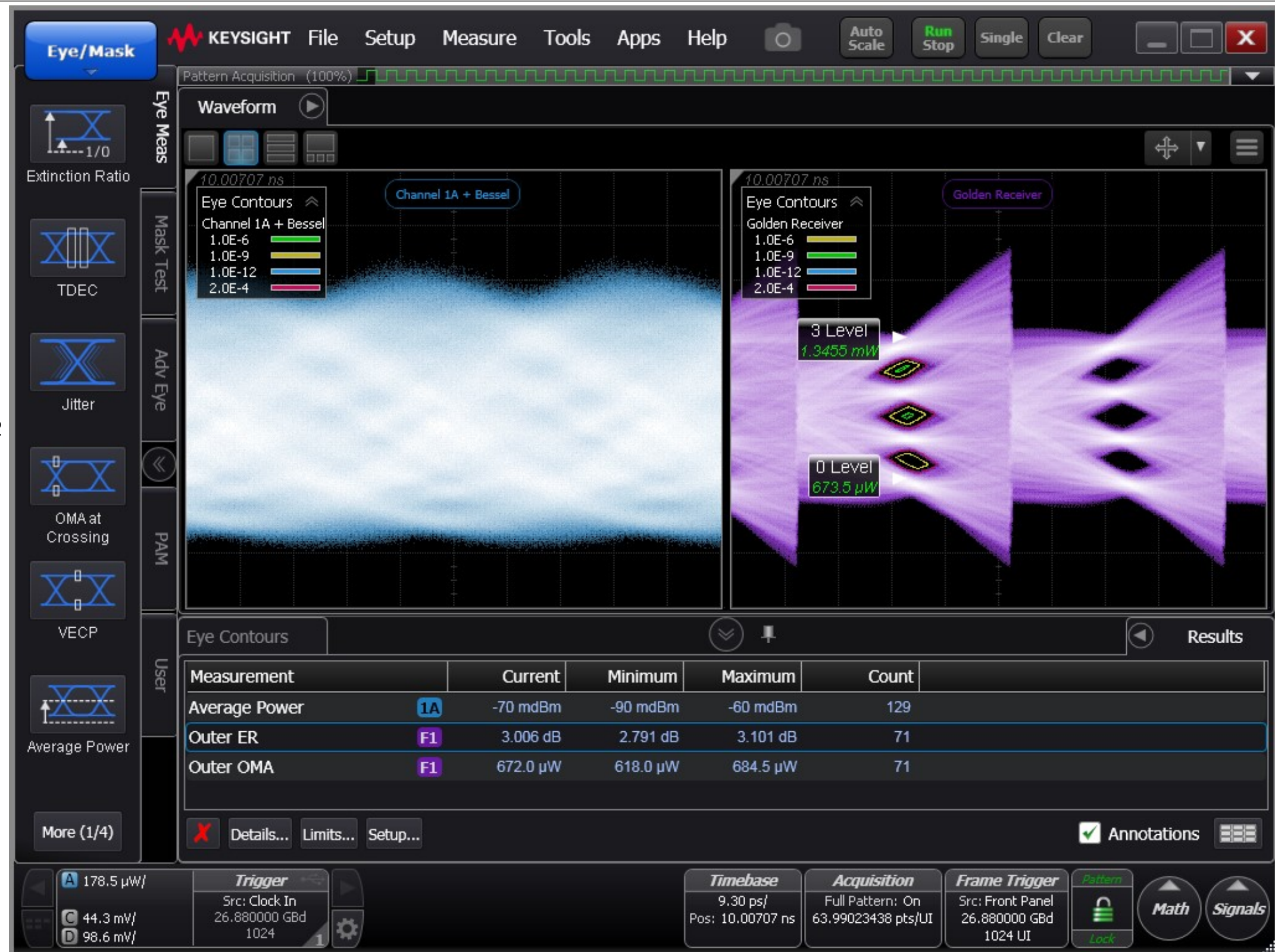
125°C, 53.76 Gb/s PAM4, 3-tap TX FFE, Ibias 6mA, ER 4 dB



# 125°C, 53.76 Gb/s PAM4, I<sub>bias</sub> 5mA, ER 3 dB



< 13 kA/cm<sup>2</sup>

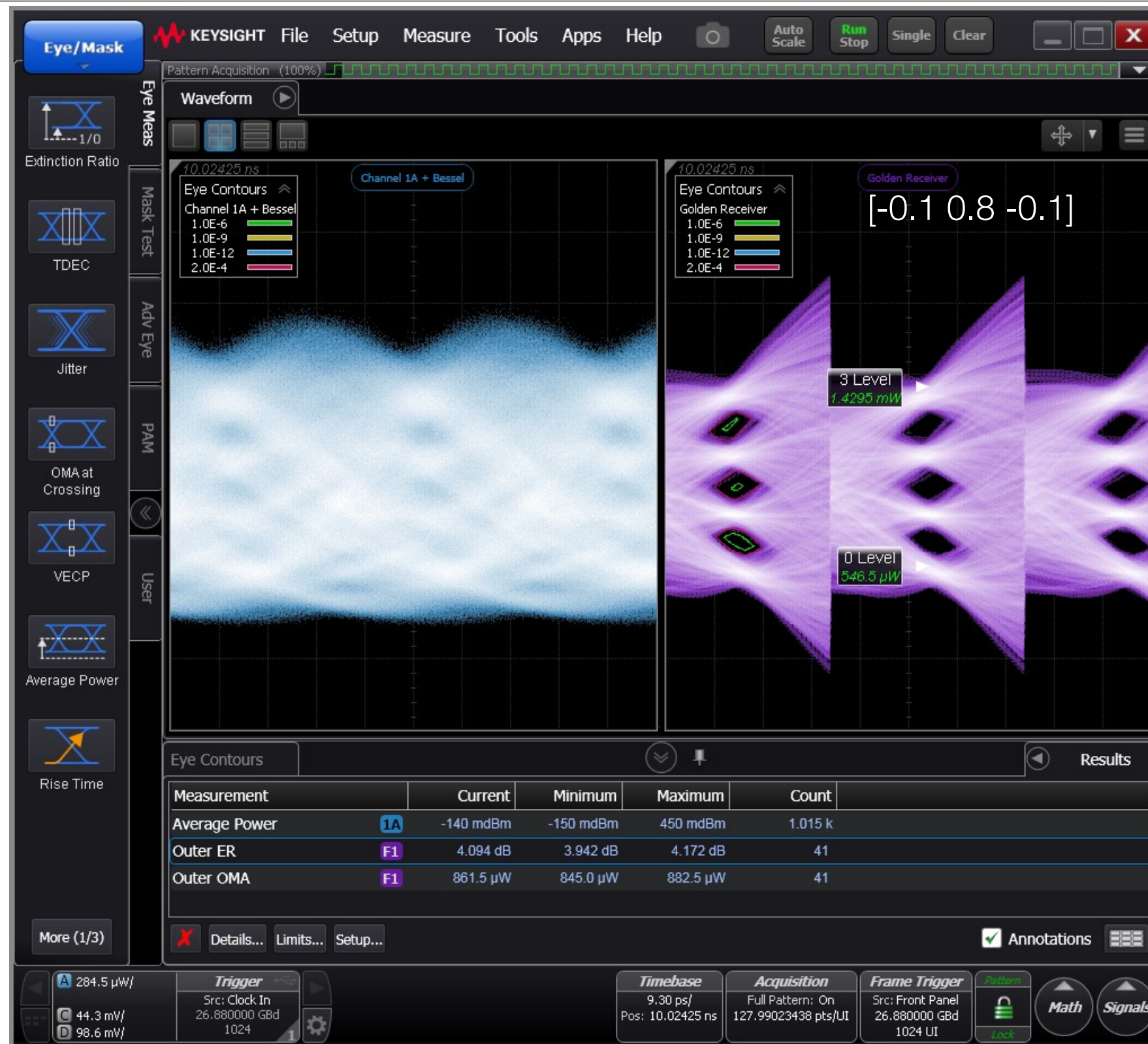




125°C, 53.76 Gb/s PAM4, 3-tap TX FFE, I<sub>bias</sub> 5mA, ER 4 dB

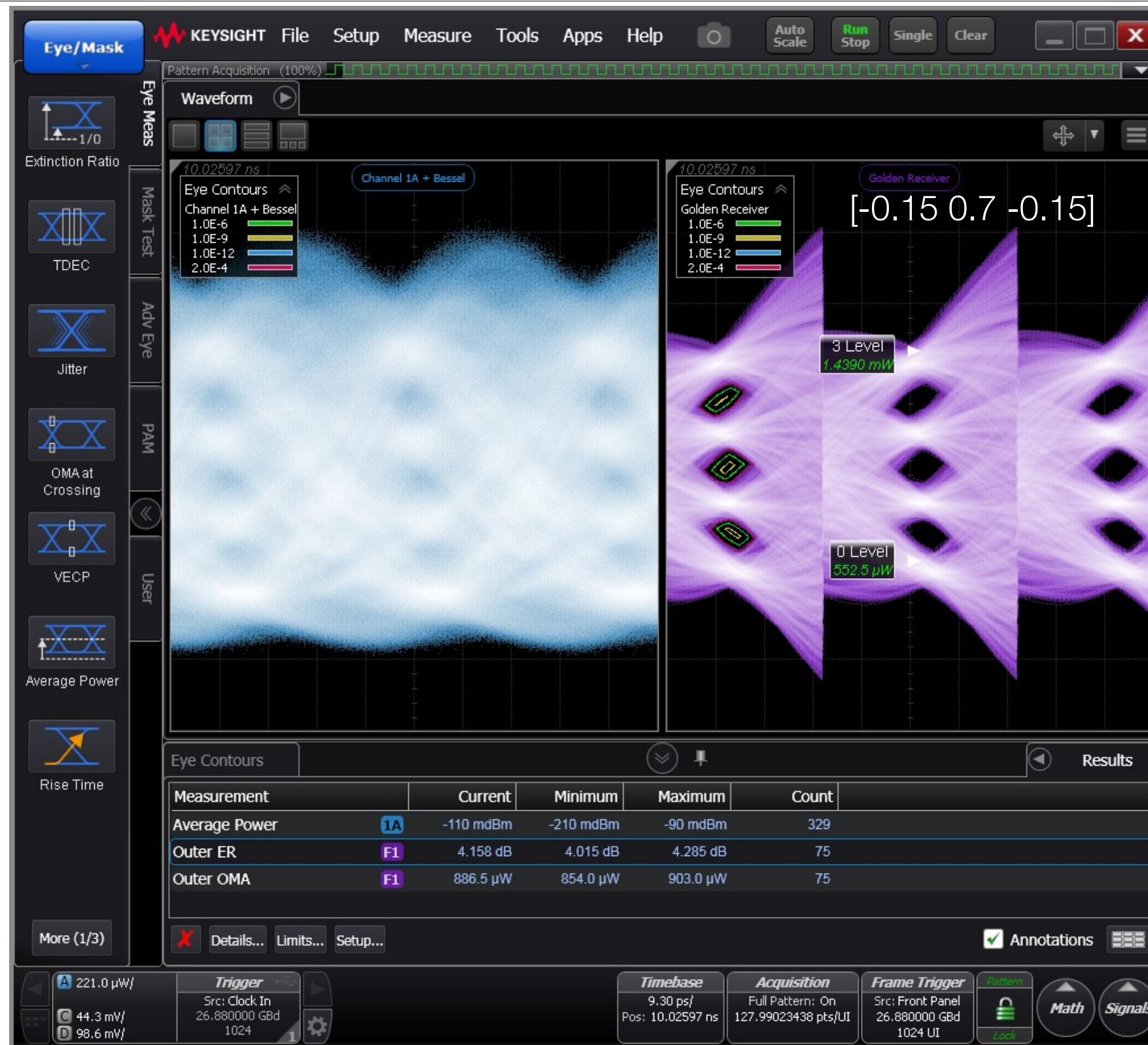


< 13 kA/cm<sup>2</sup>



125°C, 53.76 Gb/s PAM4, 3-tap TX FFE, I<sub>bias</sub> 5mA, ER 4 dB

< 13 kA/cm<sup>2</sup>

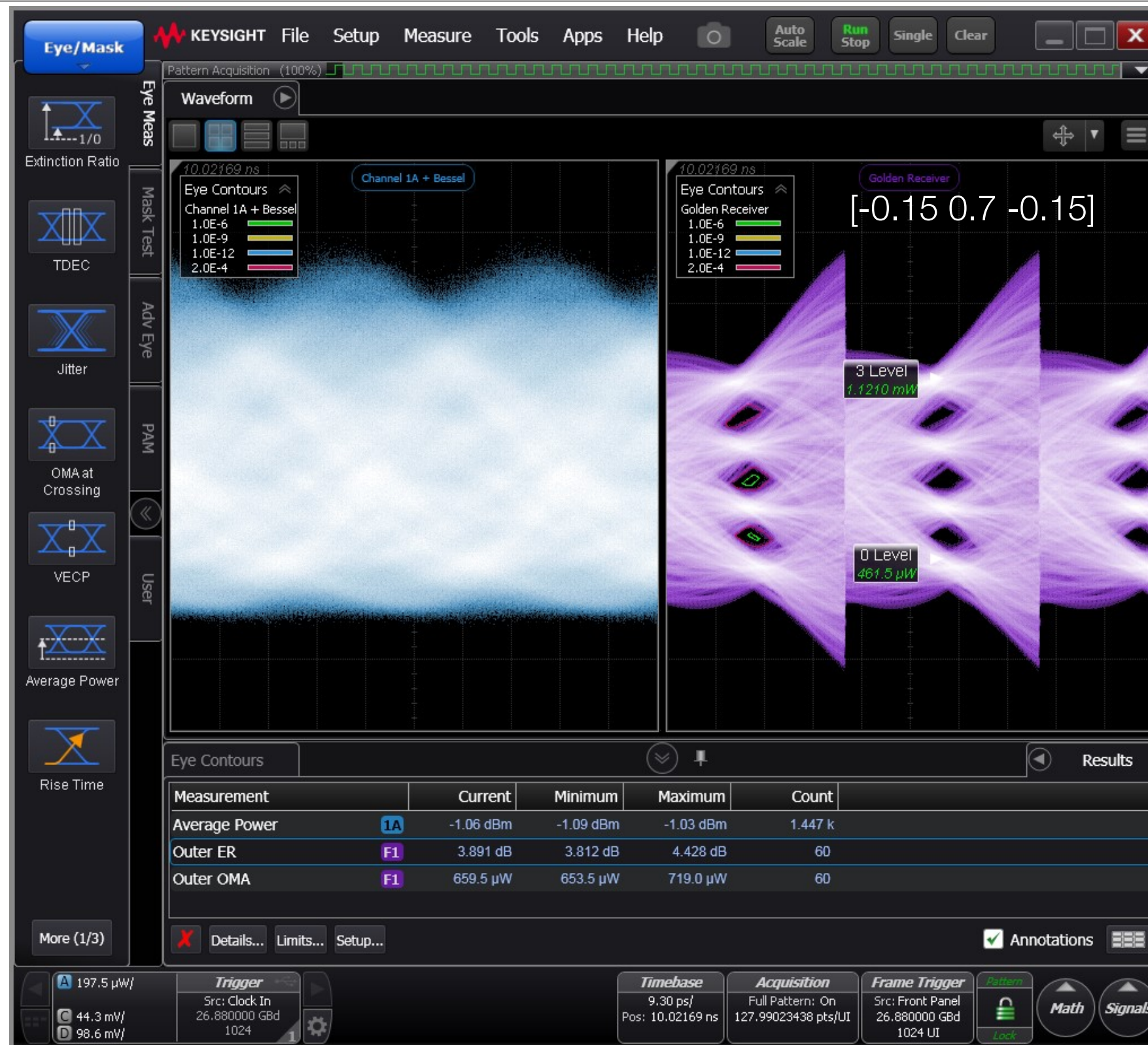




125°C, 53.76 Gb/s PAM4, 3-tap TX FFE, Ibias 4mA, ER 4 dB



< 13 kA/cm<sup>2</sup>





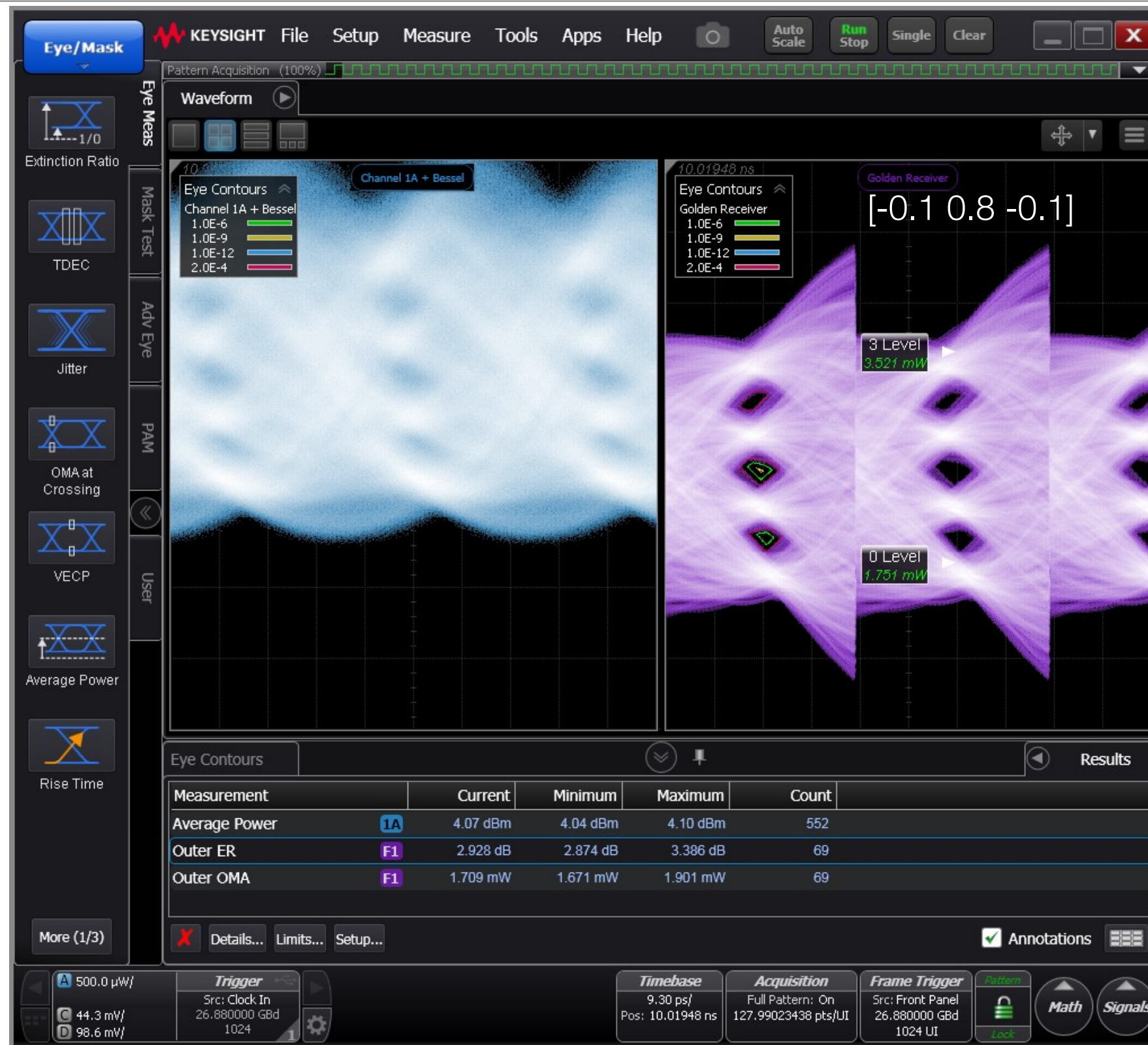
# Real-time performance at -40°C

-40°C, 53.76 Gb/s PAM4, I<sub>bias</sub> 7mA, ER 3 dB





-40°C, 53.76 Gb/s PAM4, 3-tap TX FFE, I<sub>bias</sub> 7mA, ER 3 dB



-40°C, 53.76 Gb/s PAM4, 3-tap TX FFE, I<sub>bias</sub> 7mA, ER 2 dB





# Conclusions



- A new 850nm VCSEL designed by TRUMPF for 25 Gb/s NRZ transmission was characterized according to the methodology reported in [1] and used for 50 Gb/s PAM4 real-time transmissions
- It was demonstrated that 50 Gb/s is feasible in extreme temperatures using PAM4 modulation scheme, even using a VCSEL not designed for that aim, when the proper transmitter and receiver are used (i.e. TX FFE, RX timing-recovery & equalization, etc)
- **Nevertheless**, in the short term, characterization, reliability data, real-time transmission experiments, as well as link budget assessments will be provided for **longer wavelength VCSEL** devices able to operate even faster and with better reliability in high temperatures, therefore allowing **lower power consumption and lower complexity** transceiver implementations (i.e. reduced DSP requirements like lower TX FFE gain and smaller RX equalizer computational complexity)

# References

---



- [1] R. Pérez-Aranda, “Test methods for VCSEL characterization,” July 2020, [Online], Available: [https://www.ieee802.org/3/cz/public/jul\\_2020/perezaranda\\_OMEGA\\_01b\\_0720\\_VCSEL\\_test\\_methods.pdf](https://www.ieee802.org/3/cz/public/jul_2020/perezaranda_OMEGA_01b_0720_VCSEL_test_methods.pdf)
- [2] R. Pérez-Aranda, “Reliability constrained link budget assessment for 25 and 10 Gb/s,” Dec 2020, [Online], Available: [https://www.ieee802.org/3/cz/public/22\\_dec\\_2020/perezaranda\\_3cz\\_02a\\_221220\\_reliability\\_linkbdget.pdf](https://www.ieee802.org/3/cz/public/22_dec_2020/perezaranda_3cz_02a_221220_reliability_linkbdget.pdf)



Thank you!