Remarks on Stream FEC for Ethernet

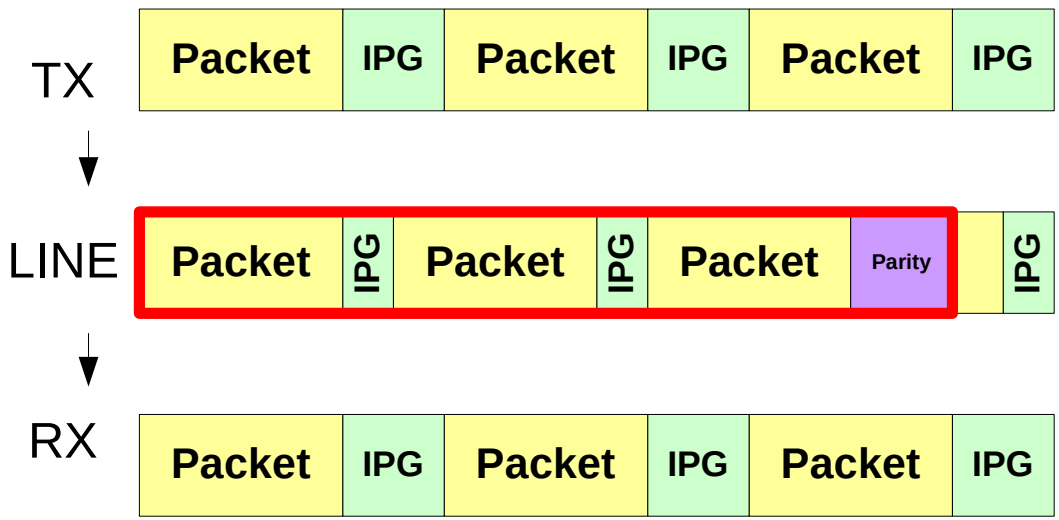
No Compliance to 1000Base-X in S-FEC

Rate Adaptation

- Rate adaptation for S-FEC is highly complicated
  - 10G rate adaptation uses frame based extensions (IPG stretching)
    - FEC Tx layer needs to remove added IPG
    - FEC Rx layer needs to add Idles to IPG
  - S-FEC layer is frame aware!
    - S-FEC layer would need to detect packet boundaries and need to convert IPG time to parity time with a very wide decision tree

IPG stretching

- Parity time is added only at the end of the frame. Need for additional buffer
  - (1530/191+1)*17= 153 bytes
- Need to detect packet boundaries to squeeze in Tx and stretch in RX, IPG between frame
  - A complex state machine is need to handle all cases



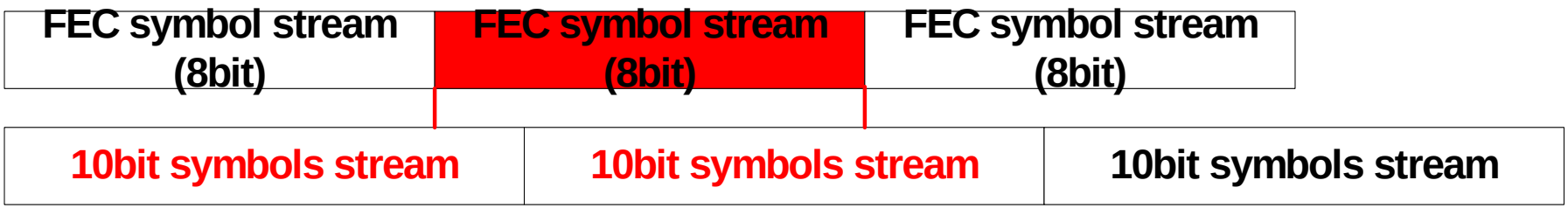
Increasing Line Rate

- The only way to match rate for a stream FEC is to increase the line rate.
  - New PMA!
  - New PMDs!
- When increasing the line rate, no negotiation is possible
  - How is FEC optional?

Errors Duplication, lower Burst Protection

- A single error over protected stream may be translated to two errors after detection

- Maximal error burst protection is decreased to 64 bits (from 80 bits in F-FEC)



Byte alignment in Rx

- FEC needs byte alignment for decoding
- Excess IDLE codes are removed/inserted from/to IPG
  - Byte alignment is performed in FEC layer since PMA aligns to 10 bits
  - A byte sync state machine similar to PCS performing COMMA synchronization is also required

Frame Synchronization

- 1 byte frame sync. symbol is not enough:
  - Very long acquisition time to achieve downlink lock
  - Very high probability of false-lock in uplink
- Crucial details are missing for baseline
  - What is the synchronization time in the uplink/downlink?
  - What is the probability of misdetection?
  - What is the state machine?

Rebuttal Comparison of FEC Proposals

	Stream- FEC (S- FEC)	Frame- FEC (F- FEC)	Comments
Backwards Compatibility	**No**	**Yes**	Are there any EPON transceivers out there today?
Overhead (computed at information rate)	**8% (independent of traffic)**	**14% (function of traffic)**	The MAC rate needs to be reduced correspondingly Not possible for S-FEC – need to increase line rate
Complexity	**Low** **Medium (Increase rate)** **High (Maintain rate)**	**Medium**	F- FEC layer is an enhanced PCS layer under existing PCS Layer. S-FEC requires a state machines of similar complexity
Protection	**Equal protection of all bits. Does not better protect sync symbols**	**Only MAC frames are protected**	
Upper layer Awareness	**Yes**	**Yes**	If Phy- rate is increased, S-FEC can be transparent to upper layers.
Delay due to FEC	**~416 bytes**	**~2389 bytes** **Actually 1522+7*16**	Jitter effects PON performance. Latency needs to be tightly controlled in F-FEC. Actually there is No Jitter. Same stretching must be used in S-FEC at both ends to avoid jitter
Prior field experience	**Proven (G. 975) only for increased rate case**	**Same New technology**	