### 61.0.0.1 Application and examples of PHY PMI Aggregation

The PHY PMI Aggregation Function defined in 61.2.2 allows multiple PMI interfaces to be aggregated together to form one logical link underneath one MII (or MAC). Additionally, the control mechanism allows multi-MAC devices to be built with flexible connections between the MACs and the PMIs. Clause 45 defines a mechanism for addressing and controlling this flexible connectivity. The relationship between the flexible connectivity and the other functions within the PCS is shown in Figure 61–1 .

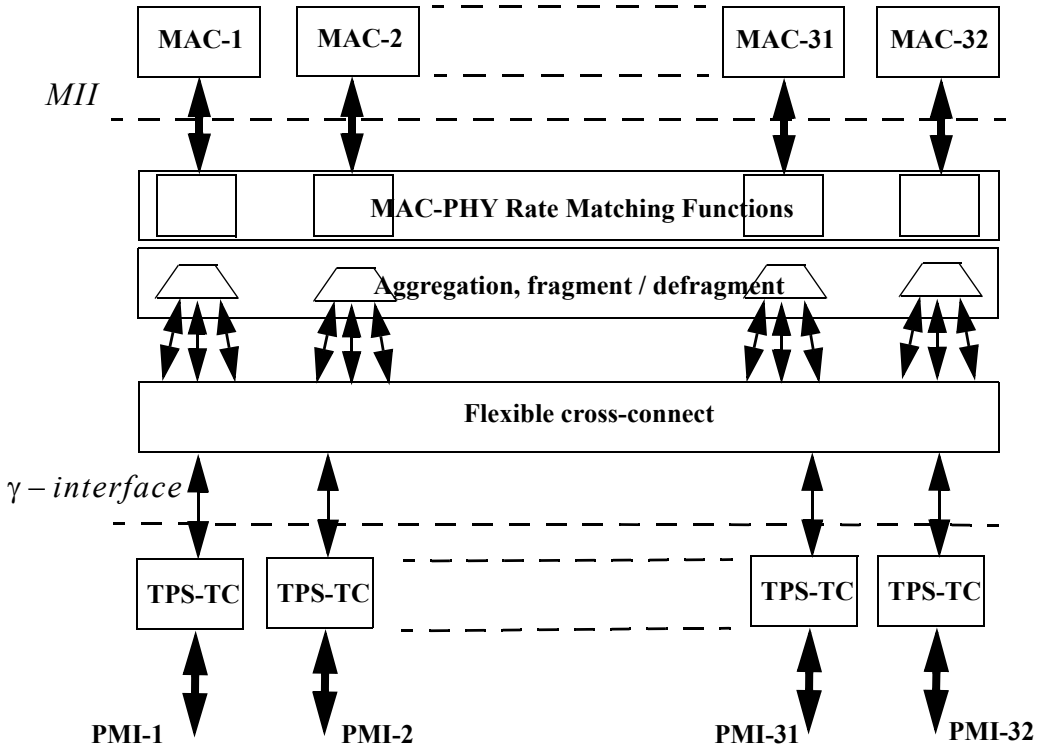


**Figure 61–1—Relationship of flexible connectivity to other PCS functions**

The connection relationship between the PCS instances (including MIIs) and the PMA/PMD instances (including PMI) is defined in two registers: PMD Available register (see 45.2.2.1) and PMD Aggregate register (45.2.2.2 ). Note that the addressing of PCS instances must be independant of the addressing of PMA/PMD instances in order to support the flexible connectivity. This behavior may not be obvious to casual readers of Clause 45.

Note also that the definition of the PMD Available register may seem to imply that multiple MIIs may connect through the same PMI simultaneously but this is not the case. Bits corresponding to the same PMI may appear in multiple PMD Available registers but the PMD Aggregate register for each MII must be set such that each PMI is only actively connected to one (or no) MII. A particular bit set in one PMD Aggregate register shall exclude the same corresponding bit in all other PMD Aggregate registers for the same MDIO connected system.

#### 61.0.0.1.1 Addressing PCS and PMA/PMD instances

The addressing of the MDIO management interface is defined in 45.1, it is assumed that the reader is familiar with the definition of this interface. The examples here assume that only two MMDs are used: PCS (MMD = 3) and PMA/PMD (MMD = 1). The difference between these examples and the example shown in

45.1 is that the PCS instances are addressed independantly of the PMA/PMD instances. Up to 32 PCS instances and up to 32 PMA/PMD instances may be addressed by one MDIO bus. These instances may make up one or more aggregateable sub-domain. The connection of the MDIO bus to the MMDs is shown in Figure 61–2 .

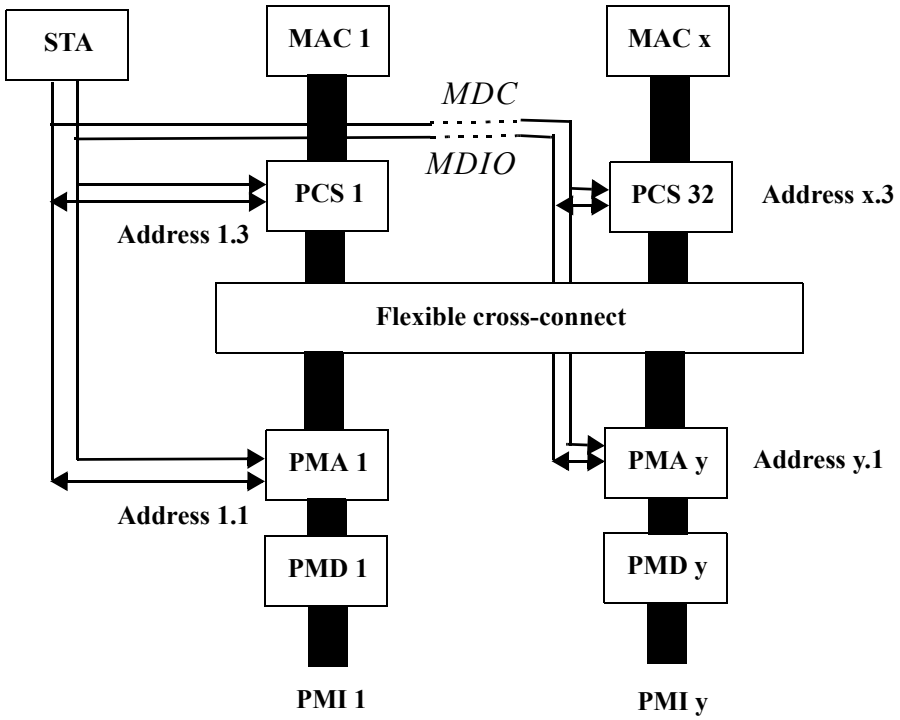


**Figure 61–2—Connection of MDIO bus to MMD instances**

In the example shown there is no necessary connection between the PCS address and the PMA/PMD address. Similarly, the number of PCS instances may be different to the number of PMA/PMD instances addressed by one MDIO bus.

### 61.0.0.1.2 Indicating PMI aggregation capability

The PMI aggregation capability is indicated by the state of the PMD Available register (see 45.2.2.1). A copy of this register is readable for each PCS instance (x) at register addresses x.3.45 and x.3.46. A bit is set in this register corresponding to the PMA/PMD address for each PMA/PMD which can be aggregated through that PCS. Some examples are given which show register contents and connectivity for some popular configuration:

1) Simple two PMI per MII connections, 32 PMIs (PMA/PMD instances) are aggregated into 16 MIIs (PCS instances). PMD available register contents are shown in Table 61–1—. A diagram

**Table 61–1—**

| PMD available register | Contents |
|---|---|
| **1.3.45 / 46** | **b11000000_00000000_00000000_00000000** |
| **2.3.45 / 46** | **b00110000_00000000_00000000_00000000** |
| **etc.** | **etc.** |
| **16.3.45** | **b00000000_00000000_00000000_00000011** |

of the connectivity is shown in Figure 61–3 .

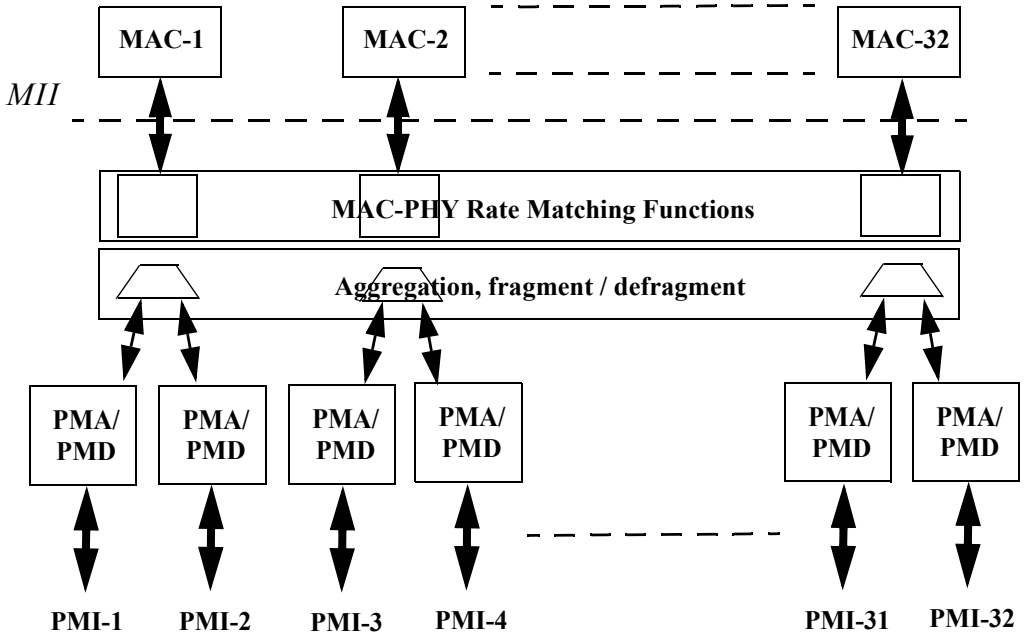


**Figure 61–3—2 PMI for each MII connectivity**

2) Pairs of 2-to-1 connections, 32 PMIs (PMA/PMD instances) are aggregated into 16 MIIs (PCS instances) in a manner that allows each PMI to connect to one of 2 MIIs and each MII to aggre-

gate up to 4 PMIs. PMD available register contents are shown in Table 61–2—. A diagram of the connectivity is shown in Figure 61–4 .

**Table 61–2—**

| PMD available register | Contents |
|---|---|
| **1.3.45 / 46** | **b11110000_00000000_00000000_00000000** |
| **2.3.45 / 46** | **b11110000_00000000_00000000_00000000** |
| **etc.** | **etc.** |
| **16.3.45** | **b00000000_00000000_00000000_00001111** |

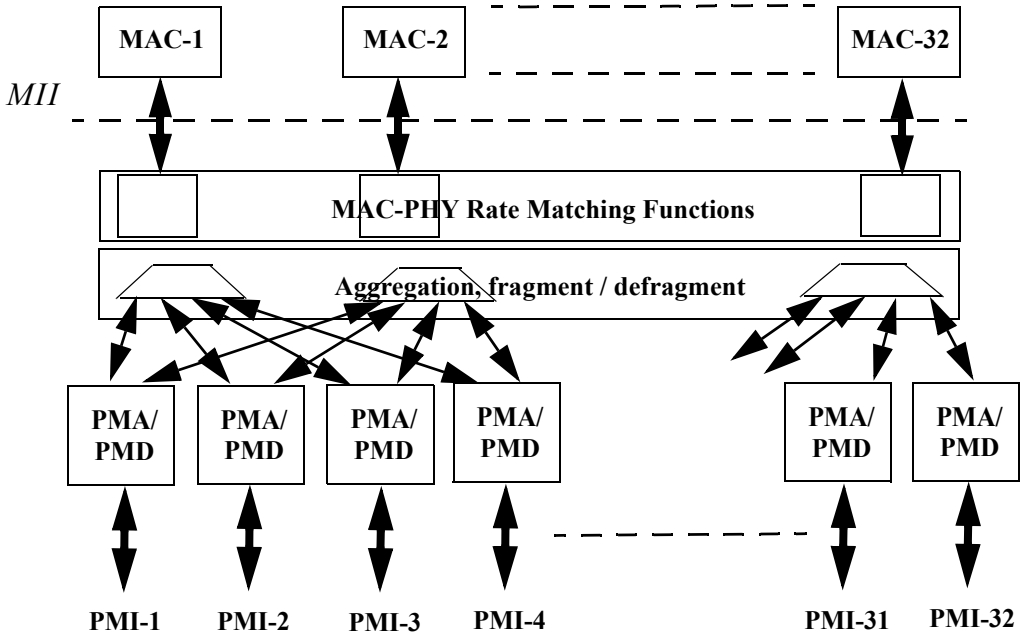


**Figure 61–4—4 PMI for each 2 MII connectivity**

3) 12-to-24 fully flexible connections, 24 PMIs (PMA/PMD instances) are aggregated into 12 MIIs (PCS instances) in a manner that allows any PMI to connect to any MII. PMD available register contents are shown in Table 61–3—. No connectivity diagram is shown as any connection is possible between PMIs and MIIs.

### 61.0.0.1.3 Setting PMI aggregation connection

The PMI aggregation connection is set using the PMD Aggregate register (see 45.2.2.2). This register is writeable for each PCS instance (x) at register addresses x.3.47 and x.3.48. A bit is set in this register corresponding to the PMA/PMD address for each PMA/PMD which is to be aggregated through that PCS. Some examples are given which show register contents and connectivity for some popular configurations:

1) Simple two PMI per MII connections (as shown in example 1) above), the first MII aggregates 2 PMIs, the second MII only connects through 1 MII, as does the sixteenth. PMD aggregate register contents are shown in Table 61–5—.

**Table 61–3—**

| PMD available register | Contents |
|---|---|
| **1.3.45 / 46** | **b11111111_11111111_11111111_00000000** |
| **2.3.45 / 46** | **b11111111_11111111_11111111_00000000** |
| **etc.** | **etc.** |
| **12.3.45 / 46** | **b11111111_11111111_11111111_00000000** |

**Table 61–4—**

| PMD aggregate register | Contents |
|---|---|
| **1.3.47 / 48** | **b11000000_00000000_00000000_00000000** |
| **2.3.47 / 48** | **b00010000_00000000_00000000_00000000** |
| **etc.** | **etc.** |
| **16.3.47 / 48** | **b00000000_00000000_00000000_00000010** |

2) Pairs of 2-to-1 connections (as shown in example 2) above), the first MII aggregates 3 PMIs, the second MII only connects through 1 PMI, the sixteenth MII aggregates 2 PMIs. PMD aggregate register contents are shown in Table 61–5—.

**Table 61–5—**

| PMD aggregate register | Contents |
|---|---|
| **1.3.47 / 48** | **b11100000_00000000_00000000_00000000** |
| **2.3.47 / 48** | **b00010000_00000000_00000000_00000000** |
| **etc.** | **etc.** |
| **16.3.47 / 48** | **b00000000_00000000_00000000_00000110** |

3) 12-to-24 fully flexible connections (as shown in example 3) above), the first MII aggregates 5 PMIs, the second MII only connects through the 24th PMI, the eleventh MII is not used, twelfth MII aggregates 2 PMIs. PMD aggregate register contents are shown in Table 61–6—.

**Table 61–6—**

| PMD aggregate register | Contents |
|---|---|
| **1.3.47 / 48** | **b11111000_00000000_00000000_00000000** |
| **2.3.47 / 48** | **b00000000_00000000_00000001_00000000** |
| **etc.** | **etc.** |
| **11.3.47 / 48** | **b00000000_00000000_00000000_00000000** |
| **12.3.47 / 48** | **b00000000_00000000_00000110_00000000** |