FEC in EPON
Technical Proposal

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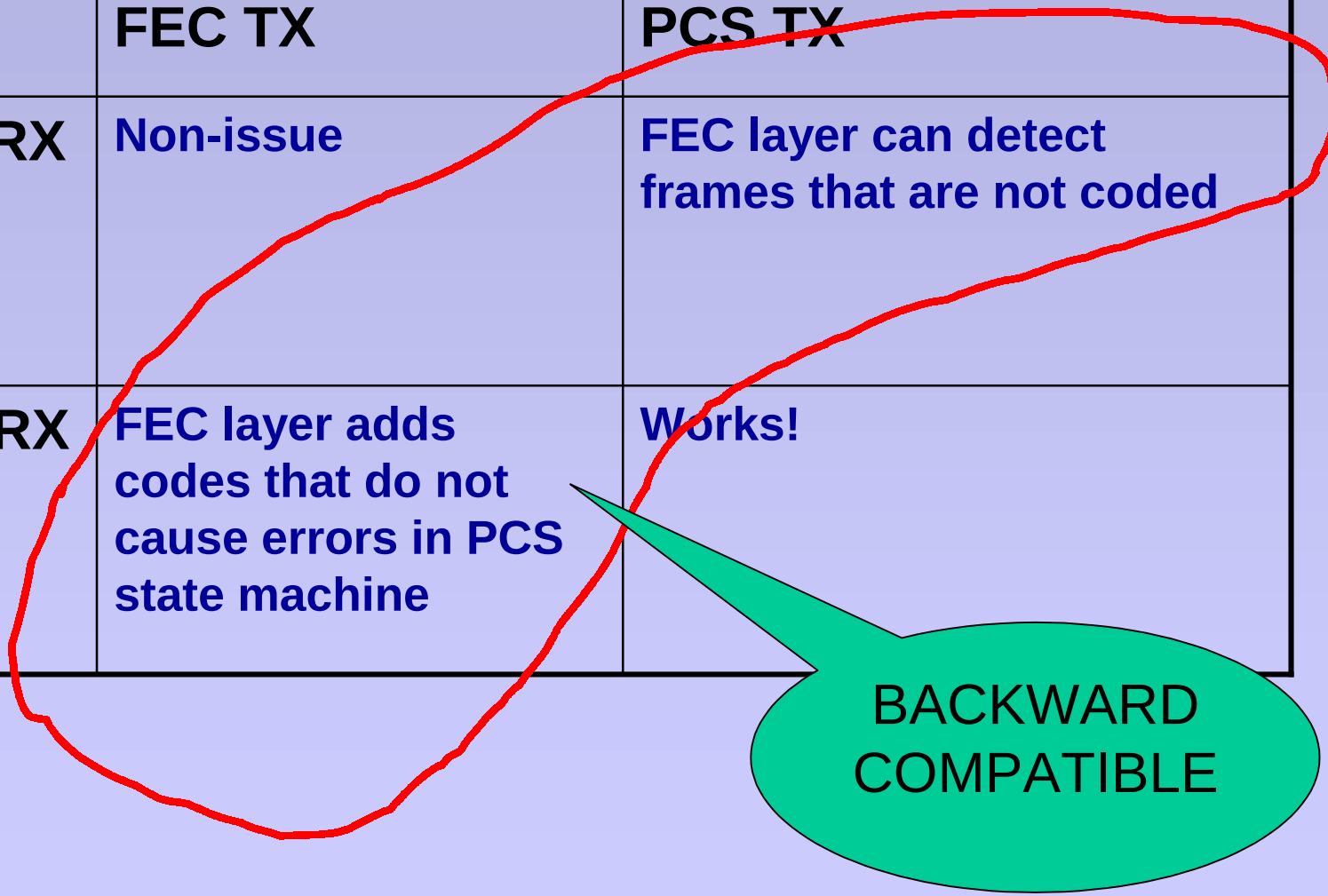
Proposal

- **FEC Line coding**
- **Location of FEC in Ethernet stack**
- **Frame synchronization algorithm and state machines**
- **Analysis:**
  - Mean Time to False Packet Acceptance
  - Start & Stop Miss Detect

FEC Compatibility Matrix

	FEC TX	PCS TX
FEC RX	Non-issue	FEC layer can detect frames that are not coded
PCS RX	FEC layer adds codes that do not cause errors in PCS state machine	Works!



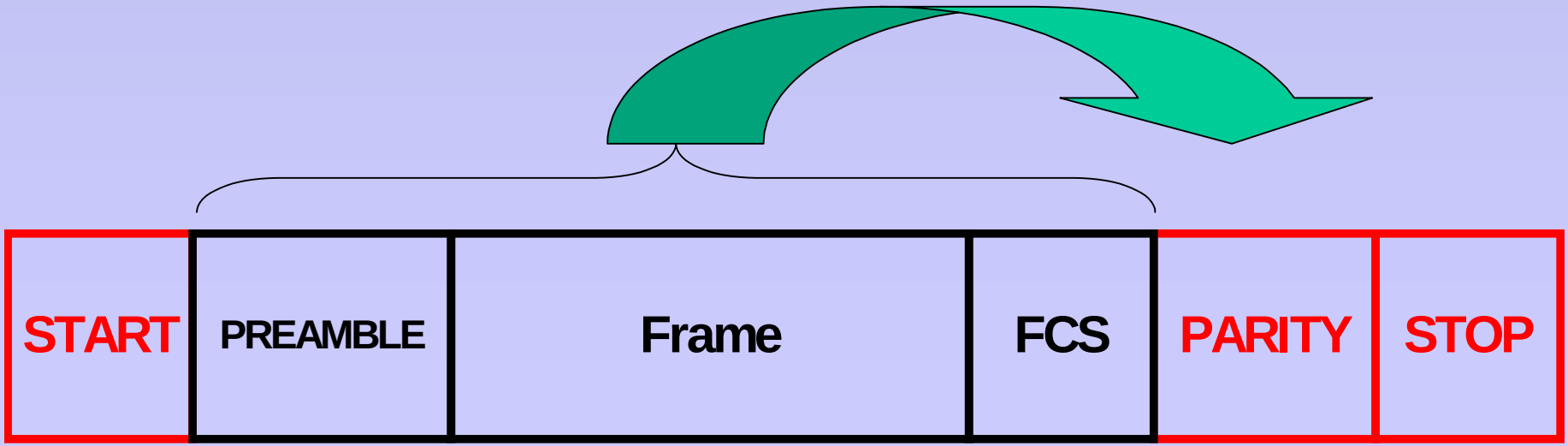
Basic Principles of Operation

- **Keep line rate**
- **Maintaining the atomic frame structure**
  - Parity check bytes added at the end of the frame
- **FEC is coded before the 8B/10B code**

- **Legacy devices observe a normal Ethernet frame**
  - False_Carrier_detect mode of PCS Rx when parity bytes received (RX_ER is asserted)

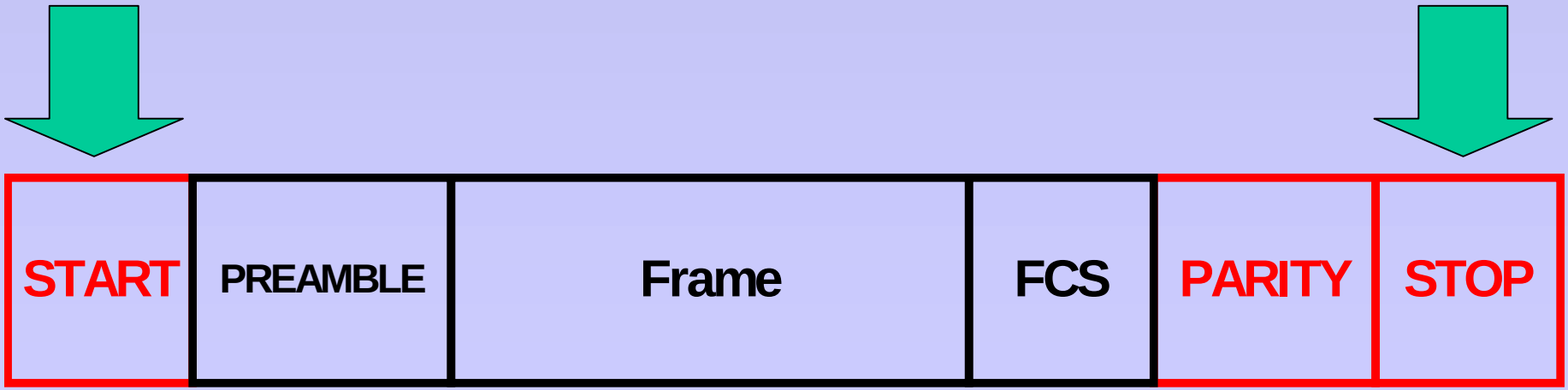
Encoding

- Parity check bytes added at the end of the packet
- All of the packet is encoded including preamble, address and FCS
- Shortened last frame – virtual zero padding
- Idles not protected



Frame Markers

- Special start and stop symbols added
- Symbols are immune to high noise
- Symbols are actually sequences detectable with a correlator
- 60 bit long for noise immunity



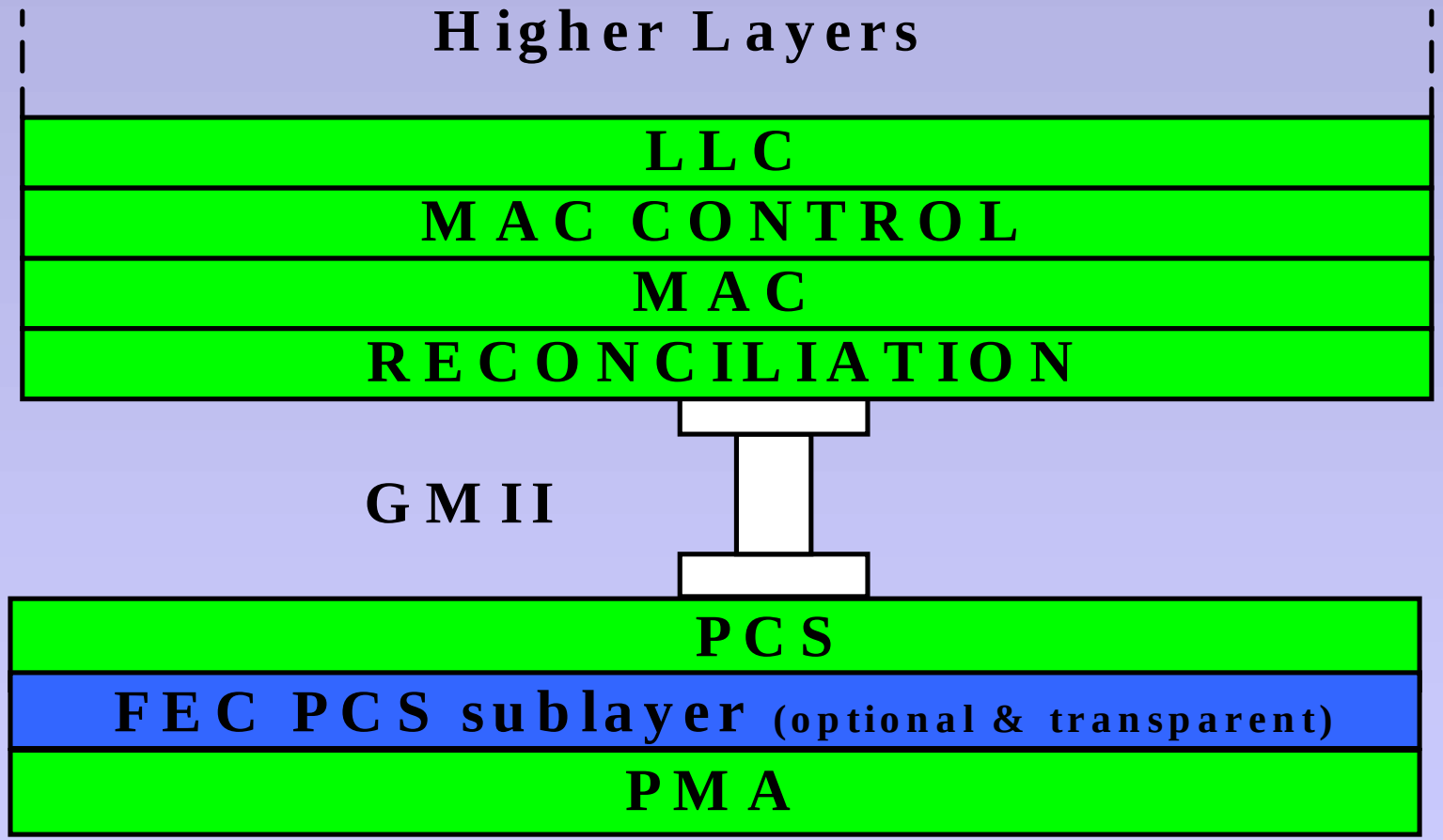
Protection Sequence Selection

- **Sequence is long enough to be detected with very high probability**
  - Scan the input symbol stream for a match with the S_FEC bit sequence and say you have sync when the match has less than d/2 errors
- **Sequence can flow through non-FEC PCS transparently**
- **Suggested codes**
  - /S_fec/ - start of packet - /D21.2/R/K28.5/D16.2/S/
  - /T_fec/ - end of packet - /T/R/K28.5/D16.2/T/R/

FEC Rate Adaptation

- **Additional idles inserted in FEC packet reception instead of additional data**
- **In transmission rate adaptation can be achieved in open loop, IPG stretching, adapting MAC rate**
  - like in the 802.3ae
  - There is a known ratio between the packet size to the additional parity bytes per packet

FEC Layering in Ethernet

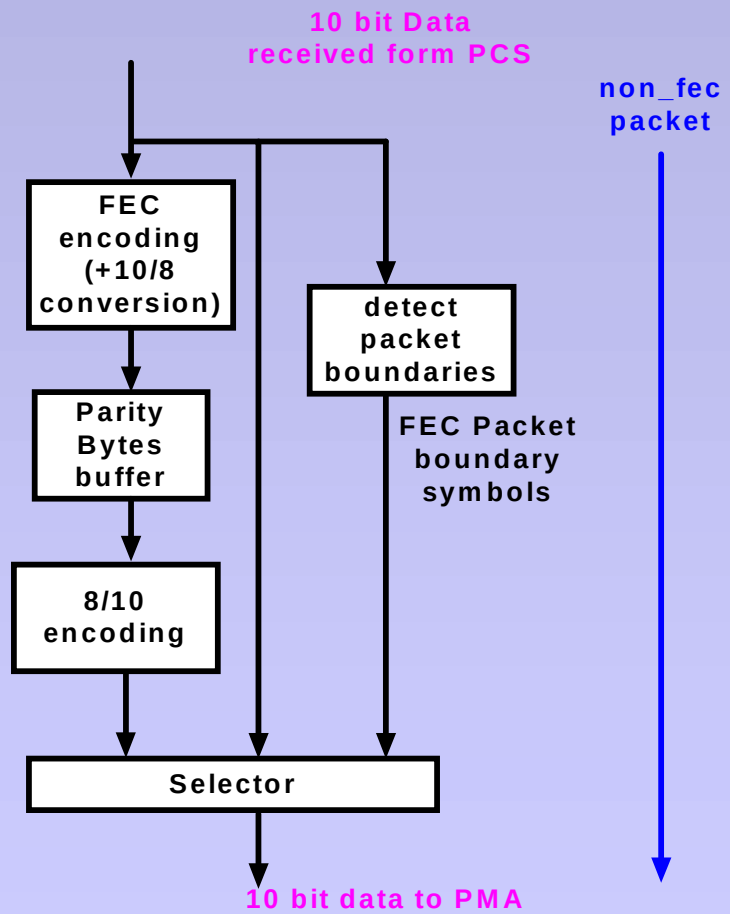


PCS State Machine

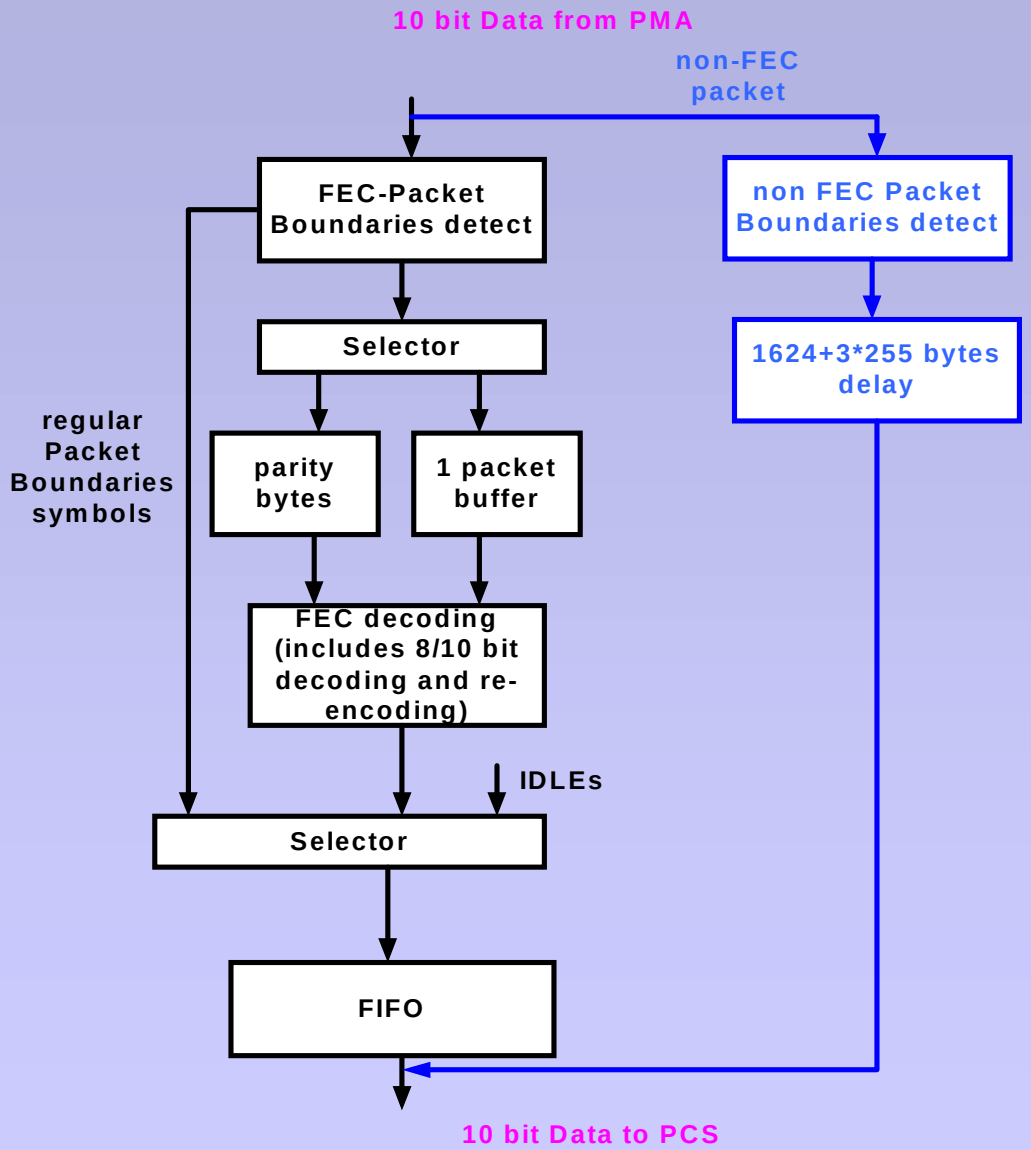
- **RX and TX state machines** remains the same **as legacy 1000BASEX PCS**

Data Flow for FEC Sub-layer - Tx

Packet Tx
FEC Encoding



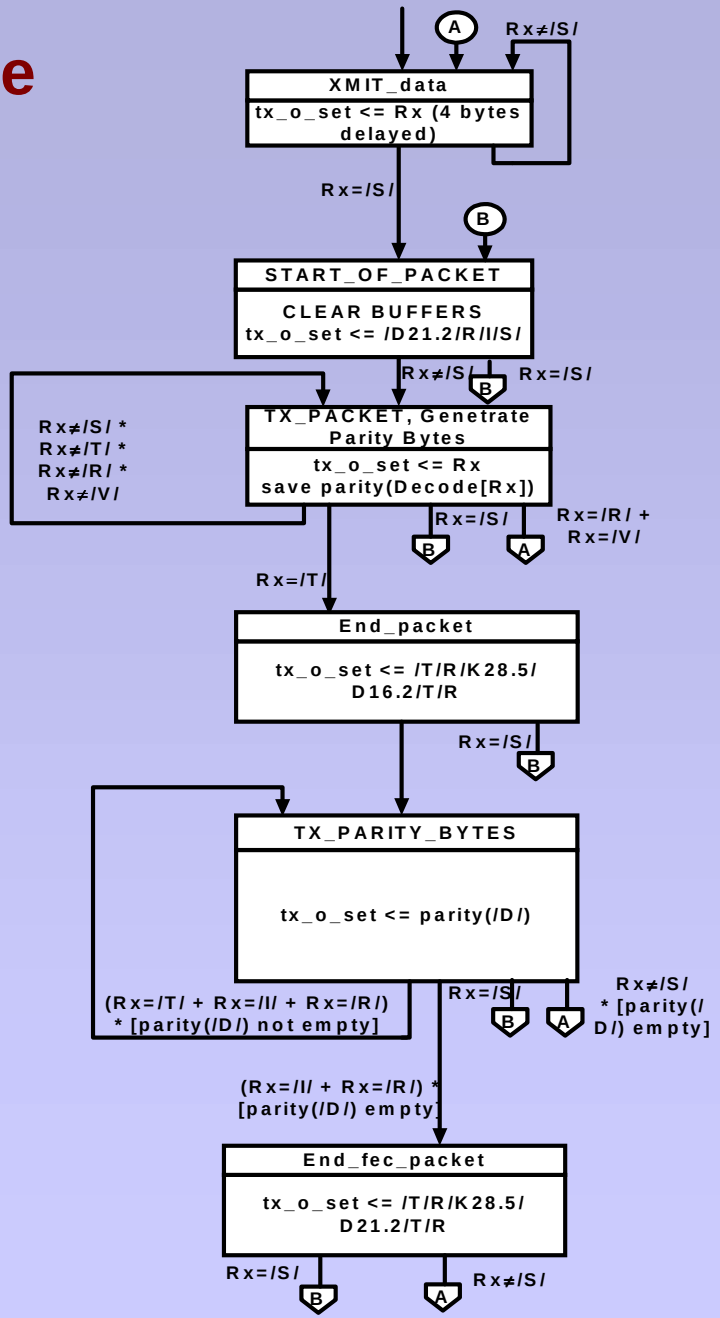
Data Flow for FEC Sub-layer - Rx



RX. FEC Sub-layer

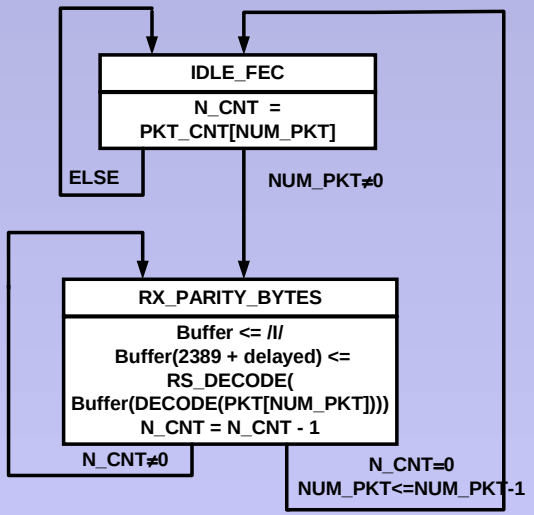
- **RX. FEC Sublayer delays data for PCS by:**
  - one maximal packet (1512) + parity(7*16) + 3 FEC frames (3*255) = 2389 bytes
  - Delay is constant
  - $RX_{t\text{-}delay}$<9:0> is valid at time **t** for the PCS
- **Enhancing Sync in FEC sub-layer**

FEC layer Tx state machine

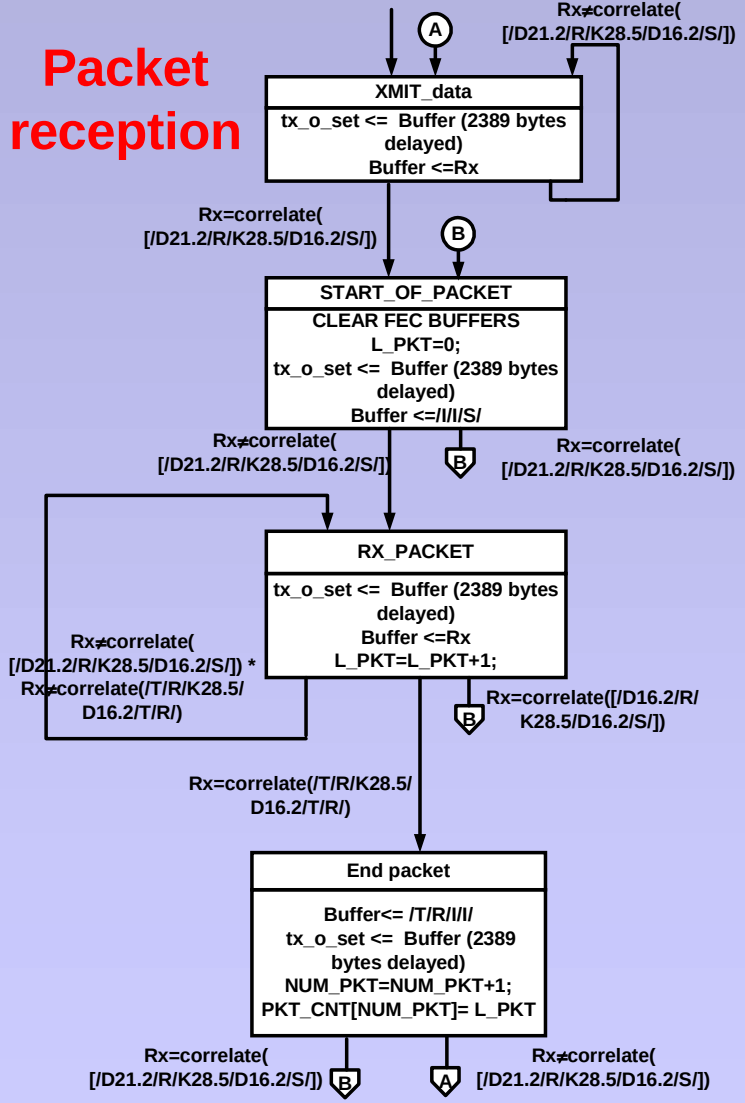


FEC layer Rx State Machine

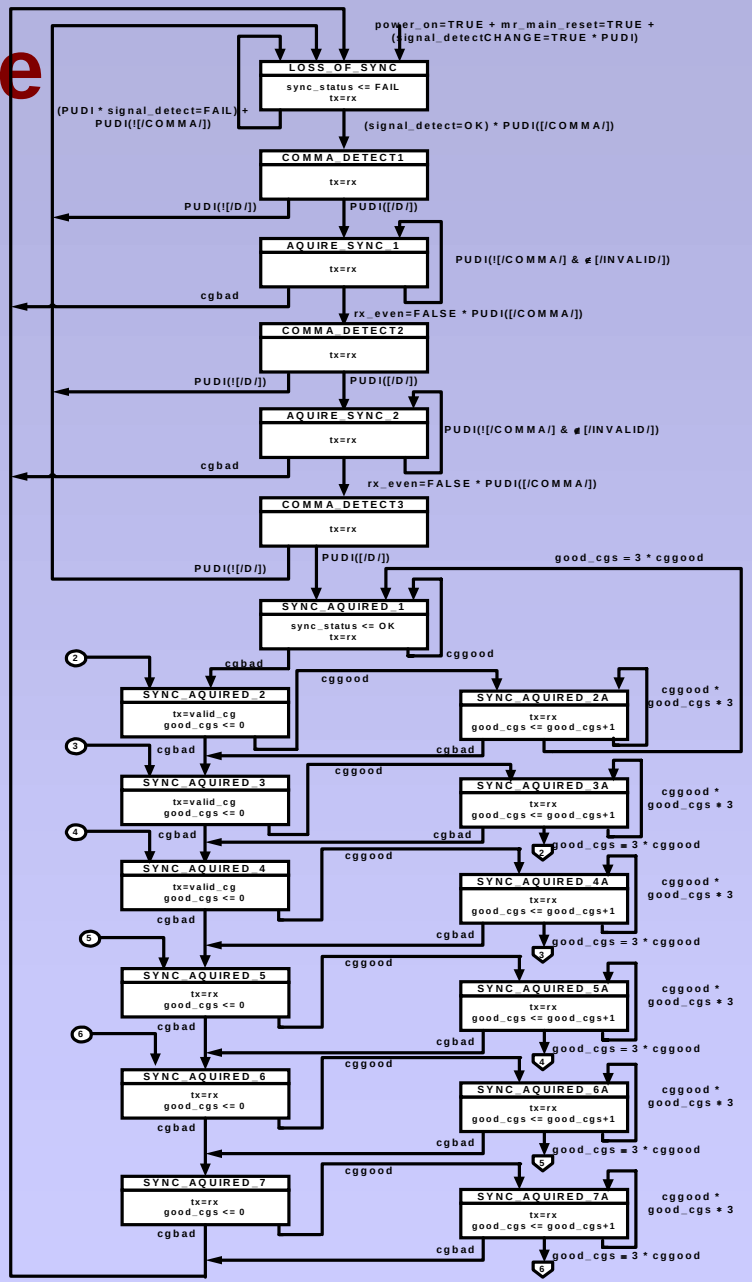
FEC decoding



Packet reception



FEC Sync State Machine



Probability for Lock Errors

- Acquiring is done after detecting 3 commas The probability for error in acquisition is reduce from 3e-11 to 3e-3
- Probability for de-acquiring – After 4 sequential bad words (with hysteretic) – reduced from the order of (1e-11)^4 to (1e-3)^4 – one in every 2hours.
- Increasing the state machine to 7 reduces the probability to the order of (1e-3)^7 – one in every 250000 years

Mean Time to False Packet Acceptance

- Bit error probability before FEC is Pe=1e-4
- Bit error probability After FEC is Pcu=1e-12
- The probability for an FCS error in Ethernet:

$$P_{UD} = \frac{1500}{255} \cdot \frac{P_{CU}}{10} \cdot \left(\frac{1}{2}\right)^{32} = 1.4e-22$$

- Most code-words are not 17 bytes distant The number of 17 bytes neighbors:

$$R_{17} = \frac{\binom{17}{9} \cdot A_{17}}{\binom{255}{9} \cdot (256)^9} = \frac{\binom{17}{9} \cdot \left[\binom{255}{17} \cdot 255\right]}{\binom{255}{9} \cdot (256)^9} \approx 6 \cdot 1e-8$$

Mean Time to False Packet Acceptance – Cont’

- Total probability of undetected errors for Ethernet with FEC – 1e-29
- For 1GE this means an error in 4e16 years

Miss detect in Start & Stop Markers

- **Length of correlation sequence – 6 bytes that are 60 bits – detected with bit correlators**
- **Probability of miss-detect from IDLE pattern**
  - The minimal distance of a sequence from an IDLE pattern is 15 bits –

$$P_{ce} < \binom{15}{7} P_b^7 \approx 1e-24$$

- **Probability of miss-detect from data pattern**
  - The nearest data sequence is 6 bits distant -

$$P_{ce} < \frac{320}{\left(2^8\right)^6} \cdot \binom{6}{3} P_b^3 \approx 2e-23$$

Conclusion

- FEC framing compatible with legacy Ethernet introduced
- Layering proposed below PCS with same 1000Base-X PCS
- Frame format uses IPG for code words
- 60 bit patterns used as markers
- IPG Stretching for Rate Adaptation like in 802.3ae
- Low probability of error propagation shown