Operation, Cost and Legacy Compatibility

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Outline

Note: Assumes FEC scheme proposed in "FEC Framing in EFM", khermosh_1_0102.

- **Codeword generation and packet formatting.**
- **The FEC sublayer and operational overview.**
- **Operational changes with FEC addition.**
- **Cost.**
- **Operation with legacy (non-FEC) nodes.**

Note: The technical benefits obtained with FEC are discussed in other FEC presentations.

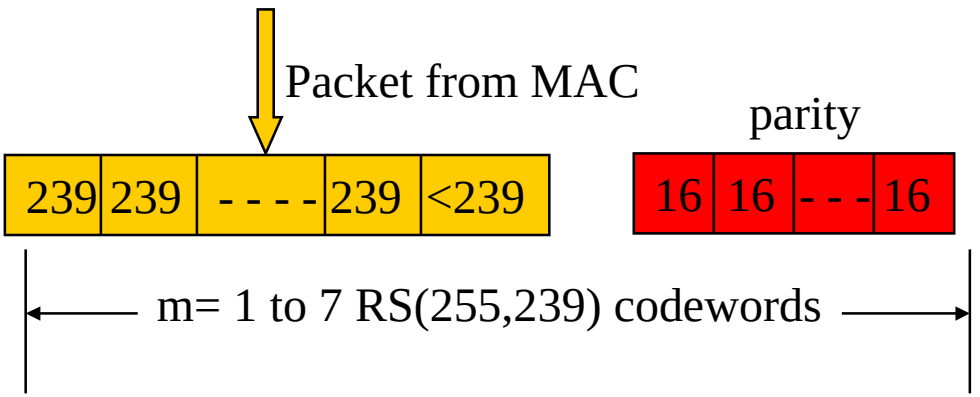
A Systematic RS(255,239) block code is proposed.

A Systematic block code is a code in which the encoded data is left unaltered and parity information is appended. Adding a systematic code to EFM requires finding a way to:

1. **transport the new, additional parity bytes across the link.**
2. **Increase robustness of non-FEC'd control codes.**
3. **detect the parity bytes.**
4. **impart flow control due of the increased size of the inter packet gap.**
5. **Operate with legacy 1000BASE nodes.**

Forming the RS(255,239) Codewords

1. Divide Packet into k= 239 byte codeword information sub-blocks.
2. Short packets (<239bytes) and remainder of large packets treated as a shortened codeword.
3. Encoder generates a 16 byte codeword parity sub-block for each k.
4. There will be from m = (1shortend) codeword to (6 + 1shortened) codewords/packet.

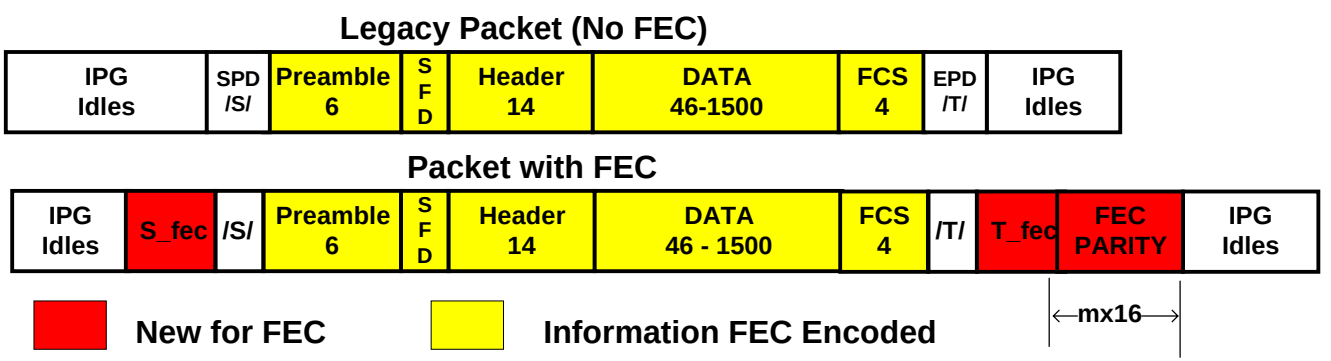


Packet Changes with FEC

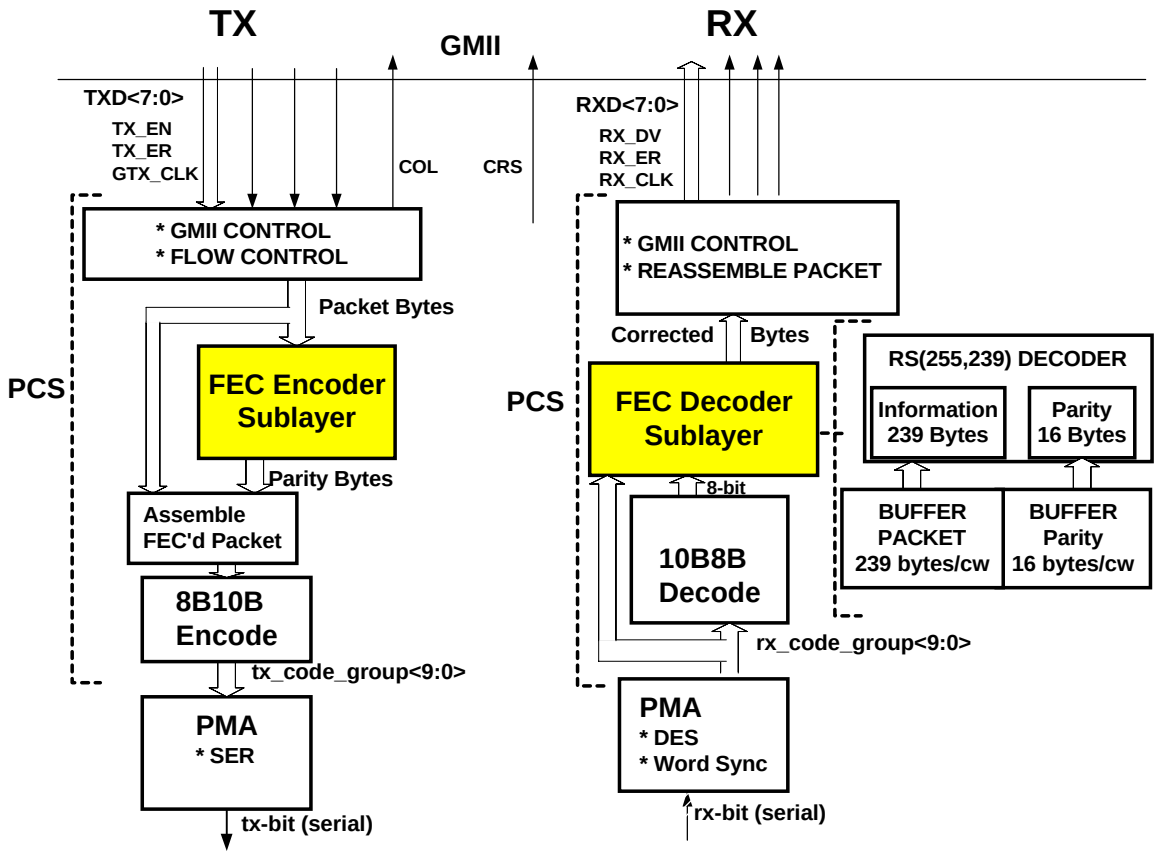
1. FEC code is RS(255,239), where,
   n= Codeword size = 255 bytes
   k= Number of Information bytes = 239 bytes/CW
   (n-k)= Number of parity bytes = 16 bytes/codeword

2. SPD and EPD extended to increase robustness

3. Transmit last codeword as shortened code if < 239 bytes.
   Number of CW's/packet = m (1 to 7)



The FEC Sublayer



Operational Changes with addition of FEC.

1. **Flow control needed because FEC adds approximately 6% overhead to the packet. Can use IPG stretching as in 10G or a new scheme using MAC control signals CRS and COL.**

2. **Special SPD and EPD codes needed because they are not FEC encoded and the need to recognize FEC'd and non-FEC'd packets.**

3. **Because whole packet must be received before FEC decoding, there will be additional latency time:**

Max Latency approx. = 1500 bytes x 8bits/byte x 1Gbits/s= 12usec.

Cost of Adding RS(255,239) FEC is Negligible.

1. **Approximately 37K Gates for a 1G RS(255,239) implementation. Based on actual designs in 0.35u CMOS. Pipeline decoder processing at 1byte/clk (125MHz clock). 50 to 100 mW in 0.18u CMOS.**

2. **Compared to OLT/ONU cost and system benefits gained, the cost of adding FEC to EFM is negligible.**

Legacy Compatibility

1. **The FEC'd packet structure still contains the unaltered original packet.**

2. **FEC'd packets are therefore compatible with legacy 1000 BASE-X nodes.**

3. **The only difference will be the generation of False_Carrier-detect caused by the parity bytes.**

Note: See the khermosh_1_0102 Raleigh presentation for detailed state diagrams.

Summary

1. **Adding an FEC sublayer to the existing 1000BASE_X PCS and PMA (Clause 36) is straightforward.**

2. **Considering the benefits, the cost of adding FEC to EFM is negligible.**

3. **Operation with legacy nodes is maintained.**