Status of Interoperability Study for 100Base-LX10

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The Problem

- There is a general expectation that we will be able to use existing devices for this interface.
  - 100Base-TX/FX PHY chips
  - OC-3 Transceivers
- The current designs for these parts may produce problems in some combinations
- To provide additional information as input to developing the 100Base-LX10 specification a number of vendors were polled

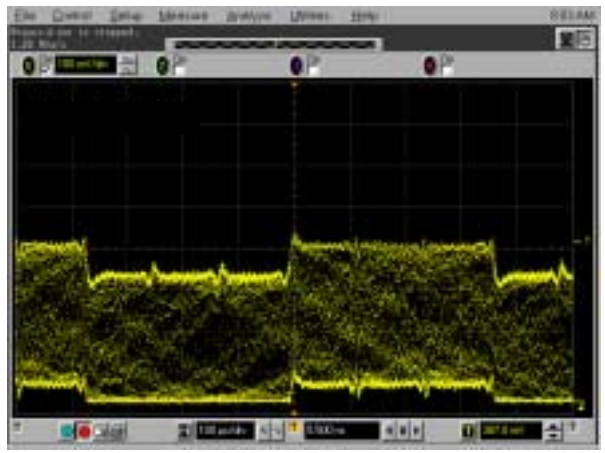
Vendor Poll

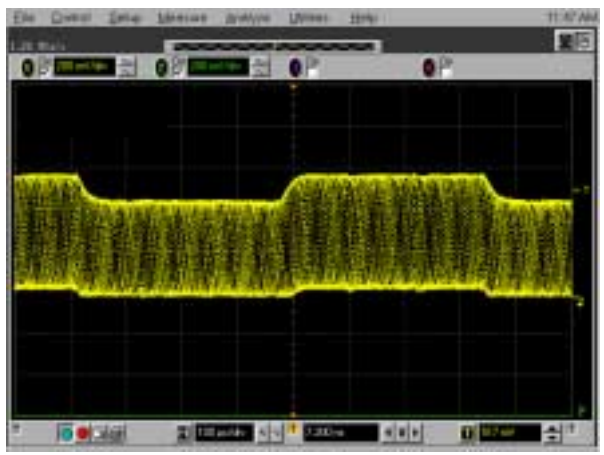
- Vendors were polled as to the characteristics of their transmitters, receivers and clock recovery circuits
  - 5 PMA Vendors, 9 PMD Vendors
  - A reasonable number responded
  - The detail of the responses varied widely
- Many reported serving this market for a long time and having no negative customer feedback.
- The following is a compilation of vendor responses and my interpretation
  - Attempting to keep vendor anonymity at the request of several vendors

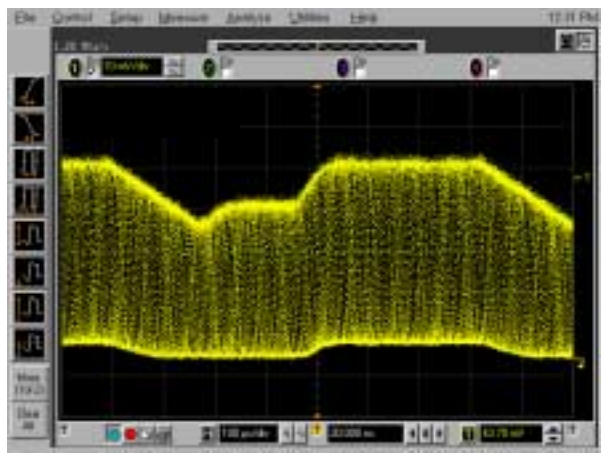
Transmitter Overshoot

- SONET based transmitters are designed for a balanced pattern without baseline wander
- The response of the average power control is not critical
- Some transmitters have the average power control feedback loop characteristics that may cause problems with unbalanced patterns

The Envelope Response to the BLW Pattern Varies Greatly







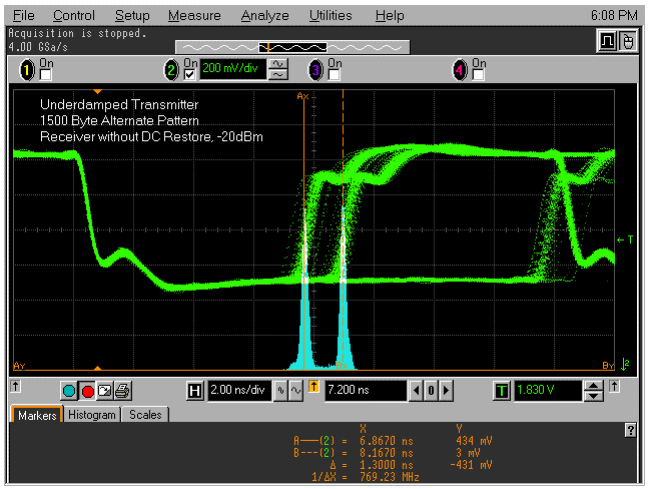
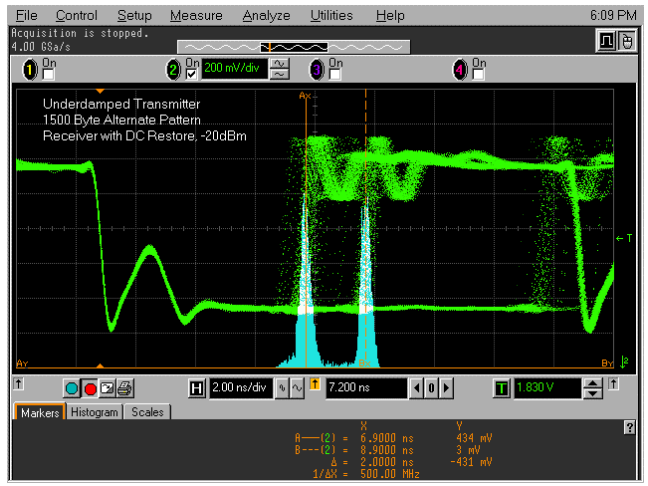
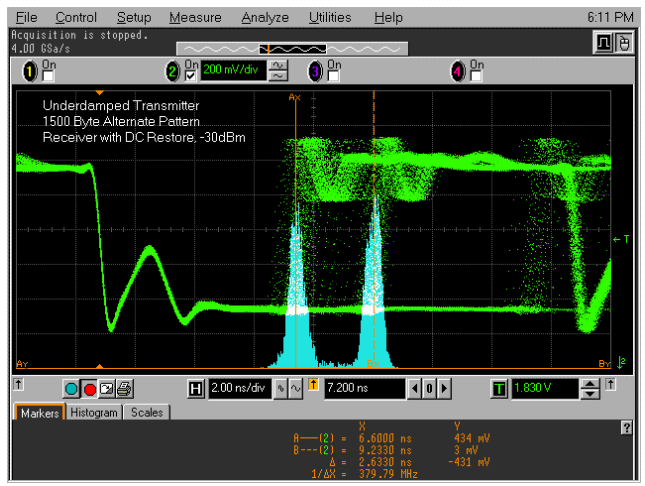
Average Power Control

- The average power control has no industry standard
  - Designed for scrambler based patterns. Tested this way.
  - The time constants vary widely
  - Damping constants vary widely. (Only a few are under-damped)
  - At least one vendor has a slew rate limit situation with a BLW pattern
    - The sensitivity impact is small
- 100Base-LX10 will have to live with this
  - Accept the impact on sensitivity
  - The option is to require changes from the vendors
  - Cost impact

DC Cancellation Circuits

- Some receivers are designed with a DC cancellation circuit to automatically compensate for internal offsets and achieve the best sensitivity.
  - Feeds back a correction signal that expects a balanced data pattern
- When subjected to an unbalanced pattern the internal operating point is upset to attempt to achieve a balanced output.
  - Additional duty cycle distortion is introduced by the receiver
  - Effect varies with signal level

DC Cancellation Measurements

	Without DC Cancellation	With DC Cancellation
-20dBm		
-30dBm		

DC Cancellation Circuits (cont.)

- Simulation was carried out to determine the effect
- The results are strongly dependent on the bandwidth and waveforms of the receiver at the input to the limiting amplifier
  - Simulation with a 4th order B-T filter
  - The effect of signal level was not modeled

		DCD (ns p-p)	
		w/o DC Can.	w/ DC Can.
Simulation	117 MHz	1.25	5.60
	94 MHz	1.60	6.38
Test Data	-20dBm	1.3	2.0
	-30dBm	1.4	2.6

  - The measurements were worse than the simulation without DC Cancellation and better with DC Cancellation

DC Cancellation (cont.)

- The majority of vendors report the presence of DC Cancellation circuits
  - Maximizes sensitivity of receiver, allows one design to be used for multiple applications
  - Low cost – Typically located in the PIN/TIA can
- The DCD introduced by these circuits is not as great as simulation would indicate
  - Limited adjustment range reduces impact at high signal levels.
- We will have to live with this effect
  - Due to our low sensitivity requirements (-25dBm) the effect should not be large
  - I will make additional attempts to quantify the numbers

Clock Recovery

- Vendors reported both single and dual edge clock recovery
- The differences are not as great as they may seem
  - Dual edge clock recovery has a dead zone in the clock alignment in the presence of DCD
  - The dead zone is reduced at low optical signal levels by the presence of noise induced jitter on the data edges
- The critical factor is the clock alignment and edge tolerance
  - A well designed single edge clock recovery will outperform a poorly designed dual edge system
- At this time I do not have good numbers on this
  - Continuing to enquire

Recommendations

- All of the bad effects are present in a significant portion of the vendors
  - Envelope distortion due to BLW
  - DC Cancellation circuits increasing DCD
  - Single edge clock recovery
- 100Base-LX10 will have to live with them
- Recommended Approach
  - Assign a penalty for envelope distortion (.5dB?)
  - Get vendor feedback on max DCD at –25dBm
  - Design the eye mask and jitter tables based on single edge clock recovery
  - Poll vendors on alignment tolerance